VLSI Implementation of Digital Filter

Professor Disha Bhosle[1] Vikas Anaokar[2] Omkar Dixit[3] Aditya Trivedi[4]
[1]Head of Dept. [2,3,4]Student
[1,2,3,4]Department of Electronics
[1,2,3,4]Atharva College of Engineering

Abstract— Designing digital filters mathematically, and verifying their functions, is a simple task with the help of many available electronics CAD software such as MATLAB. With the growth of Programmable Logic Devices (PLD), and Field Programmable Gate Array (FPGA) devices, implementing hardware digital filters became an easy task. PLD and FPGA implementation approach has both, performance of ASICs and flexibility of software. Hence to learn practically how the digital filters work in a computer based environment and then implementing it on PLDs gives a basic idea of implementing algorithms on circuit design level to enhance the concepts. The designed filter can be used to remove powerline interference from the ECG signal. Power line interference cause uneven spikes at 50/60 Hz frequency and can cause inaccuracy in ECG graphs. Hence, this noise has to be eliminated and can be done through IIR/FIR digital filter.

Key words: VLSI, Digital Filter

I. INTRODUCTION

Digital filters are commonly used in various applications in signal and image processing domains. VLSI implementation of filters gives an application specific design for integrated circuits. Designing filter on circuit design level includes design of certain digital circuits like: Adders, Multipliers and flip flops. The mathematical relation of transfer function will be translated into digital circuits with the help of these circuits. Modified Booth Algorithm optimizes the power consumption and size for the design of multiplier. Hence, using the algorithm overall the circuit will have less power consumption and smaller size than primitive designs. This approach will enhance efficiency and reduces the cost of current systems.

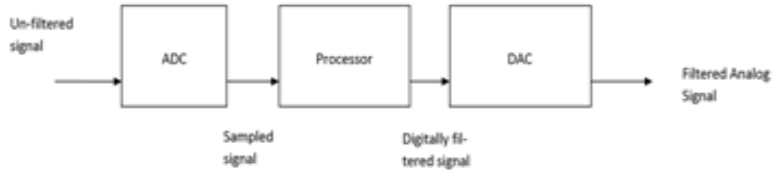

Fig. 1: Block Diagram of general signal processing system

II. LITERATURE REVIEW

1) Bishar and Ziyad [1] explained implementation of simple digital filters like IIR filter of first order on programmable logic device using simulation tools like MATLAB and MAXPLUS II for educational purpose. The paper states the realization of filters by calculating the coefficients of filter and using them with complex programmable logic device (CPLD) along with different types of response like impulse and sine wave response. Higher order filters can be implemented using higher order using advanced PLDs (FPGA).
2) Shelja and Shreena [2] proposed the design of modified booth algorithm to implement the multiplier used in the design of a filter. The salient feature of this proposed algorithm is only n/2 clock cycles are needed for n-bit multiplication as compared to n clock cycles used in Booth's algorithm. The results show that the modified Booth multiplier based FIR filter leads to the smallest area, reduced cost and power consumption. Delay time is also further reduced.
3) Farrell and Williams [3] explained the overview of general DSP concepts, filter design principles as well as techniques to implement filters in FPGA using VHDL. Method of designing with programmable logic has become more efficient with advent of Hardware Description Language (HDL). The two primary HDL's used today are Verilog and VHDL. When implementing a digital filter there are 2 choices: using a dedicated DSP processor or using hardware approach with PLD. Since PLDs are dedicated hardware, they can achieve significant performance increase over DSP processor other advantages include reduced power consumption. PLD's realize logic function by interconnecting predefined hardware logic resources such as gates and registers on IC. Implementation of fixed point math require less space in FPGA compared to floating point math. CPLDs are built in a non-volatile memory type technology and FPGA's are usually constructed in volatile memory CPLDs can be programmed once and maintain their configuration permanent but for most FPGA's the configuration is loaded when powered up and is lost when system is powered down. FPGA's are more register than CPLD. FIR filters require more filter coefficient than IIR for equivalent responses than IIR for equivalent responses. An FIR filter can be designed to have linear phase response. An IIR filter can directly emulate analog filters. Standard transformation can be used to convert Butterworth, Bessel and order conventional analog filters onto digital filters.
4) Chandarkar et al [4] surveyed about the types of noises and techniques used to remove the unwanted noise from the ECG signal. The ECG gets corrupted due to different kinds of artifacts like power line interference, electrode contact noise, motion artifacts, baseline interference, and muscle contraction and instrumentation noise due to electronic devices. Analog

filters can be used to remove these noises, but nonlinear phase shift is introduced by them. ECG signals are of very low frequency of about 0.5 to 100 Hz and digital filters are suitable to remove noise from low frequency signals. FIR filters are always stable because they have non-recursive structure. They have exact linear phase and are efficiently realizable on hardware. The digital FIR filter with Kaiser Window removes the artifacts from ECG with less modification in waveform. Use of rectangular window gives more distorted signal and hence leads to improper diagnosis.

5) J. A. Van Alste and T. S. Schilder [5] has developed the FIR filter for removal of baseline and power line interference due to the linear phase characteristics of FIR filter. This had also reduced the no. of computations involved in digital filters using desired filter spectrum , Neeraj Kumar et.al have introduced the Butterworth IIR filter and FIR type –I filter for removal of noise present in ECG signal in "Reduction of Power Line Interference in ECG Signal Using FIR Filter". FIR filter has been designed for removal of 50/60Hz power line interference present in ECG signals.
6) Phuong [6] discussed FIR Filter Design with the Window Design method. The design of a FIR Filter starts with its specifications in discrete time domain or DTFT frequency domain, or both. In the time domain, the design motive is the impulse response. In the frequency domain, the requirement is based on various parameters of the magnitude response. Analyzing all the fixed windows, the only adjustable length (M+1) was of Kaiser Window. The Kaiser window has an additional ripple parameter β, helping the designer to balance the transition and ripple.

III. PROPOSED IDEA

The design of a digital filter involves following three steps:

- Filter Specification: This includes stating the type of filter, for example low-pass filter, the desired amplitude and phase responses and the tolerances, the sampling frequency, the word length of the input data.
- Filter Coefficient Calculation: The coefficients of a transfer function H(z) is determined in is this step, which will satisfy the given specifications. The choice of coefficient calculation method will be influenced by several factors and the most important are the critical requirements i.e. specification. The window, optimal and frequency sampling method are the most commonly used.
- Realization: This involves converting the transfer function into a suitable filter network or structure.
- In the pass-band, the magnitude response has a peak deviation of ∂p and in the stop band; it is a maximum deviation of ∂s. The difference between ω_s and ω_p gives the transition Width of the filter and transition band determines how sharp the filter response is. The magnitude response decreases monotonically from the pass-band to stop-band in this region. The following are the key parameters:

1) ∂p Peak pass-band deviation (or ripples).
2) ∂s Stop-band deviation.
3) ω_s Stop-band edge frequency.
4) ω_p Pass-band edge frequency.
5) F_s Sampling frequency.

Thus, the minimum stop-band attenuation, A_s And the peak pass-band ripple, A_p, in decibels are given as

$$A_s \text{ (stop-band attenuation)} = -20 \log_{10} \partial_s$$

$$A_p \text{ (pass-band ripple)} = -20(1 + \log_{10} \partial_p) \text{ [7]}$$

Another important parameter is the filter length, n.

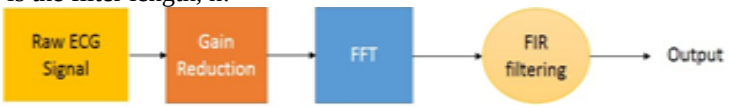

Fig. 2: Block Diagram of Filtering of ECG signal

Fig. 3: Flow of the complete project

The Raw ECG waveform with power line noise is plotted on MATLAB. The waveform is then reduced to normal form by reducing the gain by dividing it by gain of amplifier in last stage of ECG machine. The FFT is taken of the raw signal. Here we observe sudden surge at 50 Hz frequency which shows presence of noise in the ECG signal. This is then filtered using FIR filters. The filtered signal is then taken as output and compared with filters like IIR filter.

After generating the magnitude and phase response, filter coefficients are generated and stored. These are then used to convert the MATLAB code to HDL code using HDL coder in MATLAB. The HDL code uses these fixed point coefficients. The HDL code is then optimized by using modified booth algorithm. This generated code is then implemented on PLD device like CPLD and FPGA.

IV. ADVANTAGES

1) Noise removal from signal
2) Low distortion in the original signal
3) Less power consumption because of use of Booths multiplier
4) Comparatively less area than generic devices
5) Better Readability of ECG signal.

V. APPLICATIONS

A. Echo Cancellation

- Telecommunications
- Data communications
- Wireless communications

B. Ghosting Cancellation In

- HDTV
- DTV
- Video Processing

C. Multi-Path Delay Compensation

D. Speech Synthesis

E. Waveform Synthesis

F. Image Enhancement In

- HDTV
- DTV

G. Filtering

- High-speed modems
- Biomedical Applications

H. Black Box in Air Planes

VI. CONCLUSION

It is studied that digital filters have an advantage over analog filters as use of analog filters introduces non-linear phase shift. Among digital filters, FIR filters are stable as they have non recursive structure. They give exact linear phase. The digital FIR filter with Kaiser Window removes noise with less modification in original waveform. Use of rectangular window gives more distorted signal. IIR filters were studied to have nonlinear phase response but they are easy to be implemented on hardware. IIR filters tend to attenuate the power line noise in the ECG signal but also attenuates other neighboring frequencies which affects the ECG waveform. At the hardware level, IIR filters are easily implementable on a CPLD board. It has lower order and uses less number of multipliers and adders compared to FIR filter. Digital filters on hardware can also be optimized using modified booth algorithm. Using booth algorithm, many researchers have found low power consumption, less chip area and optimized speed.

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