Design of Reversible Ternary Content-Addressable Memory (TCAM) Design using verilog HDL

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Abstract— Ternary CAM is an improved version of CAM memory which could be used for broader searching operations. It searches input data among stored data and gives the output as the matched data. Now a day Ternary CAM became very popular for its deterministic and quick searching ability as it operates in parallel to compare the data stored with the search data. Reversible method has also gained its name in the industry because of its feature of ultra-low power-characteristics. Hence the reversible-logic has been used as an alternate option for limiting the power consumption in the current design scheme of TCAM cell. The proposed method includes the design of different sized 4x3, 4x4 and 4×5 R-TCAM arrays using individual TCAM cells which are completely built by reversible elements to overcome with the power problem. The optimized limits of a reversible TCAM memory cell are estimated as worst case delay, garbage outputs number and quantum-cost of the design. This proposed model provides us the greater matching and searching ability for fast running applications such as in routers and some networking equipment.

Key words: TCAM, Garbage output, Quantum cost, Reversible logic, Content addressable memory, Power consumption

I. INTRODUCTION

In many high-performance network applications the need of a special kind of memory called as Content-Addressable-memory which is different than a Random-Access-Memory. Here these type memories are mentioned as CAM and RAM in short forms throughout the chapters. Normally in RAM an operating system must uses the memory address to obtain the data stored at this address location. But in CAM an operating system operates in opposite manner, here the operating system must uses the data stored and meanwhile CAM work is to produce the address location in the memory where the data is located. In a regular type memory like RAM the memory can access only one location at a time. Where as in CAM can access the entire memory locations in a single operation, hence we can conclude that CAM is comparatively fast memory than RAM. But the designing a CAM will leads to complex design and also expensive in building it. It also consumes much power and generates heat into the system during high speed manipulations. Thus it concludes that CAM has a disadvantage of high power dissipation during the matching and searching contents.

The CAM is also called as a binary CAM as it operates with only two states logic '0' and logic '1' and hence we can use it for exact matching values. Whereas the improved version of CAM is called as TCAM which stands for Ternary Content Addressable memory having the operating states as logic '0', logic '1' and logic 'X'. Where 'X' denotes the value of don't care state or unknown state. By using this TCAM we can able to search for the third state also hence we named it as a Ternary CAM. The TCAM has the capability to use the third state as the mask bit to manipulate which bit is to be matched and which to be ignored as don't care. The all type high performance routing networks and equipments always use TCAM incorporated into it as into the high functional routing tables and special type of lookup-function tables.

To design such a TCAM cell many techniques were into the design industry. As the speed of operation the TCAM memory is very high and the larger and larger computations needed to be carried out quickly there might a chance of losing the information. This losing of information may cause the generation of lot of heat into the system. To overcome this we use the circuits designed with reversible-logic elements because the reversible-logic circuits have been proven ideally with zero dissipation of heat into it. Hence we used the reversible-logic gates to design the TCAM cells to minimize the dissipation of heat in it.

The proposed method includes the design of 5 bit wide 4×5-TCAM array using reversible type gates and also presents the 4×3-TCAM array along with a basic TCAM cell. A SRAM cell is also designed with reversible objects for storing data bit in the TCAM cell. The match-line and the search-line are also realized with reversible gates. This proposed scheme incorporates several reversible-logic gates into the design which are named as Feynman Gate, Fredkin Gate and Peres Gate. The entire design modules are verified and simulated with the help of Xilinx-ISE simulator.

II. LITERATURE REVIEW

There are two interesting things outcome while designing any combinational or sequential circuit design. The first thing is how to optimize the speed of operation of any circuit and the second thing is how to optimize the factors which affect power utilization by these high speed circuits. In the faster network circuits the use of special kind of memory elements like TCAM needed for broader search as well as speedy searches. In the modern days the reversible-logic type design attracting more as it is having ultra lowest power plans. For designing any low power circuit, we must use the reversible-logic elements to overcome with power problems.

According to Prashant R.Yelekar[1], the reversible-gates can be helpful in all regular circuits to realize the Boolean functions. He has presented concepts for some important reversible gates such as Fredkin gate, Feynman gate, Toffoli gate and Peres gate. He has used these gates to build the complex circuits including both combinational and sequential circuits.

Similarly the memory elements used in RAM like D flip-flop and RS flip-flop are also designed by using the reversible gates and this was proposed by Nagarjuna S [2] and some others. Their proposed designs were bought comparatively better results with the existing ones. The main purpose of their design is to reduce the power by optimizing the gate parameters such as quantum cost, number of garbage outputs and depth of the circuits.

Mathew Morrison [3] and some others proposed the design of SRAM and DRAM arrays using reversible-gate and decoder. They were also presented a MLMR gate which was used for controlling the read/write operations in SRAM cell.

Shailja Shukla[4] and some others proposed a lowest processing unit carry look ahead adder using reversible objects and design was simulated using Micro-wind 3.1 simulation tool on 90nm scale technology. They got design was optimized with 47ns delay, 0.2 mw power consumed and 245μm^2 area acquired.

Md. Saiful Islam [5] presented a novel on quantum-cost-efficient reversible full-adder gate in nanotechnology. Here the gate can be a universal gate which means it is used for synthesizing any Boolean functions. Normally this gate is referred as the Peres Full Adder Gate.

Dejan Georgiev [6] presented a CAM chip model designed at architectural level. He has also presented the two power reducing techniques, first one is pipelined-power scheme and the second one is modified-pre-computation based approach.

Zahid Ullah [7] and some others have proposed an SRAM based architecture for TCAM in which they have used the benefits of SRAM to design Z-TCAM. They have designed two models of size 512×36 and 64×32.

These preferences and techniques help us to design a quality level design with efficient results. These emerging methods of modern designing improve our skills of designing and reduce the design effort.

III. REVERSIBLE ELEMENTS

Among the reversible and irreversible-logic gates, the using of irreversible gates always dissipates heat into the environment. But with the usage of reversible-logic gates we achieve zero heat dissipation ideally. A logic device is said to be reversible if it has equal number of inputs and outputs and that too have one to one mapping between them. The states of the input variants can be reconstructed from the states of output variants. This property assures logical reversibility as the inputs and outputs can be retrievable from each other uniquely.

The main theme of the reversible-logic synthesizing is to reduce the below mentioned parameters.

- Minimize the count of garbage outputs in the circuit.
- Reduce number of gates in the circuit.
- Minimize the additional inputs that are not required.
- Minimize the delays in the circuit.
- Reduce the circuit's quantum cost.

There are different kinds of reversible-logic gats like Toffoli Gate, Feynman Gate, Fredkin Gate, Peres Gate and some others. Among these Feynman Gate, Fredkin Gate and Peres Gate are used in the proposed design modules. A Brief discussion about these reversible gates as follows one by one. Each gate is having its special functionality used for designing the different modules required for the proposed scheme.

A. 2×2-Feynman gate:

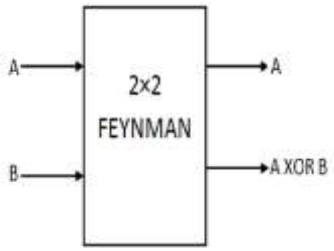

Fig. 3.1.1: 2×2-Feynman gate

The figure 3.1.1 shows the 2×2-Feynman gate with inputs 'A' and 'B' and outputs 'A' and 'A XOR B'. The Feynman Gate can used as XOR Gate as well as a NOT Gate. It is also used for copying its output to the next gate as it is a fan-out gate. It's quantum-cost is 1.

B. 3×3-Fredkin gate:

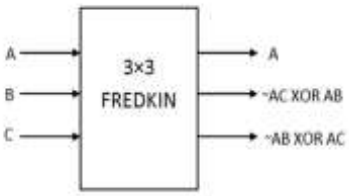

Fig. 3.1.2: 3×3-Fredkin gate

The figure 3.1.2 shows the 3×3-Fredkin gate with inputs 'A', 'B' and 'C' and outputs 'A', '~AC XOR AB' and '~AB XOR AC'. The Fredkin Gate can also be used as a selecting device for multiples with input 'A' as a select line. The quantum-cost is 5.

C. 3×3-PERES GATE:

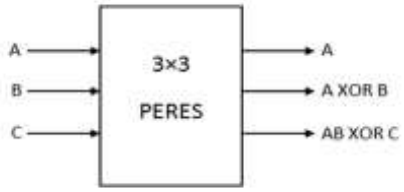

Fig. 3.1.3: 3×3-PERES GATE

The figure 3.1.3 shows the 3×3-PERES GATE with inputs 'A', 'B' and 'C' and outputs 'A', 'A XOR B' and 'AB XOR C'. The Peres Gate can be a match-line and be a search-line with Fredkin Gate. The quantum-cost is equals to 4.

D. Simple Sram Cell:

A simple SRAM cell can be constructed using two reversible-logic gates namely 3×3-Fredkin gate and 2×2-Feynman gate. The figure 3.2.1 shows the simple SRAM cell designed by using Fredkin and Feynman gate. This SRAM cell is used to store single bit value in TCAM cell. In the figure we can see the 'WL' input is a word-line which makes SRAM cell to operate either in hold state or read/write state. If WL=0, then it holds the previous value otherwise the operation mode is read or write. This design's quantum-cost is 6.

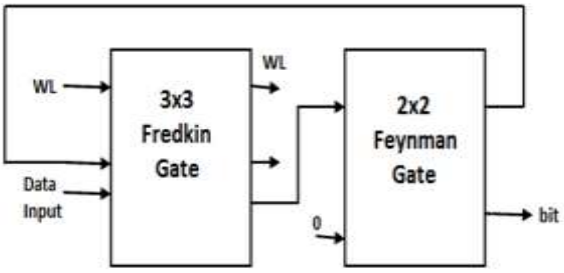

Fig. 3.2.1: Simple Sram Cell

E. Sram Cell Having Read/Write Signals:

The figure 3.2.2 shows SRAM cell included with read/write signals and along with the row decoder. The row decoder is most needed for SRAM array construction, as it enables or disables the entire row. This type cell stores single bits in TCAM memory cells.

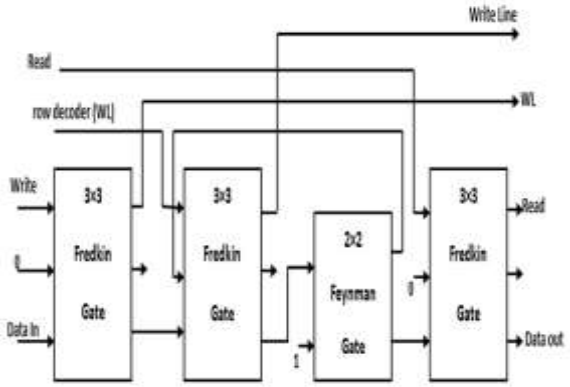

Fig. 3.2.2: Sram Cell Having Read/Write Signals

This design requires three Fredkin gates and one Feynman gate as shown in the figure which is having quantum-cost of 16.

IV. CONVENTIONAL METHOD

A. Designing a Tcam Cell:

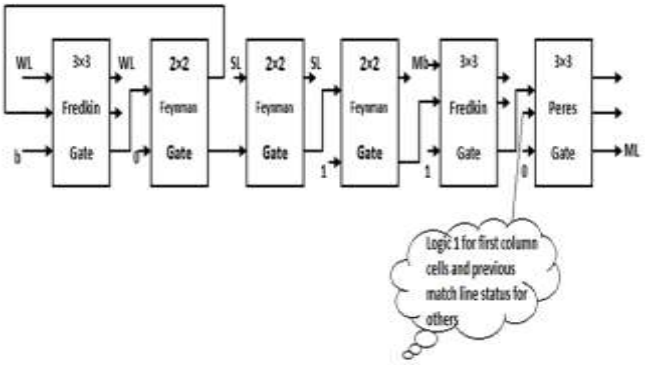

Fig. 4.1.1: A TCAM cell

The figure 4.1.1 shows a TCAM Cell which is built by using 2 Fredkin gates, 3 Feynman gates and 1 Peres gate. The quantum-cost of this cell is 17 and hence worst case delay is 17. The number of garbage outputs is 6 in this cell. This TCAM Cell is having two parts, first one is SRAM cell for storing data and a comparison circuit logic for comparing stored data with the search data. And also it is having a matching network for matching the contents.

The first two gates namely Fredkin gate and Feynman gate form a SRAM cell. The next two gates are Feynman gates among which first Feynman gate acts for XOR operation and the second Feynman gate acts for inverting operation. And the last two gates are Fredkin gate and Peres gate which are used in searching and matching operations. The inputs to this Fredkin gate are a 'match bit', logic '1' and the output from inverting Feynman gate. And for Peres gate the inputs are logic '0', logic '1' for the first column cells in TCAM array and output from the Fredkin-gate. The combine operation of these two gates gives the match line status either high or low depending upon the match-bit set. If the search data and stored data are matched then match line status is high otherwise it is low. And if in case the match-bit is set high then the match line status is always high independent of the inputs applied. Whatever the inputs applied it will not care or we can say wild care to the applied inputs. It means it shows the functionality of a Ternary CAM. By using this feature we exceed the functioning of binary CAM in searching criteria as TCAM cell having broader search capability with third don't care bit.

B. Tcam Cell Operation:

The functioning of an R-TCAM cell can be explained more clearly by referring the functioning table mentioned below. This table contains both search data bits and store data bits and also the match-bit for ternary operation of TCAM-cell. From the table we can see the match line status shows high bit whenever the search bit and store bit are matched. And it shows low bit when mismatching happens between the two type data bits. These two operations occur when match bit is low. Now see the cases where whenever the match-bit is high, then match line status always shows the high bit value irrespective of input values matched or mismatched. This shows the Ternary CAM cell functionality with the match-bit value.

Stored Data Bit	Search Data Bit	Match Bit Mb	Match-line State
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 4.1.1: Functional Table of TCAM cell

C. Overview of Conventional 4 × 3-Tcam Array:

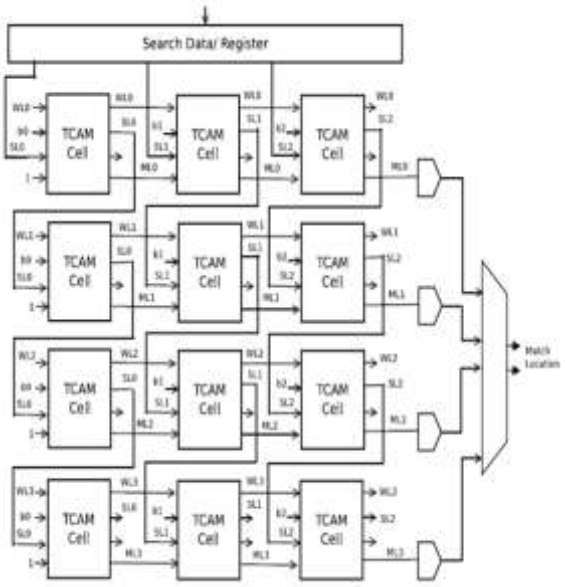

Fig. 4.2.1: Conventional 4 × 3-Tcam Array

The figure 4.2.1 shows the 4×3-TCAM array which is designed with incorporating 12 TCAM cells and a 4:2 encoder into it. This design is having quantum cost of 204 and hence worst case delay is also 204. The garbage outputs count in this design is 16. This design is used for searching and matching of 3 bits wide data. This TCAM array is having 4 rows and 3 columns. Each row cells are linked through a common-match-line and each column cells are linked through a common-search-line. The common-match-line is made either enable or disable depend upon the applied match bit. If the match line status in anyone of the TCAM cell is low then the status of common-match-line of entire row will be at low and if the match line status of all TCAM cells is high then the status of common match line of entire row will be at high. These two conditions still depend on the match-bit condition; if the match-bit is set high then the entire row status will be at high regardless of the applied inputs. The each common-search-line along the same column cells will be used to search the entire column cells data.

The 4×3-TCAM array can be designed using Verilog source code and synthesized using XLINX-ISE Tool. The figures 4.2.2, 4.2.3 and 4.2.4 show the RTL view of the block diagram, internal architecture and technological view of 4×3-TCAM array.

D. Extended 4 × 4 -Tcam Array:

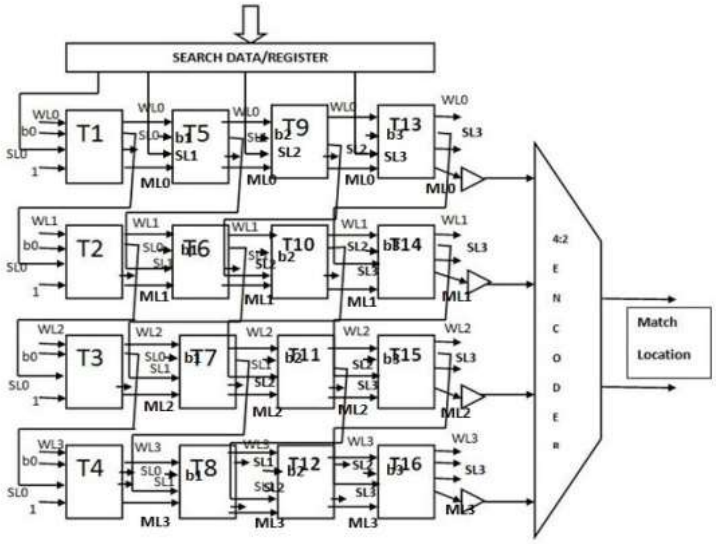

Fig. 4.3.1: Extended 4X4 TCAM Array

The extended 4x4 TCAM Array has been designed according to the conventional TCAM array, it has built with 16 individual TCAM cells and has the capability of searching and matching data upto 4 bit wide data.

This extended version also can be synthesized and simulated using the same procedure steps followed in the XLINX tool. The following are the two figures which show the top block and internal block of synthesized extended 4x4 TCAM array.

V. PROPOSED METHOD

A. Overview of Proposed 4×5-TCAM-ARRAY:

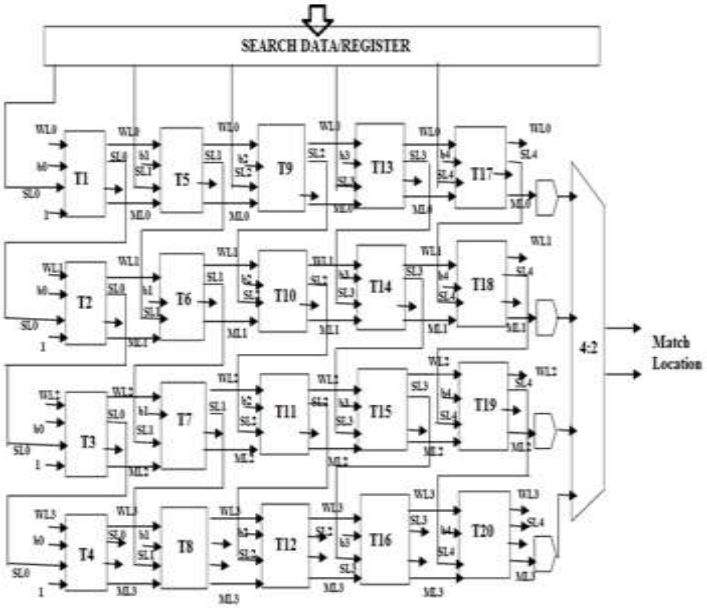

Fig. 5.1.1: Proposed 4×5-TCAM-ARRAY

The 4×5-TCAM array is as shown in figure 5.1.1, which is having the array of 20 TCAM cells and one 4:2 encoder. This design looks almost like the design of 4×3-TCAM array, only the difference in width of the search bits. This scheme helps us in searching and matching of 5 bits wide data. Again this final design is having 4 rows and 5 columns. Each of the four rows has a common-match-line and each of the five columns has a common-search-line. The TCAM cells arranged along the common matching line are stored with data bits with the help of SRAM cells. And the search bits are passed to column TCAM cells through common searching lines from the search-data registers. If any one of the same row cells having the match line status low then the status of the common-match-line of entire row becomes low. And if all the cells in the same row having the match-line status high then the status of the common-match-line of that entire row becomes high. The functioning of this proposed scheme is similar to the farmer method with broader searching capability.

The match line status also depends upon the match-bit 'Mb' applied that is considered as don't care bit. It helps in broader searching of data. Whenever the match-bit is high then the match line status becomes always high regardless of the applied inputs. At the end of the each row we get the match line status. It means four match line status at each row end and

these status signals are fed to a 4:2 encoder which selects among the four status lines of addresses and gives exact match line address at its output.

B. Operation of 4 ×5-Tcam-Array:

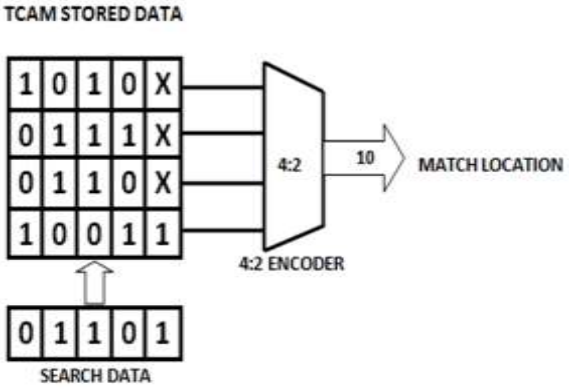

Fig. 5.2.1: Operation of 4 ×5-Tcam-Array

The operation of the proposed 4×5-TCAM-array can be easily understood through the figure 5.2.1. The TCAM cells in the four different rows contain stored bits. Each row stored with a predefined content value like 1010X, 0111X, 0110X and 10011 respectively. The search bits are sent from search data registers through the five column TCAM cells. Assume the search data here is 01101 which is compared with all row contents. The stored data also contains don't care bits at the end bit. Each bit of the search data is compared with each bit of column data. If both of the stored data bit and search bit matches then the particular TCAM cell shows its match line status as high. If mismatching happens then that particular TCAM cell shows match line status as low. If and only if all the bits of stored data and search data are matched then only the corresponding row line status becomes high. If a single TCAM cell in the same row shows low status then the entire row will be at low status.

The below mentioned four conditions show the operation of the TCAM cell. It makes us to find out the match line address where the search data is available and found by comparing and matching operations by TCAM cell.

- If first row gives match line status high then encoder output is '00'.
- If second row gives match line status high then encoder output is '01'.
- If third row gives match line status high then encoder output is '10'.
- If fourth row gives match line status high then encoder output is '11'.

Here in the given assumption the search data content matches to the third row stored data content, hence gives the output as '10' at the encoder output. The fifth bit in the stored content of third row is 'X' which is flexible to search for both logic '0' and logic '1'. Hence matches with the search data. This shows the ternary functionality of a CAM memory.

The entire hardware setup is shown in the figure 5.5.5 mentioned below. Here the left side part shows the DIP switches used for assigning input bits individually one bit value for each. Total 33 I/O pins are used in this implementation among which 31 input pins and 2 output pins. A datasheet of XC3S400 is used for proper pins assignment. The right side part indicates the LED lights to be blown for watching outputs. The green light on FPGA board blinks on only when the program is succeeded. The output shown in this image is processed by R-TCAM array to deliver the address value of "10".

Fig. 5.5.5: Complete Hardware Impedence Setup

VI. TESTING AND SIMULATION RESULTS

The simulation of the each module used in the proposed design and the simulation of the conventional as well as the proposed scheme are done by using the XLINX ISE 14.5 design suite. The designs can be verified and tested by giving different inputs and checking repeatedly for all type desired outputs.

Fig. 6.2.8: Simulation Waveform of Conventional 4*3 TCM array

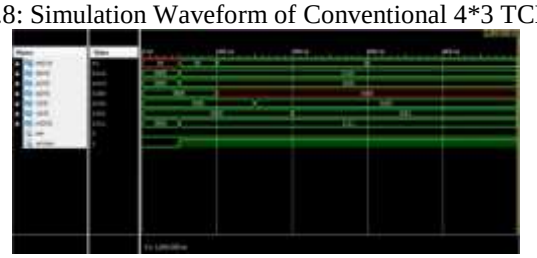

Figure 6.2.9: Simulation waveform of 4x4 TCAM array

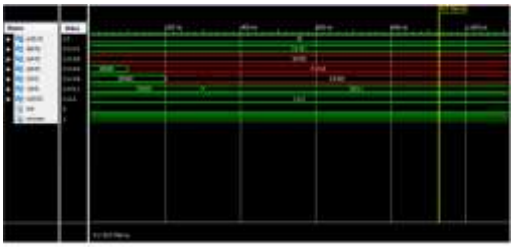

Fig. 6.2.9: Simulation waveform Proposed 4x5 TCAM array

The design constraints of all the reversible circuit designs are measured as the number of garbage outputs present in the design, which means the number of outputs unused in the circuit, and the another parameter is quantum cost of the design which means the cost of the design. The quantum cost directly depends on the number of 1×1 or 2×2 primitive gates or unitary gates that are used in the circuit design. And one more parameter related to timing constraint is the worst-case delay which is directly proportional to the unitary gates count in any design. Each unitary gate produces one delay unit processing time between its inputs and outputs. The proposed TCAM array holds totally 340 unitary gates in the array, hence The quantum-cost of this design is 340 and the worst case delay is also 340. And the number of unused outputs called as garbage outputs is equal to 24.

The optimization of these design factors will lead the design efficiency and reduces the power requirement. The avoidance of garbage outputs effects the reversible property but it is necessary to decrease its value when considered to the power parameter. It must to be kept in mind that, the number of gates to be reduced as much as possible which saves the design area, reduces delay units and hence cost.

VII. CONCLUSION & FUTURE WORK

The proposed work is a design of different sized TCAM arrays such as 4x3, 4x4 and 4x5 wide raged array using reversible-logic-entities. The 4x5 array can be helpful in matching and searching up to 5 bit wide length of data. The design comprises of four matching lines along row wise and five search lines along column wise. It allows us to search a 5 bit wide data among four 5 bit stored data. The functioning of this design is similar to the functionality of farmer TCAM array. And hence this design could be used in routing table for looking-up addresses, in high-speed networking instruments and switches.

This project work also included with the designs of a SRAM cell, TCAM cell and the farmer design of 4×3-TCAM array and extended 4x4 – TCAM array by using the reversible gate entities such as 2×2-Feynman gate, 3×3-Fredkin gate and 3×3-PERES GATE. The design also used one 4:2 Encoder for the selection of four match lines status as inputs and gives the single match line status as output. The entire designs are synthesized, verified and simulated by using the XLINX provided XST tool.

The future invention about the TCAM designs is to optimize the design using nanotechnology which may definitely optimize the design and increases the efficiency of the networking related equipments.

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