A New Implementation of Minimum Leakage with Improved Performance SRAM Architecture using CMOS VLSI Circuits

Saraswati M[1] Dr. K. Srinivasa Rao[2] Dr. D. Sreenivasa Rao[3]
[1]Associate Prof. & Head of Dept. [2]Professor & Principal [3]Professor
[1,2,3]Department of Electronics & Communication Engineering
[1]Govt. Engineering College Raichur, Karnataka [2]TRR College of Engineering, Hyderabad [3]JNTU, Hyderabad

Abstract— The growing demand for high integrity VLSI circuits, the leakage current in deep sub-micron CMOS technology is a major challenge. In deep submicron technologies, leakage power becomes a key parameter for a minimum leakage power design. Emerging battery-operated applications on one hand and shrinking technology of deep submicron on the other hand, leakage power dissipation is playing a significant role in the total power dissipation as threshold voltage scaled down. Due to the trade-off between power, area and performance, various efforts have been done. In this paper, our concentration is mainly based on minimizing the leakage power dissipation with improvement in the performance of the VLSI circuits. Here we proposed a Novel SRAM architecture called Low-Leakage, Improved-Performance (LLIP) SRAM. In this paper we designed the New SRAM architecture with newly proposed techniques and compare this one with other techniques. We observed that the total power consumption is reduced with improved performance. Here the total architecture is designed with 120nm technology.

Key words: SRAM, Deep Submicron Technology, Sub Threshold Leakage Power and LLIP_SRAM

I. INTRODUCTION

SRAMs strongly impact the over- all power, performance, stability and area requirements. In order to manage constrained trade-offs, they must be specially designed for target applications because the Static Random Access Memory (SRAM) is a critical component in the modern Digital Systems-on-Chip (SoCs) [1]. Rapid growth in semiconductor technology has led to shrinking of feature sizes of transistors using deep submicron (DSM) process. As MOS transistors enter deep submicron sizes, undesirable consequences regarding power consumption arise. Until recently, dynamic or switching power component dominated the total power dissipated by an IC. Voltage scaling is perhaps the most effective method to decrease dynamic power due to the square law dependency of digital circuit active power on the supply voltage.

As a result, this demands a reduction of threshold voltage to maintain performance. Low threshold voltage results in an exponential increase in the sub-threshold leakage current. On the other hand as technology scales down, shorter channel lengths result in increased sub-threshold leakage current through an off transistor. Therefore, in DSM process static or leakage power becomes a considerable proportion of the total power dissipation. For these reasons, static power consumption, i.e. leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies.

Here we present some VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power. In this paper we designed SRAM cell [2] with low power techniques with 120nm technology and compare with conventional SRAM cell.

SRAM is one of the most fundamental and vitally important memory cell. Because they are fast, robust, and easily manufactured in standard logic processes, they are nearly universally found on the same die with microcontrollers and microprocessors. Due to their higher speed SRAM based Cache memories and System-on-chips are commonly used. Due to device scaling there are several design challenges for Nano-meter SRAM design. Low power SRAM design is crucial since it takes a large fraction of total power and die area in high performance processors. A SRAM cell must meet the requirements for the operation in submicron/Nano ranges. The scaling of CMOS technology [3] has significant impacts on SRAM cell random fluctuation of electrical characteristics and substantial leakage current.

II. DIFFERENT APPROACHES AND SRAM CELL BASED ON CORRESPONDING APPROACH

This Section reviews the different leakage reduction techniques or approaches. In order to compare with the proposed approach, this section explains several previous leakage reduction approaches like base, sleep, stack and sleep keeper.

A. Base Approach

It is a traditional approach. Base approach is generally indicates conventional CMOS transistor or inverter. In the base approach pull-up network and pull-down network are used using few transistors. The pull-up network is called a P-MOS transistor and pull-down network is called as N-MOS transistor. This is shown in fig. 1a.

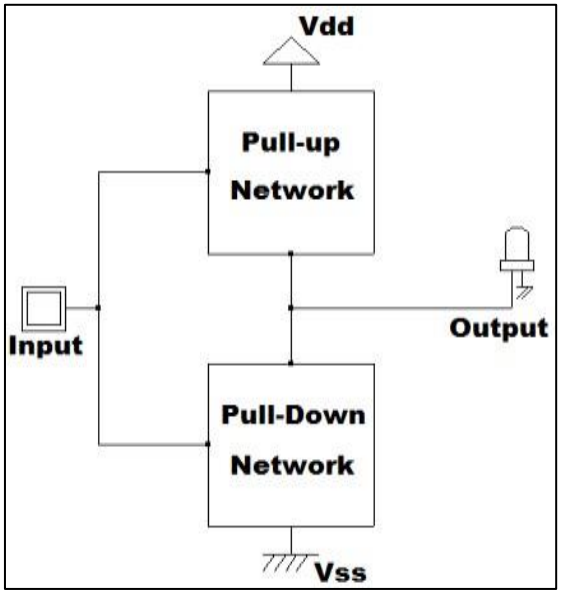

Fig. 1(a): Base Approach

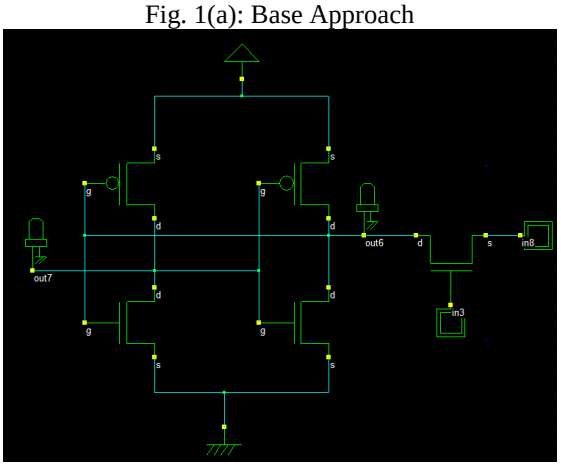

Fig. 1(b): Conventional SRAM Cell

Fig. 1b is a conventional schematic of Static Random Access Memory (SRAM) based on base approach.

It has 2 pull up PMOS and 2 NMOS pull down transistors as two cross coupled inverters and one NMOS access transistor to access the SRAM cell during Read and Write operations [4]. Both the bit lines (BL and BLB) are used to transfer the data during the read and write operations in a differential manner. To have better noise margin, the data signal and its inverse is provided to BL and BLb respectively. The data is stored as two stable states, at storing points VR and VL, and denoted as 0 and 1.

B. Sleep Approach

The most well-known traditional approach is the sleep approach [2][3]. In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between V_{dd} and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and Gnd.

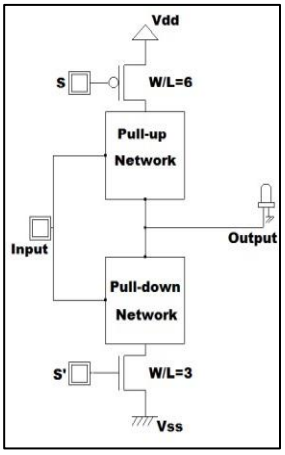

Fig. 2(a): Sleep Approach

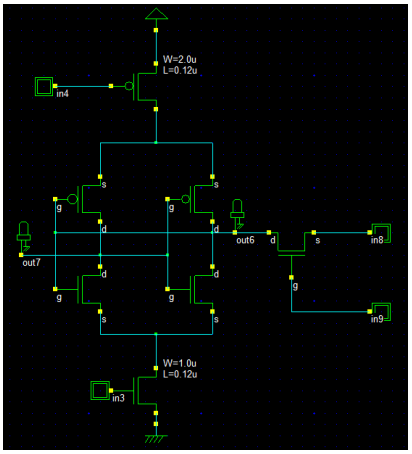

Fig. 2(b): Sleep Approach

Fig. 2b is shown as SRAM in Sleep approach [17].

C. Stack Approach

Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [5]. Fig. 4a. Shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach. The sleepy stack approach combines the sleep and stack approaches.

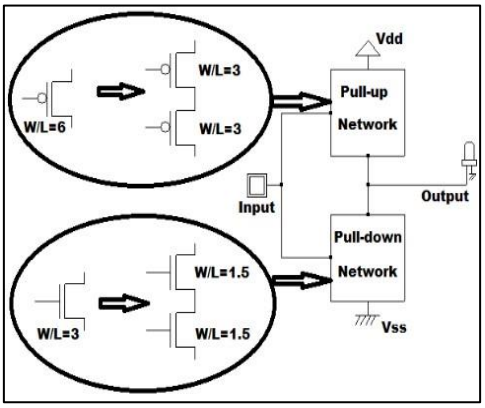

Fig. 4(a): Stack Approach

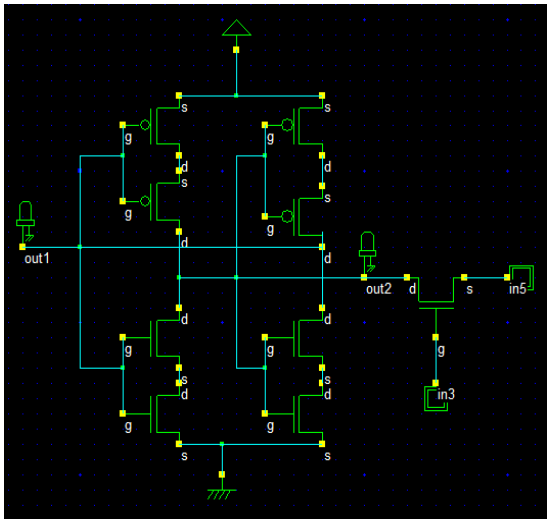

Fig. 4(b): Stack Approach

SRAM shown in Fig. 4b. Uses stack approach and thus reduce leakage current.

D. Sleepy Keeper Approach

The basic problem with traditional CMOS is that the transistors are used only in their most efficient, and naturally inverting, way: namely, PMOS transistors connect to V_{dd} and NMOS transistors connect to G_{nd}. It is well known that PMOS transistors are not efficient at passing logical zero level or Ground and NMOS transistors are not efficient at passing V_{dd} or logical high level. However, to maintain a value of "1" in sleep mode, given that the "1" value has already been calculated, the sleepy keeper approach uses this output value of "1" and an NMOS transistor connected to V_{dd} to maintain output value equal to "1" when in sleep mode. As shown in Figure 5a.

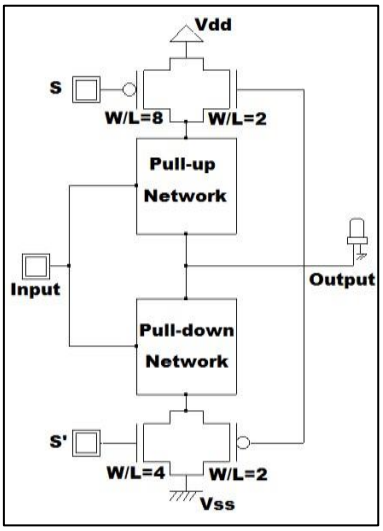

Fig. 5(a): Sleepy Keeper Approach

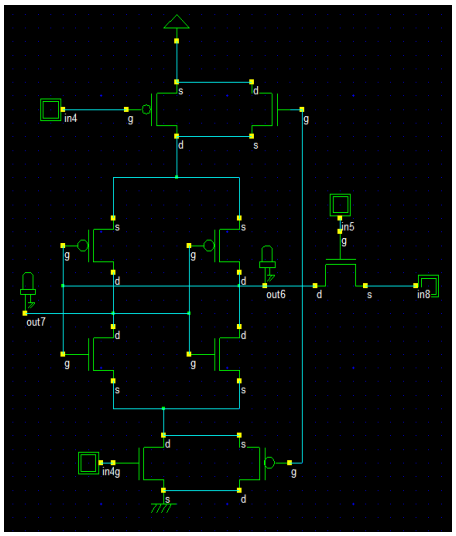

Fig. 5(b): Sleepy Keeper Approach

Fig. 5b shows the SRAM using sleepy keeper approach.

An additional single NMOS transistor placed in parallel to the pull-up sleep transistor connects V_{dd} to the pull-up network. When in sleep mode, this NMOS transistor is the only source of V_{dd} to the pull-up network since the sleep transistor is off. Similarly, to maintain a value of "0" in sleep mode, given that the "0" value has already been calculated, the sleepy keeper approach uses this output value of "0" and a PMOS transistor connected to G_{nd} to maintain output value equal to "0" when in sleep mode.

III. PROPOSED APPROACH: LLIP (LOW LEAKAGE IMPROVED PERFORMANCE)-SRAM CELL USING SLEEPY-KEEPER WITH STACK AND FEEDBACK APPROACH

In Proposed approach, we combined the techniques called stack approach and sleepy keeper approach with feedback to reduce the leakage power consumption in the circuit. Here we use two-two NMOS transistors in pull down network and two-two PMOS transistors in pull up network, so as to provide the stacking of the transistor for further leakage reduction. To maintain the proper logic level '1' we insert NMOS transistor parallel to PMOS transistor in pull up network, to connect sleep transistor to V_{dd} to the pull up network. In sleep mode, this NMOS transistor connects V_{dd} to the pull up network when sleep transistor cut off.

Similar action also repeat in pull down network the two-two NMOS transistors provide the stacking effect. To maintain the value '0' in sleep mode a PMOS transistor is connected in parallel with NMOS transistor. To maintain an output value to '0' PMOS transistor is connected to GND in sleep mode. For Proper Logic, NMOS is connected to V_{dd} and PMOS is connected to GND. The stacking of the transistor reduces the leakage power in proposed approach and enhances the performance of the circuit by maintaining proper logic of the circuit.

MICROWIND software is used for this approach to analyse the power dissipation at 120nm technology for a given power supply.

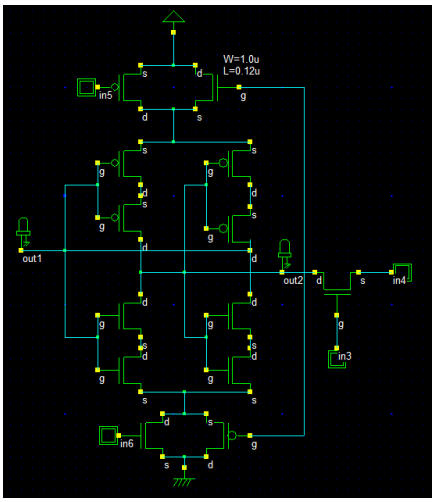

Fig. 6: Sleepy Keeper with Stack & feedback Approach

IV. SIMULATION RESULTS

A SRAM Cell is simulated with leakage power reduction techniques like sleep, forced stack, sleepy keeper and sleepy stack with DTCMOS. After analysing the results in terms of static power consumption, we conclude that proposed circuit with DTCMOS is producing comparatively better results. All schematics are designed and simulated using Microwind EDA tool for a SRAM Cell in different approaches using BSIM4 MOSFET model with 120nm technology. Performance characteristic such as static power dissipation is observed using conventional CMOS, Sleep, Stack, Sleepy keeper and sleepy stack techniques at a temperature of 27 ^{0}C and a Supply voltage, V_{DD} of 1.2V.

Table 1 shows all possible static input combinations for measuring static power dissipation in a SRAM Cell.

Static power dissipation was obtained by combining all possible static input combinations. The overall static power dissipation was calculated as the average of power dissipation in all possible static input combinations. In the case of Sleepy Keeper technique, Sleep and high V_{TH} transistors were turned OFF when the sleep signal was activated while they were turned ON when the sleep signal was deactivated. This static power was measured for 50 ns time interval.

Dynamic power dissipation was obtained by applying two dynamic clock inputs A and B of same frequency of 200 MHz and at a temperature of 27 ^{0}C. The supply voltage, V_{DD} was fixed at 1.2 V. In the case of Sleepy Keeper technique, sleep and high V_{TH} transistors were turned ON during the measurement of dynamic power dissipation. This power dissipation was also measured for 50 ns time interval.

Propagation delay of the logic gate was measured from the trigger input edge reaching 50 % of V_{DD} to the circuit output edge reaching 50 % of V_{DD}. Power delay product is measured to determine the efficiency of a circuit in terms of both power dissipation and propagation delay. Power delay product of a digital circuit is the product of its power dissipation and its propagation delay. Static and dynamic power delay products were obtained for the logic gate using various techniques.

Static input A	Static input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

Table 1: Static input combinations for measuring static power dissipation

Technique	Static Power dissipation (microwatts)
Base case SRAM Cell	2.268
Sleep Transistor based SRAM Cell	0.785
Forced stacking based SRAM Cell	2.216
Sleepy Keeper based SRAM Cell	1.017
Proposed SRAM Cell	2.335

Table 2: Comparison of Static Power of sleep, forced stack, sleepy keeper and sleepy stack & Proposed Circuit are shown.

Waveform to measure the static power dissipation using conventional CMOS and Stack techniques

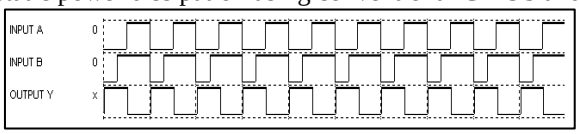

Fig. 7: Waveform

V. CONCLUSION

Performance characteristic such as static power dissipation of a SRAM Architecture is analyzed using various techniques. Performance characteristics of the logic gate were compared using conventional CMOS, Sleep, Stack, Sleepy keeper and sleepy stack techniques in 120nm technology.

In nanometer scale CMOS technology, sub-threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this paper, we present a new circuit structure named "stacking with sleepy keeper Approach with feedback" to tackle the leakage problem. The Stacking with sleepy keeper Approach with DTCMOS has a combined structure of four well-known low-leakage techniques, which are the forced stack, sleep transistor techniques, DTCMOS. However, unlike the forced stack technique & the sleepy Keeper over technique can utilize high-Vth transistors without incurring large delay overhead. Also, unlike the sleep transistor technique, the combination of stack approach with sleepy keeper approach retains exact logic state and mitigates leakage power. In future new approach of leakage reduction technique at gate level and block level are expected to give more power saving than the existing approach at CMOS circuit level design.

REFERENCES

[1] Sengupta D., Resve Saleh , "Generalized Power-Delay Metrics in Deep Submicron CMOS Designs", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 26, 183- 189, (2007).
[2] Chatterjee A., "An Investigation of the Impact of Technology Scaling on Power Wasted as Short-circuit Current in Low Voltage Static CMOS Circuits", Proceedings of the International Symposium on Low Power Electronics and Design, 145-150, (1996).
[3] Chandrakasan A., Bowhll W. J., Fox F., "Design of High-Performance Microprocessor Circuits", IEEE Press, (2001).
[4] Deepek subramanyan B.S., Nunez A., "Analysis of Subthreshold Leakage Reduction in CMOS Digital Circuits", Proceedings of the 13th NASA Symposium on VLSI Design, Post Falls, Idaho, USA, June 5-6, 1-8, (2007).
[5] M. Powell, S.H.Yang, B. Falsafi, K. Roy and T. N. Vijaykumar, "Gated-Vdd: A Circuit Techniqueto Reduce Leakage in Deep submicron Cache Memories," International Symposium on Low Power Electronics and Design, July 2000, pp. 90-95.
[6] Y. Taur, T.H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, New York, 1998.
[7] Z. Chen, M. Johnson, L. Wei and K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks," International Symposium on Low Power Electronics and Design, pp. 239-244, 1998.
[8] K.-S. Min, H. Kawaguchi and T. Sakurai, "Zigzag Super Cutoff CMOS (ZSCCMOS) Block Activation with Self-Adaptive Voltage Level Controller: An Alternative to Clock-gating Scheme in Leakage Dominant Era," IEEE International Solid-State Circuits Conference, pp. 400-401, 2003.
[9] Se Hun Kim, Vincent J. Mooney III, "Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design"
[10] K. Roy, S.Mukhopadhyay, H. Mahmoodi-meimand, "Leakage tolerant mechan- isms and leakage reduction techniques in deep-submicron CMOS circuits", Proceedings of the IEEE 91 (2003), pp. 305–327.
[11] Kawaguchi, H., Nose, K., and Sakurai, T. "A Super Cut-Off CMOS (SCCMOS) Scheme for 0.5-V Supply Voltage with Pico ampere Stand-By Current," IEEE Journal of Solid State Circuits vol.35, n.10, October 2000, pp.1498-1501.
[12] Park, J. C., and Mooney III, V. J. " Sleepy Stack Leakage Reduction," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on 14, Nov 2006, pp.1250-1263.
[13] Manish Kumar, Md. Anwar Hussain, Sajal K Paul. "Performance of a Two input NAND Gate using sub-threshold leakage control Techniques" Journal of Electronic Devices, Vol. 14, 2012 pp. 1161 -1169.
[14] Ankish Handa, Paanshul Dobriyal, Geetanjaliu Sharma, "A Novel High Performance Low power universal Gate implementation in subthreshold region," IJCA. Vol. 87, No. 12, February 2014.
[15] Ajay Kumar Dadoria, Kavita Khare, "A Novel Approach for Leakage power reduction Techniques in 65 nm Technologies," IJVLSICS, Vol. 5, No.3, June 2014.

[16] Hina Malviya, Sudha Nayar, C M Roy, "A New Approach for Leakage Power reduction Techniques in deep submicron Technologies in CMOS Circuit for VLSI Applications," IJARCSSE, Vol. 3, Issue 5, May 2013.
[17] Saraswati M, K Srinivasa Rao, D Srinivasa Rao, "A Novel Approach for Low leakage, High performance Universal Gate Implementation in Deep Submicron Regime Using subthreshold Leakage Control Techniques" IJERT, ICESMART-2015, pp. 379-384.
[18] Sonam Rathore, Vijay Yadav, Rita Jain, "A Brief Review of SRAM Architecture with Various Low leakage Power Reduction Technique in Recent CMOS Circuit" Volume 3, Issue I, January 2015.
[19] Atluri Jhansi Rani, K Harikishore, Fazal Noor Basha, V G Santhi Swaroop, VeeraRaju, "Designing and Analysis of 8 Bit SRAM Cell with Low Subthreshold Leakage Power" Vol. 2, Issue 3, May-June 2012, pp. 733-741.
[20] D Harihara Santosh, Lagudu Ramesh Naidu, "IP-SRAM Architecture at deep Submicron CMOS Technology – a Low Power Design" Vol. 2, Issue 8, Aug 2013, pp. 3554-3565.
[21] Petluru Venkata Ramasandeep, M. Vinay Kumar, "Design and Development of 4 Bit SRAM Architecture by using Static Power Reduction Techniques" Vol. 19, Issue 22, Sept 2015, pp. 2041-2050.
[22] V.G. Santhi Swaroop, B. Murali Krishna, M. Vijaya Bhaskar, B. Raghu kanth, V. Sai praveen, "Design of Low Power 8 Bit SRAM Architecture using Leakage feed back with Stack & Sleep Stack with Keeper" Vol. 2, Issue 2, March 2012, pp. 192-201.