Implementation of A XOR Based Vedic Multiplier for Area, Delay and Power Minimization

Shruthy Bastian.[1] Bency Varghese A.[2] Rachana M K.[3]
[1]Student [2,3]Assistant Professor
[1,2,3]Department of Electronics and Communication Engineering
[1,2,3]IES College of Engineering, Thrissur, India

Abstract— Nowadays, most widely used in different types of processors and other digital circuits are adders. In the VLSI design low power and area efficient high-speed circuits are most substantial area of research. One of the fast adders which has less area and reduced power consumption is Carry Select Adder. In this 32-bit carry select adder has been presented using modified XOR based full adder to reduce circuit complexity, area and delay. The modified full adder design needed only two XOR gates and one multiplexer. The modified 32-bit carry select adder gives better result than conventional carry select adder with respect to area, power consumption and delay. Using this modified 32 bit CSA a Vedic multiplier is developed. The software used is XILINIX ISE simulator. Implemented using VHDL module.

Keywords: Low Power, Area Efficient, XOR Based Adder, Carry Select Adder, Vedic Multiplier, VHDL

I. INTRODUCTION

Addition is the heart of computer arithmetic. It is very inevitable in processors and many other digital circuits. In digital adders, the speed of addition is having the limitation by the time required to propagate a carry through the adder. Design of area and high-speed data path logic systems are necessary areas of research in VLSI system design. Addition widens the overall performance of digital systems and arithmetic function. Multipliers and adders are used to execute various algorithms such as FFT, FIR, and IIR. Adders appear whenever the principle of multiplication is stated. Microprocessors, as we all know, execute millions of instructions per second. As a result, the most important constraint to remember when designing multipliers is the speed of operation. Because of device portability, device miniaturization should be high and power consumption should be low. Mobile phones, laptop computers, and other electronic devices necessitate a larger battery backup. As a result, a VLSI designer must optimize these three parameters in their design. These constraints are extremely difficult to meet, so a compromise between constraints must be made depending on demand or application.

Ripple carry adders have the smallest design but the slowest speed. Carry look ahead is the fastest, but it takes up more space. Carry select adders serve as a middle ground between the two adders. Instead of using dual ripple-carry adders, a carry-select adder can be implemented with a single ripple-carry adder and an add-one circuit. To reduce area while sacrificing speed, a multiplexer-based add-one circuit is proposed. Because of its small size and low power consumption, CSA is one of the fastest adders. In CSA, two multiplexed RCA operate in parallel, assuming carry in, Cin = 0, and carry out, Cin = 1, and the final sum is selected via multiplexer.

Full adders based on XOR, AND, and OR gates are used in conventional CSA. Because of the large number of transistors used in these gates, these adders take up more space on the chip, have a longer delay, and use more power.Adders are the fundamental components of any processor or data path application. Carry generation is the critical path in adder design. To reduce the power consumption of the data path, we must reduce the number of adder transistors. Carry Select Adder is a fast adder that is used in many data path applications. The CSA structure has the potential to reduce area, power, and delay. There is a reduction in power consumption, area, delay, gate count, and current when this method is used. The technique is used to implement a 32-bit CSA. Carry Select Adder (CSA) is the quickest adder among all others.

In this paper, an area-efficient Vedic multiplier is created by modifying the Carry Select Adder. Because multiplication is nothing more than a series of additions, the adder is a critical component in the design of a multiplier. One of the fastest adder structures is the carry select adder. In this case, a novel technique known as Vedic multiplier is used instead of standard multipliers such as add and shift multiplier, array multiplier, and so on. The multiplier in this case is based on an ancient Vedic multiplication technique. The purpose of this paper is to create an area-efficient Vedic multiplier using crosswise and vertical algorithms. Traditional CSLA designs are compared to the proposed design to demonstrate its efficiency.

II. RELATED WORK

1) K. Tejasvi et al. [1] designed a high efficiency carry select adder using the SQRT technique, which opens up many possibilities for increasing the speed and decreasing the area of any data processor. Only the Carry Select Adder (CSA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic operations. The structure of the CSLA indicates that there is room for improvement in terms of area and delay. In this thesis, we implemented a carry select adder for the computational process; these modules are written in VHDL.

   To reduce the area and delay of the CSA, this work employs a very simple and efficient gate-level modification. Based on this modification, an 8-, 16-, and 32-bit square-root CSA (SQRT CSA) architecture was developed and compared to the standard SQRT CSA architecture. When compared to the regular SQRT CSA, the proposed design has a smaller area and a slightly shorter delay. With logical effort, this work evaluates the performance of the proposed designs in parameters such as delay, area, and their products.

2) Due to P. Balasubramanian et al. [2], the addition forms the foundation of digital computer systems. This paper presents three novel gate level full adder designs based on the elements of a standard cell library: one with XNOR and multiplexer gates, another with XNOR, AND, Inverter, multiplexer, and complex gates, and a third with XOR, AND, and complex gates.
3) Uma et al. [3] proposed that adders are an almost mandatory component of any modern integrated circuit. The adder must be first and foremost fast, and secondarily efficient in terms of power consumption and chip area. This paper discusses the relevant options for selecting an adder topology with a tradeoff between delay, power consumption, and area. The ripple carry adder, carry look ahead adder, carry skip adder, carry select adder, carry increment adder, carry save adder, and carry bypass adder are the adder topologies used in this work.AC). Many other existing gate level full adder realizations have been compared.
4) G.R Gokhale et al.[4] compared conventional CSA designs such as Binary to Excess one Converter (BEC) based CSA and Modified CSA (MCSA) to the proposed CSA design to demonstrate its efficiency. It has improved in terms of area performance. This updated CSA is used to create the proposed Vedic multiplier. It takes up 6% less space than the Vedic multiplier using MCSA and 16% less space than the Vedic multiplier using BEC-based CSLA. The proposed design is also evaluated using the Booth multiplier.
5) For generating partial products, Anita jain et al.[5] a 16-bit multiplier was designed using Vedic Mathematics (Urdhva Tiryagbhyam sutra). The carry select addition technique is used to perform partial product addition in the Vedic multiplier. An 8-bit multiplier and carry select adders are used to create a 16-bit multiplier. We use the vertically and crosswise method of Vedic Mathematics when implementing the design. Verilog HDL is used to implement the design. The combinational path delay of a 16X16 bit Vedic multiplier employing a ripple carry adder is compared to that of a 16X16 bit Vedic multiplier employing a carry select adder outperformed the Booth multiplier.

III. ANALYSIS OF FULL ADDERS

Most digital circuits that perform addition or subtraction rely on a full adder circuit. It gets its name from the fact that it adds two binary digits plus a carry-in digit to produce a sum and a carry-out digit.

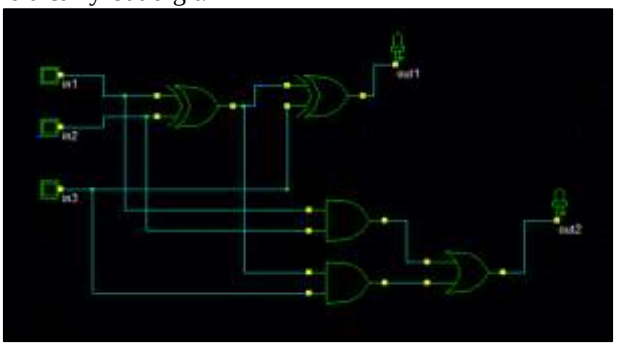


Fig. 3.1: Conventional 1bit Full Adder

As a result, it has three inputs and two outputs. So, a one-bit full adder adds three one-bit numbers A, B, and Cin, where A and B are operands and Cin is a bit carried in from a previous less-significant stage. Implementation of a standard full adder. A n-bit adder returns the result of addition with output carry while taking input carry into account. As a result, the one-bit full adder adds three one-bit numbers and the bit carried in from the previous less-significant stage.

The advantage of an XOR-based adder is that it requires fewer transistors. The main difference between conventional and XOR-based adders is that in XOR-based adders, other than two XOR gates, only one 2:1 MUX is used, which requires only 6 MOSFETs, whereas in conventional type adders, two AND gates and one OR gate are required, which requires at least 18 MOSFETs. At least 12 MOSFETs are saved in XOR-based 1-bit adders compared to conventional adders, resulting in less area and power consumption while also providing better delay performance.

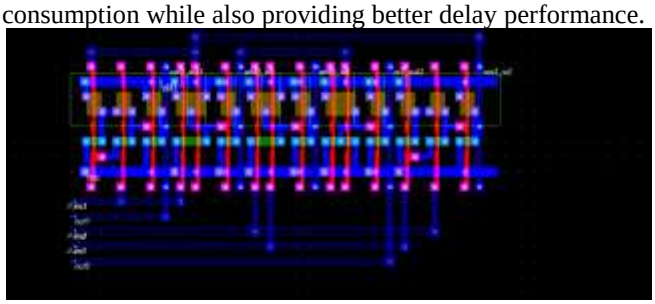


Fig. 3.2: Layout of Conventional 1bit Full Adder

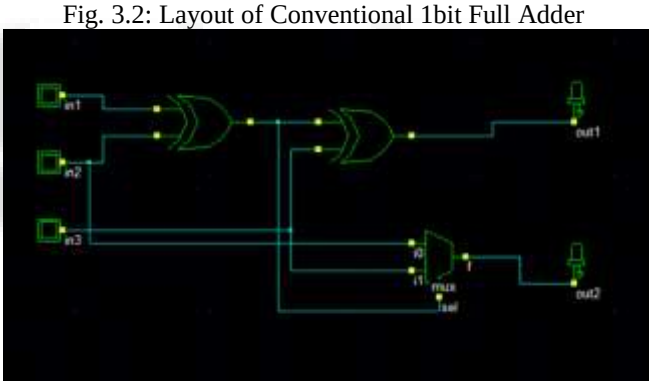


Fig. 3.3: XOR Based Full Adder

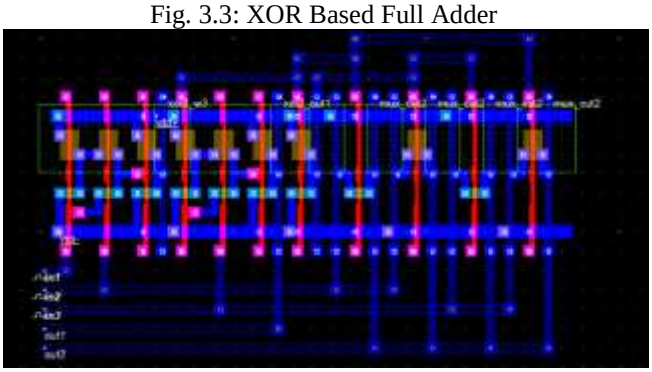


Fig. 3.4: Layout of XOR Based Full Adder

Predictive time required for the carry signal to propagate through the adder limits the speed of addition in digital adders. Two RCAs and a multiplexer are used to make up the CSA. The addition of two n-bit numbers with CSA is simply the addition of two numbers, the first with a zero input carry and the second with a one input carry. Following the calculation of the two results based on the correct carry-in, the correct sum and correct carry-out are selected, with the

multiplexer connected at the end to obtain the final output. The regular carry select adder (R-CSA) was developed to alleviate the problem of carry propagation delay by independently generating multiple carries.

IV. XOR BASED CARRY SELECT ADDER

Predictive time required for the carry signal to propagate through the adder limits the speed of addition in digital adders. Two RCAs and a multiplexer are used to make up the CSA. The addition of two n-bit numbers with CSA is simply the addition of two numbers, the first with a zero input carry and the second with a one input carry. Following the calculation of the two results based on the correct carry-in, the correct sum and correct carry-out are selected, with the multiplexer connected at the end to obtain the final output. The regular carry select adder (R-CSA) was developed to alleviate the problem of carry propagation delay by independently generating multiple carries.

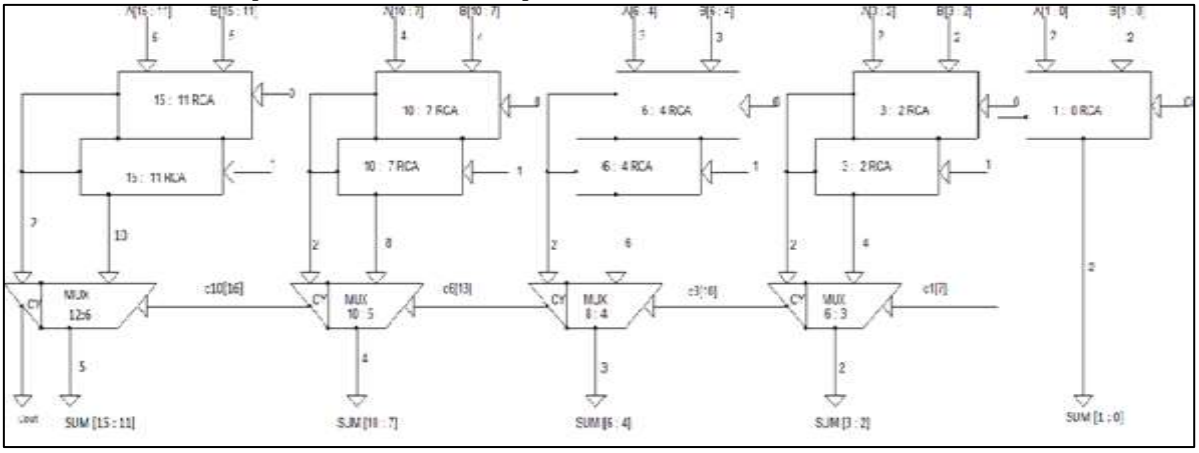


Fig. 4.1: Bit Carry Select Adder

The regular carry select adder (R-CSA) was created to address the issue of carry propagation delay by independently generating multiple carries and then selecting the correct sum and carry outputs based on the previous carry's value. An add-one circuit known as the Binary to Excess-1 Converter (BEC) circuit was introduced to create a low power consumption and area efficient CSA. This BEC circuit replaced the RCA with in =1 used in R-CSA because it used three fewer logic gates than bit RCA. M-CSA is made up of RCAs (for in =0), BEC circuits (for in =1), and multiplexers (MUX). One input to the MUX is added to the carry outputs from the RCA and another input.

V. VEDIC MULTIPLIER

This section shows how to use the Vedic multiplication technique "Urdhva Tiryagbhyam – Vertically and Crosswise." It works at a high speed because it generates partial products in parallel and then adds partial products simultaneously. High-speed data processing systems are becoming increasingly important. The Vedic multiplier satisfies this requirement without increasing power consumption. It is less complex than the Booth multiplier. The Vedic multiplier necessitates less hardware. As a result, the Vedic multiplier provides numerous benefits in terms of area, power, delay, and complexity. The following are the reasons for employing the Urdhva Tiryagbhyam Sutra in the implementation of the proposed Vedic multiplier: It has been discovered that the processing time obtained when a DSP is implemented using Urdhva Tiryagbhyam Sutra is less than the processing time obtained when the same DSP is implemented using Xilinix 14.7. The Urdhva Tiryagbhyam has a regular and parallel structure, making it simple to implement the multiplier designed using such a Sutra on a silicon chip. The parallel structure increases the multiplier's speed.

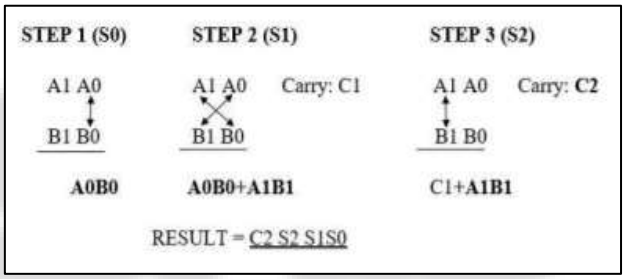
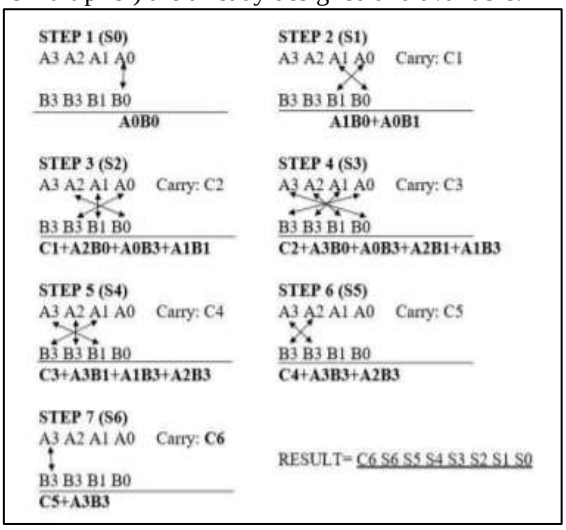


Fig. 5.1: 2x2 Multiplication

Another significant benefit of using this Sutra is that higher order multipliers (such as a 4X4 Vedic multiplier) can be easily designed if lower order multipliers (such as a 2X2 Vedic multiplier) are already designed and available.



Fig, 5.2: 4x4 Multiplication

This algorithm reduces the multiplication of two large bit numbers (say, two 8-bit numbers) to the multiplication of two small bit numbers, i.e., two 1-bit numbers.The preceding Sutra was traditionally used to

multiply two decimal numbers. This has been extended to the multiplication of two binary numbers in this case. Because the partial products are generated in parallel, the final product is obtained at a faster rate.

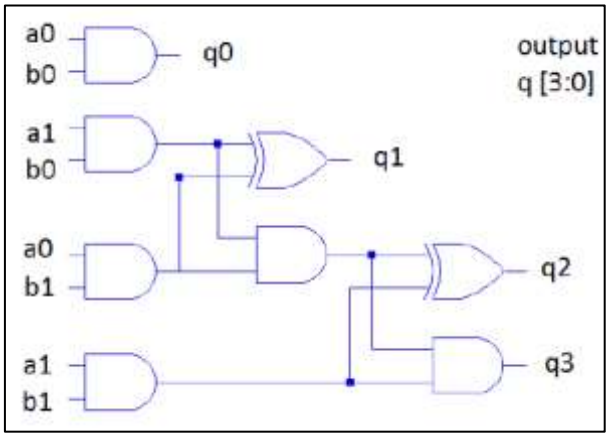


Fig. 5.3: 2x2 Vedic Multiplier

VI. RESULTS AND DISCUSSION

Every individual cell in the design contributes to the aggregate cell zone, and total power is the sum of leakage power, switching power, and static power. The power reduction for the 4-bit, 8-bit, and 16-bit XOR-based carry select adder circuits is 12.5 percent, 16.67 percent, and 20.04 percent, respectively. Similarly, the percentage reductions in area are 1.35 percent, 6.6 percent, and 9.41 percent, respectively. There is also a delay reduction of 0.8 percent, 1.3 percent, and 2.01 percent, respectively.

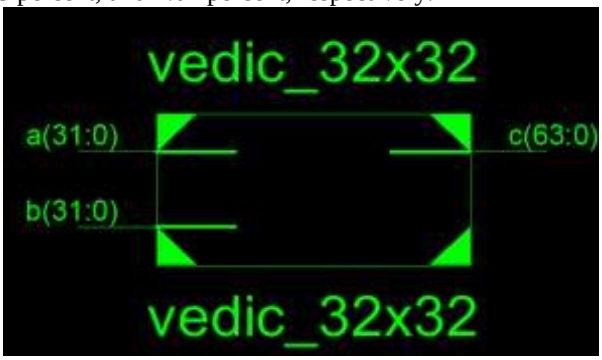


Fig. 6.1: RTL DIAGRAM

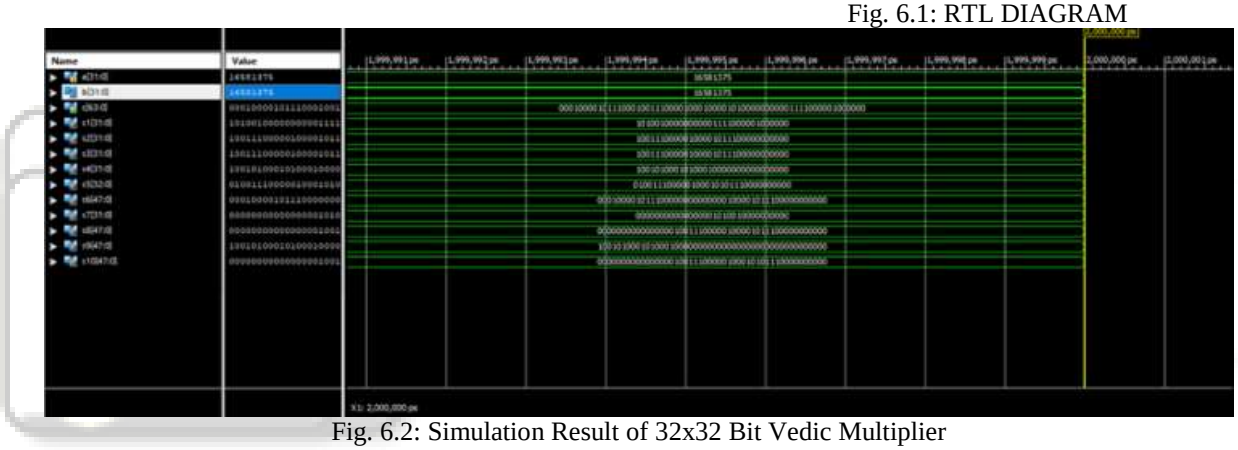


Fig. 6.2: Simulation Result of 32x32 Bit Vedic Multiplier

The RTL view and simulation result using modified xor based carry select diagram is depicted the most disadvantage of convention Vedic multiplier is its major utilization. Modified XOR based Vedic multiplier is the replacement for the issue. Comparison between the modified and conventional one is shown below.

32bit	XOR Based Vedic Multiplier	Conventional Vedic Multiplier
Delay	17.69	35.76
Number Of Slices	2% Utilization	36% Utilization
Number Of LUTS	2% Utilization	55% Utilization
Power Consumption	0.082	1.6

as the basic building block. According to the simulation results, an XOR-based 32-bit CSA consumes 20.40 percent less power, occupies 9.41 percent less space, and has a 2.01 percent shorter delay than a conventional CSA. The most significant disadvantage of the conventional al vedic multiplier is its extensive use of LUTs and slice registers; however, these issues are addressed.

ACKNOWLEDGMENT

I would like to convey my heartfelt gratitude towards my guide Ms. Rachana M K for her constant guidance, encouraging help and inspiring words. I am thankful to the department of Electronics and communication engineering for their support.

REFERENCES

[1] K. Tejasvi1 and G. S. Kishore, "Low-power and area-efficient N-bit carry select adder," International Advanced Research Journal in Science, Engineering and Technology, Vol. 3, Issue 7, pp. 186-189, July 2016.
[2] P. Balasubramanian, N. E. Mastorakis, "High speed gate level synchronous full adder designs," WSEAS Transactions on Circuits and Systems, Volume 8, Issue 2, pp. 290-300, February 2009.
[3] R. Uma, V. Vijayan, M. Mohanapriya and S. Paul, "Area, delay and power comparison of adder topologies," International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, pp. 153168, February 2012.

[4] G.R Gokhale and P. D. Bahirgonde "Design of Vedic-multiplier using area-efficient Carry Select Adder"International Conference on Advances in Computing, Communications and Informatics (ICACCI)
[5] Ankita Jain, Atush Jain "Implementation and Analysis of Vedic Multiplier Using Different Adder"IJournals: International Journal of Software & Hardware Research in EngineeringISSN-2347-4890 Volume 3 Issue 12 December, 2015

