A Comprehensive Introduction to Numerous MLI Topologies with Reduced Component Count

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Abstract— Multi level inverter is most commonly used in high power, high voltage application. Many topologies are invented for the use of multilevel inverter in drive application. In case of two level inverters, it needs high switching frequency to have a good quality output voltage due to which there are high switching losses. In order to overcome these losses the Multilevel inverter are invented. Although the conventional topologies have better performance efficiencies, but as we move towards higher voltage level the component count increases. Hence there has been an active interest in evolving new topologies. This paper presents a brief overview of such nine reduced component count topologies. There comparative analysis inters of component count is also presented comparing with conventional topologies.

Keywords: Multi Level Inverter (MLI), Neutral Point Clamped Inverter (NPCMLI), Flying Capacitor Inverter (FCMLI), Cascaded H Bridge Inverter (CHBMLI), Reduced Component Count (RCC)

I. INTRODUCTION

Multilevel inverter is most commonly used in high power, high voltage application. Many topologies are invented for the use of multilevel inverter in drive application. In case of two level inverters, it needs high switching frequency to have a good quality output voltage due to which there are high switching losses.

In order to overcome these losses the Multi level inverter are invented .A voltage level of three is assumed to be the smallest level number in multilevel converter. Initially and most commonly multilevel inverter application has been in traction, both locomotive and track side static converter. And recently they are used in VAR compensation and stability enhance emend, high voltage dc transmission, high voltage motor drive and also in medium voltage induction motor variable speed drive. In modern industrial application of multilevel inverter focuses on medium voltage motor drive, utility interface for renewable energy system, Flexible AC transmission system, and traction drive systems.

The concept of multilevel inverter was given in 1975 [1]. Separate DC full bridge cells are connected in series to obtain a staircase AC output voltage. The term multilevel started with three level converters [2]. And after that many level inverters have been invented as shown in figure 1. Diode clamped multilevel inverter which is also called Neutral point clamped inverter scheme was invented in 1981 [3]. Capacitor clamped inverter also Called flying capacitor type was invented in 1992. And in 1996 cascaded H bridge multilevel inverter was invented. Cascaded H Bridge is the combination of diode clamped and flying capacitor type inverter. Although the cascaded h bridge inverter was invented sometime earlier but its application became noticeable in mid 90's [4]. Cascaded H bridge multilevel inverter is very advantageous in motor drives and utility. It can be also used in regenerative type motor drive. The most recent multilevel inverter topologies are mixed multilevel inverter, hybrid multilevel inverter, and soft switched multilevel inverter. These inverters are helpful in enhancing rated inverter voltage and power if the voltage level is increase.

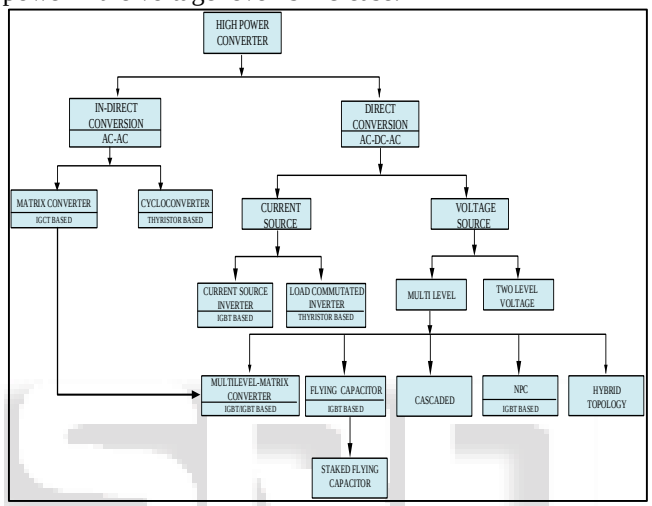

Fig. 1: Topologies of multilevel Inverters

Multilevel converters are able to switch either its input or output nodes (or both) between multiple (two or more than two) levels of voltage and current. As the number of levels approaches to maximum, the THD of the output voltage approaches zero. The number of the attainable voltage levels, however it is limited by several different factors some of which are voltage imbalance problem, voltage clamping requirements, circuit layout and packaging constraints complexity of the controller, and also because of maintenance costs.

But as the voltage level increases complication in circuit designing increases since as it increase the component requirement of the MLI. This may cause the overall system to be more expensive, bulky and complex. Consequently, for past few years, efforts are being directed to reduce the power switch count in MLIs and a large number of topologies have appeared in the literature [5-8]. These topologies have their own merits and demerits from the point of view of application requirements. As of now, no literature is available which comprehensively reviews the aforementioned topologies, thereby stipulating their comparative advantages and limitations. This paper aims at presenting a review of MLI topologies proposed with the exclusive objective of reducing the power switch count.

Table 1. Main features of the three topologies of multilevel inverter based reduced component count-mli (RCC-MLI)

Topologies which are proposed / presented with an exclusive claim of reducing the number of controlled switching power semiconductor devices for a given number of phase voltage levels are referred to as RCC-MLI topologies. In this paper nine such topologies [50-68] are reviewed which is shown in figure 2.

Merit of any given topology can be primarily judged based on the application for which it has to be employed. Still, in the context of this paper, the general criteria for an overall assessment of the merit of an RDC-MLI and its comparison with the other topologies can be:

1) The semiconductor switches count.
2) Total converter blocking voltage.
3) The controllability in terms of charge-balance control and appropriate distribution of switching frequencies.
4) Possibility of employing asymmetric sources/capacitor voltages.

While parameters (i) and (ii) affect reliability of the inverter, efficiency is influenced by parameters (i), (ii) and (iii) and application, performance and control complexity are governed by parameter (iii). A detail description of these topologies are presented in section III.

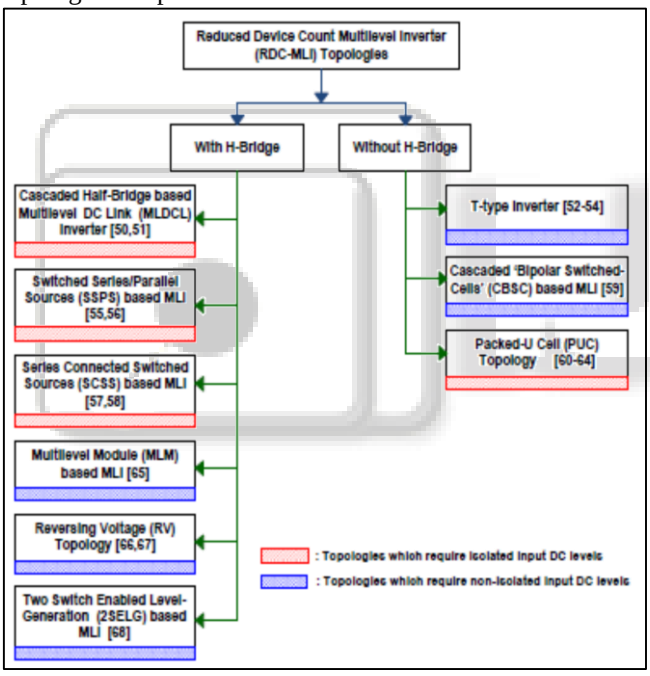

Fig. 2: Classification of RCC-MLI.

II. Review RCC-MLI

In this section, nine RDC-MLIs are reviewed and based on the parameters mentioned in section II B, topologies with reduced device count are discussed in this section.

A. Cascaded Half-Bridge based Multilevel DC Link (MLDCL) Inverter.

[50, 51] has presented a new multilevel inverter named as Cascaded Half-Bridge based Multilevel DC Link (MLDCL) Inverter as shown in figure 3. It comprises of cascaded half-bridge cells, with each cell having its own DC source. It has separate level-generation and polarity-generation.

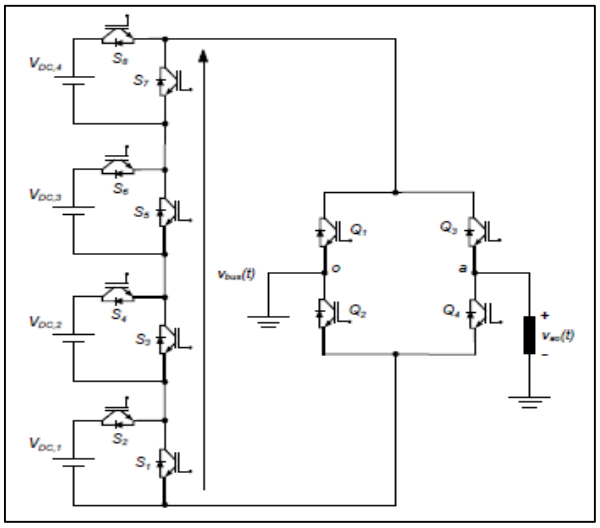

Fig. 3: Cascaded Half-Bridge based Multilevel DC Link (MLDCL)

B. T-type Inverter

T-type Inverter is proposed by [9,10] with the se of five-level single-phase inverter which results in a significant reduction in the number of power devices as compared to the conventional topologies as shown in figure 4.

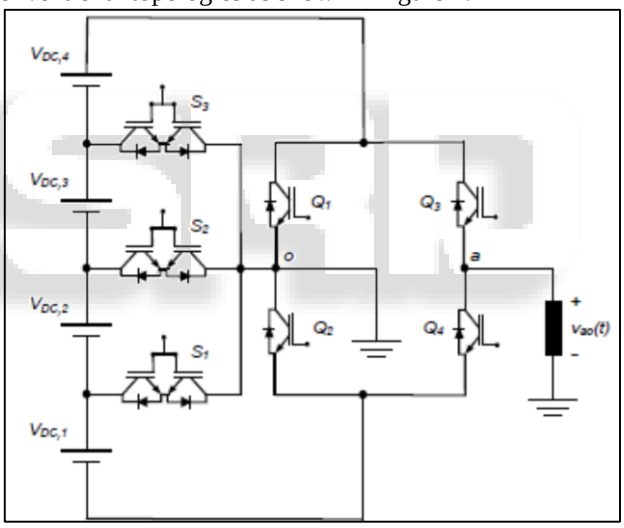

Fig. 4: T-type Inverter.

C. Switched Series/Parallel Sources (SSPS) based MLI

A single phase MLI has been proposed in [11, 12] with the combination of H-bridge and DC sources which can be switched in series and in parallel as shown in figure 5.

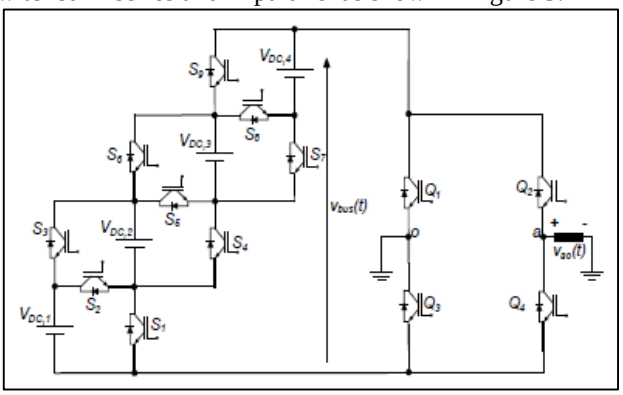

Fig. 5: Switched Series/Parallel Sources (SSPS) based MLI

D. Series Connected Switched Sources (SCSS) based MLI

In literature [13, 14] a topology is presented with sources connected in series through power switches. The low potential terminals of the sources are all connected through power switches while being also connected to the higher potential terminal as shown in figure 6.

E. Cascaded 'Bipolar Switched Cells' (CBSC) based MLI

A new class of MLI has been proposed by [15] having single-phase structure with four input voltage sources. The topology requires all the switches to be bidirectional-blocking-bidirectional-conducting in order to synthesize the required voltage levels at the output.

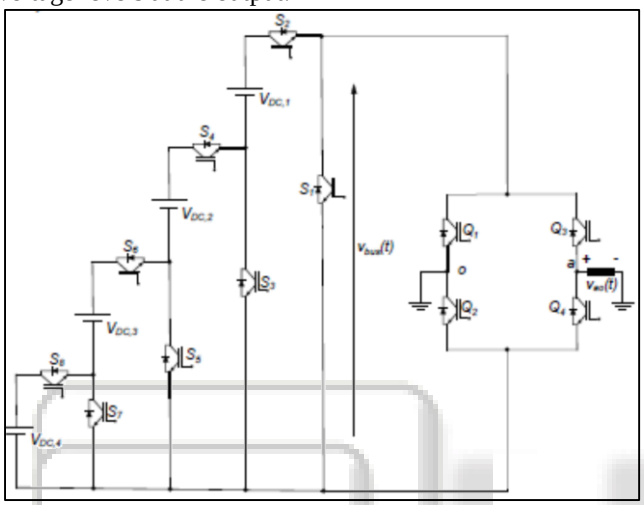

Fig. 6: Series Connected Switched Sources (SCSS) based MLI.

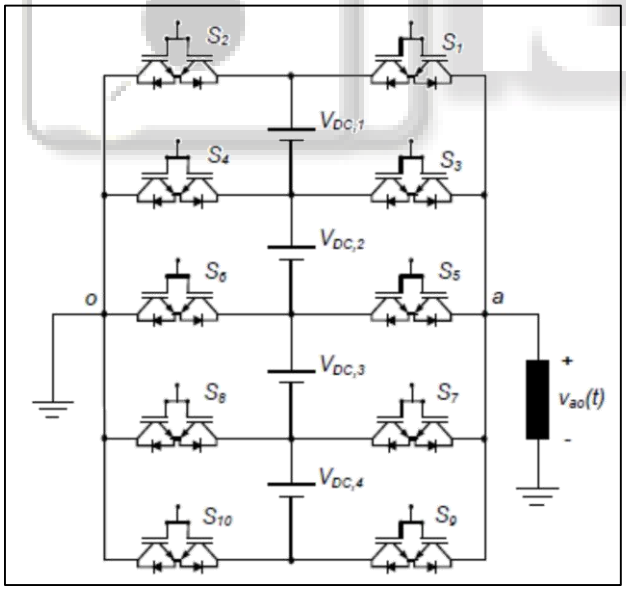

Fig. 7: Cascaded 'Bipolar Switched Cells' (CBSC) based MLI.

F. Packed U-Cell (PUC) Topology

The Packed U-Cell (PUC) Topology as proposed n [16-20] is very compatible as compared to conventional topologies. It is named so as consist of so-called packed U-cells as shown in figure 8. Each U-cell consists of an arrangement of two power switches and one DC input level. Authors claim that the topology offers high energy conversion quality using a small number of active and passive devices and consequently, has very low production cost.

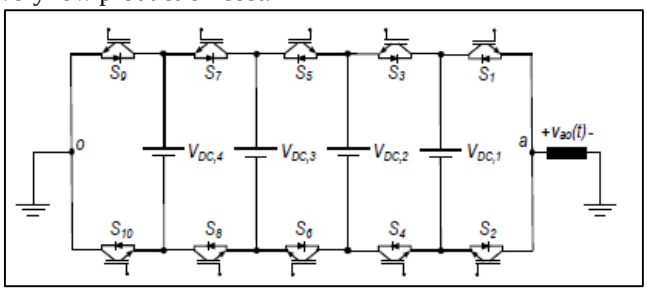

Fig. 8: Packed U-Cell (PUC) Topology

G. Multilevel Module (MLM) based MLI

In [21] a MLI topology is presented with separate level-generation and polarity-generation parts as shown in figure 9.

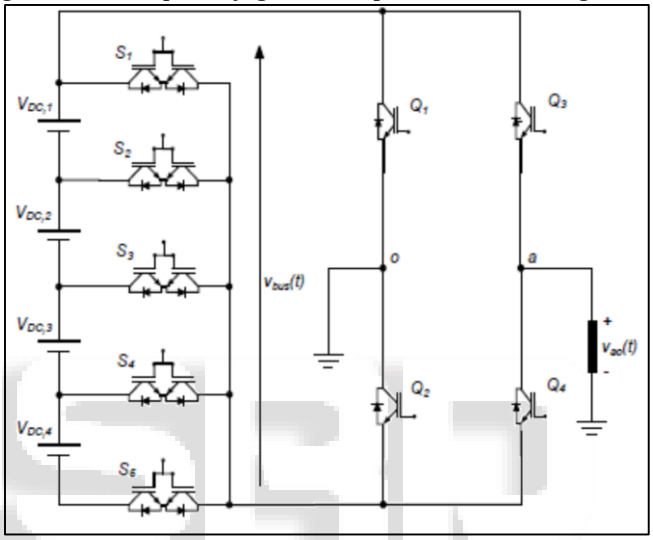

Fig. 9: Multilevel Module (MLM) based MLI

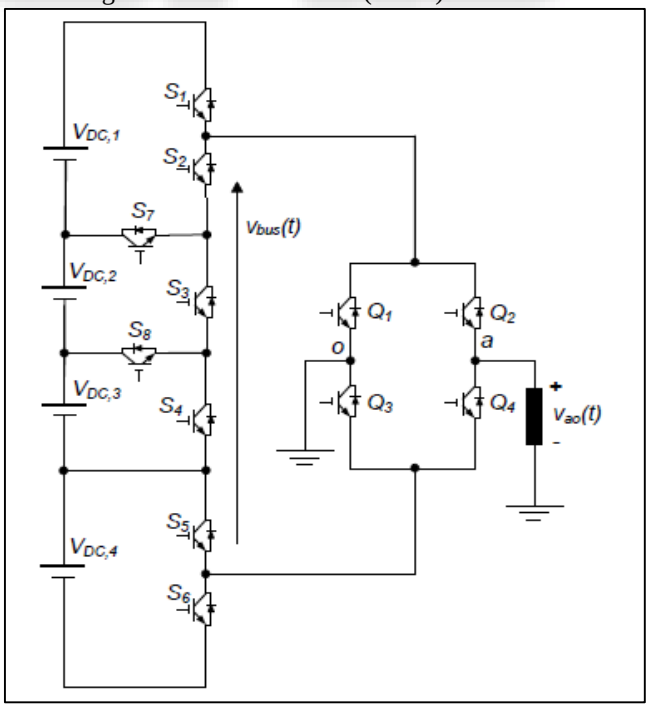

Fig. 10: Reversing Voltage (RV) Topology

H. Reversing Voltage (RV) Topology

In [22, 23] Najafi *et al.* have proposed reversing voltage MLI (RV-MLI) topology which separates the output voltage into two parts: level-generation and polarity- generation as shown in figure 10.

I. Two-Switch Enabled Level Generation (2SELG) based MLI

Paper [24] proposes this topology. The state-of-art of this topology is that the level-generation part requires only two conducting switches to synthesize any valid voltage level, irrespective of the number of input sources.

Therefore, this topology is referred to as „two-switch enabled level generation (2SELG) based MLI as shown in figure 11.

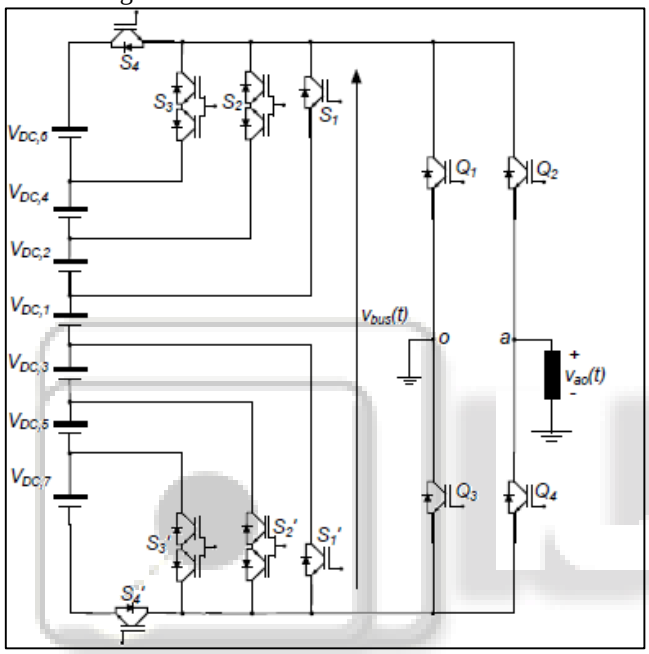

Fig. 11: Two-Switch Enabled Level Generation (2SELG) based MLI

The advantages of all the above mentioned RCC MLI topologies are briefly tabulated in table 1. The comparative analysis of all the above discussed RCC MLI in terms of component requirement is tabulated in table 2

III. Conclusion

The paper presents the comprehensive review on various RCC MLI topologies to improve the performance efficiency of MLI with reduced component requirement. In literature numerous techniques available which can be successfully implemented as RCC MLI a brief overview with circuit topologies its comparison and advantages are presented in this paper. Based on the review, it can be concluded that in the process of reducing the power switch count, various compromises are involved such as:

1) Increased rating of semiconductor switches in terms of voltage.
2) Additional bidirectional switches requires.
3) Increased sources.
4) Asymmetric input DC levels may be required.
5) Modularity loss.
6) Complex modulation / control schemes.
7) Difficulty in possibility of charge balance control.

Topology	Advantages
MLDCL-MLI	– Highly modular and simple – Requires only unidirectional switches – Equal load sharing is possible amongst symmetric input sources – Highest voltage rated switches can be operated at fundamental switching frequency.
T-type MLI	– Simple structure – Requires non-isolated input DC levels
SSPS-MLI	– Input DC sources can be combined in both series and parallel – Equal load sharing is possible amongst input DC sources – Binary source configuration can be employed
SCSS-MLI	– Simple structure – Highest voltage rated switches can be operated at fundamental switching frequency
CBSC-MLI	– Non-isolated input DC levels are required – All switches are bidirectional – Only two switches conduct simultaneously to synthesize a given voltage level
`PUC Topology	– Simple structure – Low losses
MLM-MLI	– Requires non-isolated DC sources – Simple structure – Highest voltage rated switches can be operated at fundamental frequency
RV Topology	– Requires non-isolated DC sources – Single DC link feeds all the three phases – Highest voltage rated switches can be operated at fundamental switching frequency
2SELG-MLI	– Requires non-isolated input DC levels – Low conduction losses

Table 1. Main advantages of RCC MLI

Topology	Number of Unidirectional Switches*	Number of Bidirectional Switches**	Total Blocking Voltage Requirement [p.u.]
NPC-MLI	$6(n_{levels}-1)$	0	$6[(n_{levels}-1)]$
FC-MLI	$6(n_{levels}-1)$	0	$6[(n_{levels}-1)]$
CHB-MLI	$6(n_{levels}-1)$	0	$6[(n_{levels}-1)]$
MLDCL-MLI	$3(n_{levels}+3)$	0	$9[(n_{levels}-1)]$

T-Type	12	$3(nl_{evels}$ - 1)	$3[2(nl_{evels}$ -1)+ $\sum_{K=1}^{(nlevels-3)/4}(n_{levels} - (2k+1))]$
SSPS-MLI	$\frac{3(3n_{levels} -}{2}$	0	$\frac{3(7n_{levels} - 13)}{2}$
SCSS-MLI	3(nlevels +3)		$3(3n_{levels}$-2) + $\sum_{K=1}^{(nlevels-3)/4}$ K
CBSC -MLI	0	3(nlevels +1)	$[\frac{(n_{levels}+1)(3n_{levels}}{8}$
MLM-MLI	12	$\frac{3(n_{levels} +}{2}$	$3[3(nl_{evels}$ -1)+ $\sum_{K=1}^{(nlevels-3)/4}(n_{levels} - (2k+1))]$
RV Topology	3(nlevels+ 3)	0	9(nlevels -1)
2SELG-MLI	24	$\frac{3(n_{levels} -}{2}$	$V_0 + 4n$; n = $\frac{(n_{levels}-1)}{2}$

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