Design of Receiver Continuous Time Linear Equalizer for High Gain
Mohini R. Deore¹ Prof. V. G. Raut²
¹,²Department of Electronics & Telecommunication Engineering
¹,²Sinhgad College of Engineering, Pune-411041, India

Abstract—This paper presents a design of continuous-time linear equalizer for 4 dB equalization at 1GHz frequency and for process corners the testing of MOSFET device is presented. One of the key components in the design of the digital SERIALIZER / DESRIALIZER circuit channels is the continuous time linear equalizer (CTLE), which compensates for the high frequency loss of electric channels. The objective is to design the continuous time linear equalizer circuit and to analyze the circuit performance. For the project all the circuits are being implemented in 45nm CMOS technology.

Keywords: CTLE, CMOS, CML, Desrializer, MOSFET, Serializer

I. INTRODUCTION
Modern chip-to-chip digital communications data rates are rising dramatically, increasing power consumption and imposing very tight constraints on connecting designers. In relation to the energy problem, owing to the restricted input / output (I / O) pins, occupied region and cost, high-speed electronic chip-to-chip communication devices utilize high-speed serial link transceivers. While enhancements in silicon technology facilitate the design of high-speed transceivers, unfortunately, the electrical channel bandwidth used for chip-to-chip communication has not progressed in the same way and usually has a low-pass frequency response. Thus, each frequency element experiences distinct losses for a broadband signal with a wide frequency spectrum by passing through the channel. This not only attenuates the sent bit, but also extends the bit skirt to the adjacent bits and creates inter-symbol interference (ISI). In order to continue to increase data rates, link designers implement hungry power and complicated equalizers to compensate the channel frequency-dependent loss[3]. It is possible to implement these equalizers in the transmitter or the receiver. The Continuous-Time Linear Equalizer (CTLE) is one of the most used equalizers that is implemented in the receiver. The CTLE's frequency response is essentially a continuous-time high-pass filter that amplifies the high-frequency signal component around Nyquist's transmitted signal frequency, as opposed to a low channel pass response. Thus, CTLE can effectively restrain pre-cursor and post-cursor and possibly suppress subsequent stage high-frequency noise. Unlike linear equalization, a DFE eliminates the ISI by taking the quantized previous input values and using the decision to correctly weigh the input signal. However, if noise is big enough to cause quantized output to be incorrect, a DFE has the ability to propagate error. Also, the DFE cannot cancel precursor ISI due to the feedback equalization structure. The closure of the feedback loop within a timing margin of 1 bit period or unit interval (UI) is one of the key design challenges in DFE implementation. A CTLE is therefore preferable if the requirements for error and power consumption in the serial communication system are severe.

This paper is organized as follows. Section II describes the proposed work. Implementation result is presented in section III. Finally conclusion is presented in Section IV.

II. PROPOSED WORK

Fig.1: Block Diagram Receiver CTLE

As, Fig 1 shows the block diagram of the receiver. The receiver includes CTLE for channel loss compensation. The gain is to be provided by the amplifier. CTLE being a CML structure is required to convert CML to CMOS. One of the main requirements of a current-mode logic circuit is that to maintain a constant current, the current bias transistor must remain in the saturation region. Then the signal was digitized and passed with a 50 percent duty cycle.

A. CTLE

The CTLE is a Continuous Time Linear Equalization. The channel basically acts as a low pass filter in Fig.2. This implies the magnitude of a signal's low frequency element will remain the same, but it will lessen the high frequencies. If we try to send a signal at 25GHz frequency, this signal will be greatly extenuated and it cannot be detected on the received end. In Figure 3, the CTLE's concept is to provide the receiver with a high pass filter to break down low frequencies and amplify greater frequencies.

Fig.2: Low Pass Filter Corresponding to the Channel

Fig.3: CTLE as High Pass Filter

Fig.4: Output Signal
As shown in Fig.4 We can restore our initial signal. The following bode diagram for this CTLE block can summarize this outcome, we can adjust three parameters. Let’s look at a CTLE’s bode diagram

![Bode Diagram](image)

Fig. 5: Transfer Function of a CTLE

First of all, we can adjust our CTLE zero. This parameter will determine where the gain starts in frequency. It will amplify components above this frequency. Also, we can set the poles representing the amplified frequencies. Finally, we can set our gain’s amplitude. This determines the ratio of our amplified components to one of the low frequencies. We must be careful not to attenuate excessively low frequency. In fact, if this happens, we won’t be able to distinguish between noise and the useful signal.

### B. Proposed CTLE Circuit

The idealized CTLE works by boosting the channel’s attenuated energy in frequency. The design goal is to compensate for the loss of the channel ISI to restore distortion of the waveform. In active CTLE, input amplifiers with RC degeneration can provide Nyquist frequency peak gain.

Figure 7 shows a generalized active CTLE topology. Due to the current in the circuit, the load resistors RL set the roll-off pole, Rs and Cs set the zero and the gm sets the peak. It can be concluded from CTLE’s knowledge that the value of gm is relatively greater to sustain large current and that RL is relatively smaller to set high frequency roll-off. The driving transistors are the M1 and M2 transistors in Fig.6. The Rs creates degeneration of the source. Cs sets the zero and RL offsets the gain.

![Active CTLE](image)

Fig. 6: Active CTLE

The parameters for given circuit is as follows [8].

The transfer function is given as

\[
H(s) = \frac{gm s + 1/RsCs}{Cs s + (1 + gmRs/2)/RsCs(s + 1/RpCs)}
\]

(1)

The first zero is at

\[
\omega_z = 1/RsCs
\]

(2)

The first pole is at

\[
\omega_1 = (1 + gmRs/2)/RsCs
\]

(3)

The role-off pole is at

\[
\omega_2 = 1/RpCs
\]

(4)

DC gain

\[
\omega_x = \frac{gmR_0}{1 + gmRs/2} \]

(5)

Ideal peak gain = gmR_0

(6)

\[
\text{Ideal Peaking} = \frac{\text{Ideal peak gain}}{\text{DC gain}} = 1 + gmRs/2
\]

(7)

### III. RESULTS

As CTLE is sensitive to PVT variations therefore the n-channel and p-channel transistors are simulated for various operating condition. The transistors are simulated separately in 45 nm CMOS technology; drain current is measured and presented in following table.

<table>
<thead>
<tr>
<th>Temp. /Corners</th>
<th>PMOS</th>
<th>NMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40°C</td>
<td>TT</td>
<td>FF</td>
</tr>
<tr>
<td>22.59 uA</td>
<td>uA</td>
<td>uA</td>
</tr>
<tr>
<td>27°C</td>
<td>TT</td>
<td>FF</td>
</tr>
<tr>
<td>22.59 uA</td>
<td>uA</td>
<td>uA</td>
</tr>
<tr>
<td>125°C</td>
<td>TT</td>
<td>FF</td>
</tr>
<tr>
<td>22.59 uA</td>
<td>uA</td>
<td>uA</td>
</tr>
</tbody>
</table>

Table 1: Process Corner Variation

As shown in table, the PMOS and NMOS transistor are simulated in different process corners like Typical(TT), Fast(FF), Slow(SS) using CMOS 45nm technology. MOSFET’s drain current differs with change in temperature and process corner. The value of drain current is high for fast process corner and less for slow process corner.

### IV. CONCLUSION

Receiver Continuous time linear equalizer (CTLE) circuit for 4 dB equalization at 1GHz frequency has been proposed. Transistors are ensured that they operate in saturation region only. The practical and theoretical values for all the parameters against process corners are verified and this is carried out with DC analysis. As CTLE is sensitive to PVT variations so from DC analysis it is found that process, voltage and temperature variation impacts on transistor drain current and other DC parameter values.

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REFERENCES


