# Development of Ultra Low Power VLSI Design using Various Low Power Design Techniques

**K. Shirisha[1] T. Sivaprasad[2]**
[1,2]Sr. Assistant Professor
[1]Aurora's Technological & Research Institute, Hyderabad, India
[2]AAR Mahaveer Engineering College, Hyderabad, India

*Abstract*— Leakage power plays a vital role in current CMOS technologies. As feature size shrinks leakage power also increasing. Power dissipation becomes as important consideration as performance and area for chip design in present days VLSI industry. International Technology Roadmap for Semiconductors (ITRS) forecasts that sub threshold leakage power dissipation may dominate the dynamic power dissipation. There are two types of power dissipations in CMOS technologies those are static power dissipation and Dynamic power Dissipation. This paper mainly concentrates on static power dissipation, in that mainly on leakage power. This paper reviews various low leakage power design techniques to achieve low power dissipation.

***Key words:*** Leakage Power, Power Dissipation, Low Power, CMOS Technologies

## I. INTRODUCTION

Area, Speed, Cost and Power dissipation are the major concerns when designing a VLSI system. Now a day's power dissipation became major concern for VLSI Engineers. Static power is defined as the power consumed by the device when it is in inactive mode and dynamic power is the power consumed when the device is in operation. CMOS circuits are designed theoretically to not consume any power in quiescent mode. In reality, all FETs leak current between the source and drain (if there is a voltage potential across the source & drain) even if the gate voltage is in the off position. This current is called sub threshold current and used to be insignificant.

However, as devices have become smaller and smaller and operating voltages have not scaled down with technology scaling (due to problems scaling the threshold voltage), this sub threshold voltage is becoming an increasingly important component of the total power of a chip. This becomes especially true in devices that have millions of these simultaneously leaky circuits, even if the device is not doing anything. As static power consumption has increased, it has become more important to consider techniques. The dynamic power is the power associated with switching. In any CMOS circuits, the output of the circuit is connected to a wire that is usually connected to the input of other circuits. This wire and inputs to other circuits can be modeled as capacitive loads to the circuit. When the circuit has to switch from a high voltage to a low voltage (or vice versa) then this capacitance has to be charged or discharged. This takes a certain amount of energy and if you repeat this billions of times every second, it becomes a continuous or AC power. In recent years, dynamic power was the only concern, as the technology feature size shrinks, static power, which was negligible before, becomes an issue as important as dynamic power.

## II. RELATED WORK

The main contributor to static power consumption of a CMOS circuit is subthreshold leakage and Gate –oxide leakage. Subthreshold leakage is source to drain current when gate voltage is smaller than the transistor threshold voltage. The subthreshold leakage current can be expressed as follows:

$$Isub = K1We^{-Vth/nV\theta}(1-e^{-V/N\theta}) \quad (1)$$

Where *Isub is* subthreshold leakage current, *K*1 and *n* are experimental values, *W* is transistor width, *Vth* is threshold voltage and $V\theta$ is the thermal voltage. Due to subthreshold current increases exponentially as the threshold voltage decreases, in deep submicron technology if threshold voltage is scale down, it will severely suffer from subthreshold leakage power consumption. In addition to subthreshold leakage, gate-oxide leakage power is also contributor to leakage power is due to the tunneling current through the gate-oxide insulator. As the technology decreases, gate-oxide thickness will be reduces, so deep sub-micron technology will also suffer from gate-oxide leakage power. However gate-oxide leakage is relatively small compared to subthreshold leakage. Although gate-oxide leakage will also increase exponentially when feature size decreases, a solution is developing high dielectric constant (*k*) gate insulators. In this paper, we focus mainly on to reduce the sub threshold leakage power.

## III. LOW LEAKAGE POWER TECHNIQUES

Techniques for leakage power reduction are of two categories: state-preserving techniques and state-destructive techniques. In state preserving technique the circuit present state is retained where as in state destructive technique the current Boolean output value of the circuit might be lost. A state-preserving technique has an advantage over a state destructive technique in that with a state-preserving technique the circuitry can resume operation at a point much later in time without having to somehow regenerate state. We will discuss various low leakage power reduction techniques to reduce leakage power. In order to do, first we shall have a glance on basic CMOS logic circuit. Figure -1 shows the Basic block diagram of Complementary Metal Oxide Semiconductor (CMOS) logic circuit. In this design approach, Pull up (PUP) network is designed using PMOS transistors and Pull down (PDN) network is designed using NMOS transistors. NMOS/PMOS are represented in series/parallel for sum and product term. NMOS is connected to ground and PMOS is connected to power supply.

 

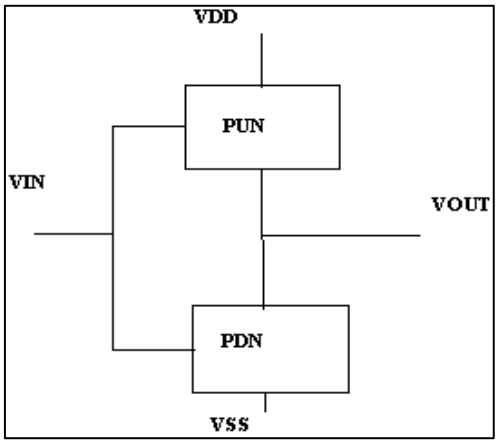


Fig. 1: Basic CMOS logic circuit

*A. Sleep Transistor Technique or Power Gating Technique*

This technique, also known as Multi-Threshold CMOS (MTCMOS) which reduces stand by or leakage power. Figure-2 shows the block diagram of sleep transistor technique. Two high threshold value sleep Transistors are used out of which one sleep transistor is placed between VDD and Pull up network and one more is placed between pull down network and GND. PMOS transistor is used in the pull down path and NMOS transistor is used in the pull up path as sleep transistors. During the active mode of operation both the sleep transistors are on, the sleep signal slp is held at logic 1 value and sleep bar (slpb) signal is held at logic 0 value. During the active period the two sleep transistors M3 and M4 are on. The node VG is at a higher potential than ground and the node VP is at a lower potential than VDD. The inverter circuit thus sees lower potential difference across nodes VP and VG. Thus the current though the circuit reduces and power dissipation comes down. During standby mode of operation signal slp is made logic 0 and the signal slpb is made logic 1. Transistor M3 and M4 are off and provide a very high impedance path between VDD and ground and leakage current is lowered. The power dissipation during this standby mode of operation is the lowest.

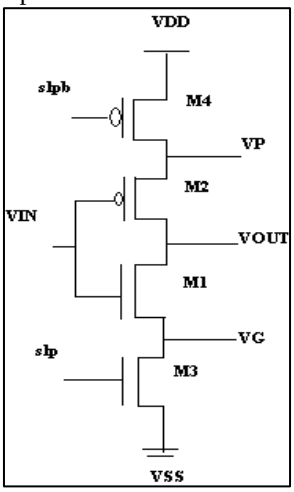


Fig. 2: Sleep Transistor Technique or Power Gating Technique

In this technique there is loss in the present state logic even though the power dissipation is lower, hence this technique is also termed as state destructive technique. In order to retain state a state retention transistor is connected in parallel to the sleepy transistors in the circuit of low leak sleepy inverter this technique is called State Retention Low Leak Inverter.

*B. State Retention Low Leak Inverter*

The sleep transistor technique though provides excellent low leakage power operation; it produces degraded output voltage levels during active mode of operation. The inverter output will not be at good logic levels. The main disadvantage of this technique is that during sleep (standby) mode of operation, the last output state is not retained. To resolve this issue, a state retention transistor is connected in parallel to the sleepy transistors shown in Figure-3. The state retention Inverter has four modes of operation.

*1) Active Mode:*

The sleep transistors M3, M4, M5 and M6 are ON by making slp=0 and slpb = 1.The circuit has good ground and VDD potentials and provides output voltage levels satisfactorily.

*2) Deep Sleep Mode*

The sleep transistors M3, M4, M5 and M6 are off by making slp=1 and slpb = 0. Due to this very high resistance path is formed between VDD and ground due the connection to ground and VDD is broken and the leakage current is thus lowered significantly.

*3) State Retention with Good Logic 1:*

By keeping sleep signals slp=0 and slpb = 0, the connection to ground is at VG and full VDD is provided. Low leakage current is obtained. The state retention takes place.

*4) State Retention with Ggood Logic 0:*

By keeping slp = 1 and slpb = 1, the connection to ground is complete and virtual VDD is provided. Leakage current is lowered due to one off transistor and the state retention takes place.

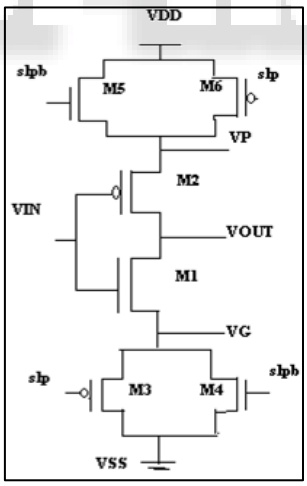


Fig. 3: State Retention Low Leak Inverter

*C. Transistor Gating Technique*

This is another one more technique to reduce leakage power. Here leakage current is reduced by inserting extra sleep transistors between power supply and ground. As shown in the figure - 4 PMOS sleep transistor (slp) is inserted in between PUN (pull-up network) and VOUT and an NMOS sleep transistor (slpb) is inserted in between the PDN (pull-down network) and ground.

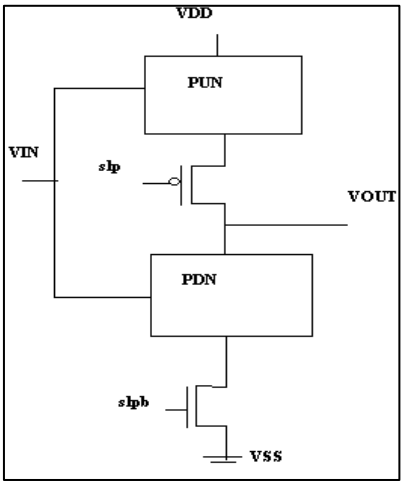


Fig. 4: Transistor Gating

*D. ZIGZAG Technique*

The Zigzag technique uses one sleep transistor in each logic stage either in the pull-up or pull-down network according a particular input pattern. Input vector can achieve the lowest possible leakage power consumption. Then, we either assign a sleep transistor to the pull-down network if the output is 1 or else assign a sleep transistor to the pull-up network if the output is 0. For below Figure-5, Let the output of the first stage is 1 and the output of the second stage is 0 when minimum leakage inputs are applied. So that, a pull-down sleep transistor is applied for the first stage and a pull-up sleep transistor is applied for the second stage. The zigzag technique is used to reduce the wake-up cost of the sleep transistor.

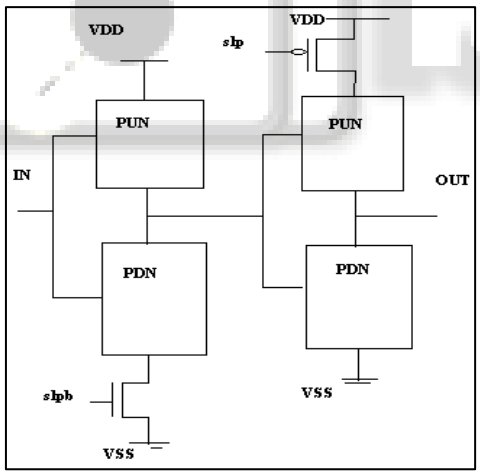


Fig. 5: Zig - Zag Technique

The zigzag technique reduces the wake-up overhead by choosing a particular circuit state and then turning off the pull-down network for each gate whose output is high while conversely turning off the pull-up network for each gate whose output is low. The zigzag technique can prevent floating by applying, prior to going to sleep, the particular input pattern chosen prior to chip fabrication,.

*E. Stack Technique*

This is another kind of technique for leakage power reduction called the stack Technique, in this technique existing transistor is broken in to into two half size transistors. Fig-6 shows its structure. When the two transistors are turned off together, reverse bias induces between the two transistors, so that sub threshold leakage current is reduced. However, due to size of the transistor is divided it increase delay and this drawback limits the usefulness of this technique.

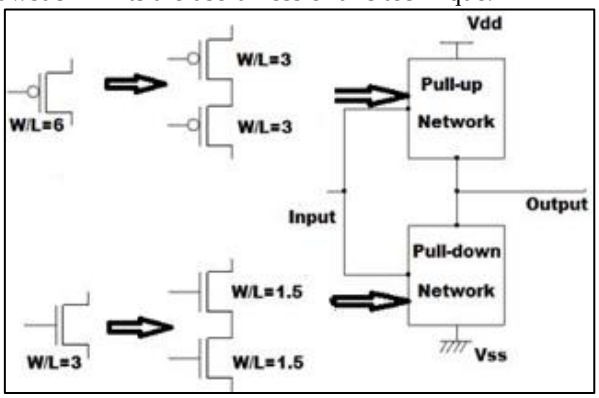


Fig. 6: Stack Technique

*F. Sleepy Keeper Approach*

In CMOS design style inversion is obtained when PMOS transistors connect to Vdd and NMOS transistors connect to Gnd. PMOS transistor has the disadvantage that it is not efficient at passing Gnd and similarly, NMOS transistors are not efficient at passing Vdd . However, to maintain a value of 1 in sleep mode, given that the 1 value has already been calculated, the sleepy keeper approach uses this output value of 1 and an NMOS transistor connected to Vdd to maintain output value equal to 1 when in sleep mode. As shown in Figure-7, an additional single NMOS transistor placed in parallel to the pull-up sleep transistor connects Vdd to the pull-up network. When in sleep mode, this NMOS transistor is the only source of Vdd to the pull-up network since the sleep transistor is off. Similarly, to maintain a value of 0 in sleep mode, given that the 0 value has already been calculated, the sleepy keeper approach uses this output value of 0 and a PMOS transistor connected to Gnd to maintain output value equal to 0, when in sleep mode.

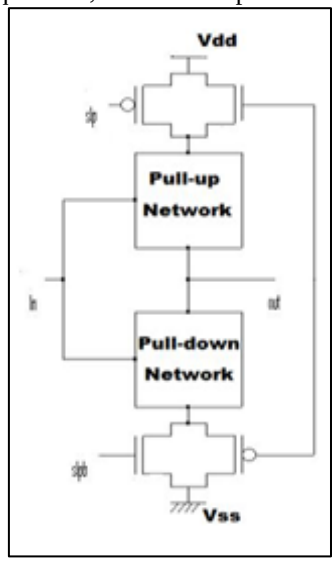


Fig. 7: Sleepy Keeper Technique

*G. Sleepy Stack*

This technique is combination of sleep transistor approach during active mode with stack approach during sleep mode

 

shown in Figure-8. Sleepy stack technique divides existing transistors in to two transistors each with half W/L of original transistor. Then sleep transistors are added in parallel to one of the transistors in each set of two stacked transistors. The divided transistors reduce leakage power using stack effect while retaining state. The added sleep transistors operate in similar to the sleep transistors used in sleep technique in which sleep transistors are turned on during active mode and turned off during sleep mode

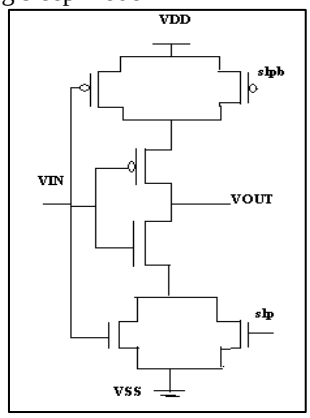


Fig. 8: Sleepy Stack

### *H. Zig-Zag Sleepy Keeper Approach*

Zig- Zag sleepy keeper is shown in Figure-9. Zig-zag keeper incorporates the traditional zigzag approach and sleepy keeper approach which use the sleep transistor plus two additional transistors driven by already calculated output – which retain the state of the circuit during the sleep mode while maintaining the state or state retention. Therefore, zigzag with keeper technique can achieve ultra-low leakage power consumption while saving state.

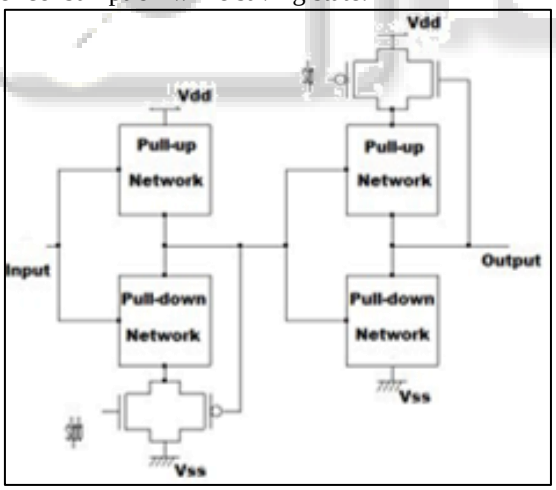


Fig. 9: Zig-zag Sleepy Keeper

In basic CMOS logic no direct path occur from power rail to ground because it is a inverter as Vdd is connected to PMOS transistor and NMOS transistor is connected to GND and if the VIN = 0, then VOUT =1 means PMOS transistor is turned on and NMOS transistor is turned off similarly if the VIN =1, then VOUT= 0 means PMOS transistor is turned off and NMOS transistor is turned on. However, it has to maintain a value 1 in sleep mode. A variation of the sleep approach, i.e the zigzag approach reduces wake up caused by sleep transistor. Sleep transistor is added in basic CMOS approach according to given logic value. It may be logic 0 or 1 value at the input of basic CMOS approach. If the input =0 then output =1. In this case PMOS transistor (PUN) is turned on and NMOS transistor (PDN) is turned off, so the (slpb) sleep NMOS transistor always add in turnoff side means connect between PDN(pull-down network) and ground of the first chain inverter but maintaining a value 1 in sleep mode, additional PMOS transistor is added to parallel with (slpb) sleep NMOS transistor..For the second chain inverter if the input = 1 then output = 0. In this case PMOS transistor (PUN) is turned off and NMOS transistor (PDN) is turned on so the sleep(slp) PMOS transistor always added in turn off side means connect between VDD and PUN but maintaining a value 0 in sleep mode, additional NMOS transistor is added to parallel with (slp) sleep PMOS transistor. During the active mode (slp=0 and slpb=1), the sleep transistors are turned on so it is reducing delay and during the sleep mode (slp=1 and slpb=0), the sleep transistor are turned off so it is saved state

## IV. CONCLUSION

It has become a challenge for the designers to maintain the power consumption in the tolerable limits without affecting other parameters like area and delay due to the shrinking in the technology feature size. In this paper, review of some of the low power design techniques is presented. Each of the discussed technique has its own advantages and disadvantages. It is choice of the designers to select the one that best suits to their requirement and design criteria.

## REFERENCES

[1] N. S. Kim et al., "Leakage Current: Moore's Law Meets Static Power," IEEE Computer, Vol. 36, Issue 12, pp. 68-75, December 2003.
[2] De and S. Borkar, "Technology and design challenges for low power and high performance," in Proc. Int. Symp. Low Power Electronics and Design , 1999, pp. 163–168.[2] K. Roy and S. C. Prasad, low Power CMOS VLSI Circuit Design. New York: Wiley, 2000, ch. 5, pp. 214–219.
[3] International Technology Roadmap for Semiconductors by Semiconductor Industry Association, http:// public.it rs.net, 2002.
[4] P. Pfeiffenberger, J. Park and V. Mooney, "Some Layouts Using the Sleepy Stack App roach," Technical Report GIT-CC-04-05, Georgia Institute of Technology, June 2004. http://www.cc.gatech.edu/techreports / index .04. html
[5] K.-S. Min, H. Kawaguchi and T. Sakurai, "Zigzag Super Cut-off CMOS (ZSCCMOS) Block Activation with Self-Adaptive Voltage Level Controller: An Alternative to Clock-gating Scheme in Leakage Dominant Era," IEEE International Solid-State Circuits Conference, Vol. 1, pp. 400-401, February 2003.
[6] Jun Cheol Park, Vincent J. Mooney III, and Philipp Pfeiffenberger, " Sleepy Stack Reduction of Leakage Power" Center for Research on Embedded Systems and Technology School of Electrical and Computer Engineering, Georgia Institute of Technology Atlanta, GA 30332-0250 USA

 