Design of 5T SRAM Cell with Low Leakage Current using VLSI Technology

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Abstract— A new single-port five-transistor (5T) Static Random Access Memory (SRAM) cell with integrated read/write assist is proposed. Amongst the assist circuitry, a voltage control circuit is coupled to the sources corresponding to driver transistors of each row memory cells. This configuration is aimed to control the source voltages of driver transistors under different operating modes. Specifically, during a write operation, by means of sizing the driver transistor close to bit line to resolve the write '1' issue. In addition, associated with a two-stage reading mechanism to increase the reading speed and to avoid unnecessary power consumption. Finally, with the standby start-up circuit design, the cell can switch to the standby mode quickly, thereby reduce leakage current in standby.

Key words: SRAM, VLSI Technology, CMOS Technology

I. INTRODUCTION

Recently, with the digitalization of electronic equipment, semiconductor memories have been used as essential components among various kinds of technical fields. SRAM requires no refreshing and will maintain its information as long as it has sufficient power supplied. This is due to the fact that the SRAM cell includes flip-flop circuitry internally that does not require refreshing. However, it is apparent that SRAM suffers from the disadvantage of relying on too many transistors. Accordingly, there is an important need to have an SRAM cell that requires fewer than six transistors. An SRAM cell has three modes of operation, namely read, write and standby.

Memories take up 80% of the die area in high performance processors. Therefore, there is a crucial need for a low leakage and highly robust SRAM design. Leakage current from a memory cell can cause unnecessary power consumption, especially during a standby mode. Recent research has shown that the leakage current will become even greater than the dynamic current in the overall power consumption. As CMOS technology scales down to 90 nm and below, the power consumption caused by leakage currents is becoming a significant part of the global power consumption. Therefore, it would clearly be desirable to provide a design for an SRAM cell that has less leakage current than traditional designs when the cell in standby.

A. Aim of Project

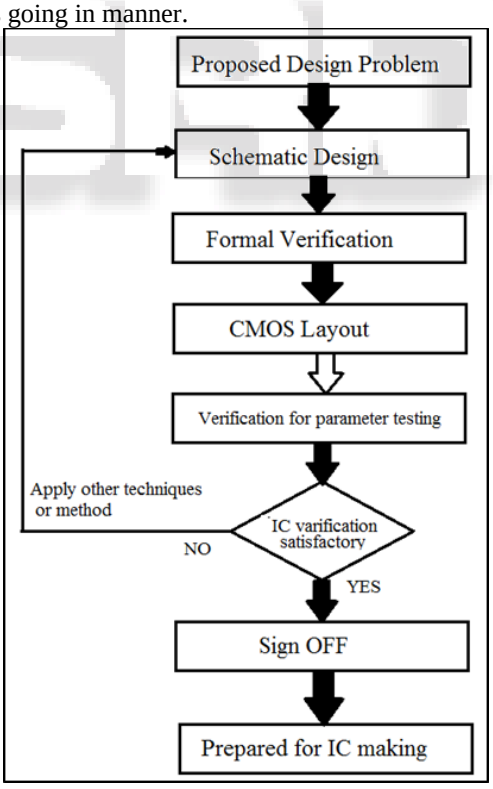
Hence to have very low power consumption, this research work is decided to implement CMOS technology. This paper focuses on minimizing the Power consumption during Write and Standby operations and delay during Write in a 5T-SRAM cell by using a new proposed the proposed research is aimed to achieve the high speed, low power consumption with 5T SRAM. Power has become one of the most important paradigms of design convergence for high density and low leakage current based on CMOS technology architectural design in 32 nm technology and comparing the results with the architectural designs being used nowadays. As microprocessors and other electronics applications get faster and faster, the need for large quantities of data at very high speeds increases.

B. Design Methodology

The keywords use for this design is Content Addressable Memory (SRAM), memory-resistor based (SRAM), memory-resistor based MOS hybrid architecture, modeling. Every step of design follows the design flow of Microwind 3.1 software. The design methodology will be according to VLSI backend design flow. The main target is to design and analyze the hybrid architecture of SRAM cell for future high performance engines.

II. FLOW CHART

The flowchart of the project is as given below on behalf of process going in manner.



III. THE PROPOSED 5T SRAM CELL CONFIGURATION

The proposed 5T SRAM cell with a write assist technique is shown figure. Unlike the traditional 5T SRAM cell, cross-coupled inverters are asymmetrical by sizing the driver transistor close to bitline BL to improve the write-ability of the cell. Thus, this design has the additional advantage of

increased current through the driver transistor during a read operation, and consequently lower read delay than the standard 6T cell. Beyond memory arrays, there are write assist, namely pre-charging circuit, standby start-up circuit and voltage control circuit. In all SRAMs, for each column in the SRAM array there is a bitline BL that connected to the pre-charging circuit. The function of the pre-charging circuit is to pull up the bitline BL of a selected column to VDD before the read or write operation. Furthermore, the standby start-up circuit design is to enable the single-port SRAM to quickly switch to the standby mode, and thus effectively to enhance the standby performance. Besides, the voltage control circuit is connected to the source terminals corresponding to driver transistors of each memory cell in a selected row cells. This configuration is intended to control the source voltages of driver transistors under different operating modes.

During a write operation, the voltage of nodes L1 and L2 are set to the ground voltage. Due to transistor N11 is sized smaller, the issue concerning the difficulty of writing '1' can be resolved. Specially, the reading operation can be divided into two stages. In the first stage, the voltage of node L1 (VL1) is set to a negative voltage called "RGND" to speed-up the reading speed.

However, in the second stage, the voltage VL1 is pulled up to ground to reduce power consumption. Under these circumstances, the voltage RGND can effectively improve the reading speed without incurring unnecessary power consumption. Finally, during a standby operation, VL1 and VL2 are set to VGS(N23) to reduce the leakage current.(Fig1)

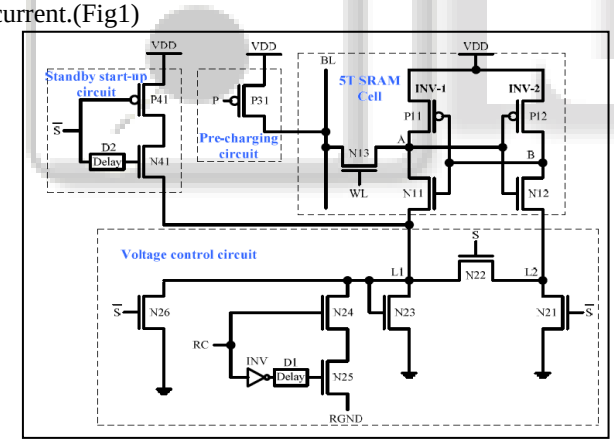


Fig. 1: Circuit diagram of the proposed 5T SRAM cell

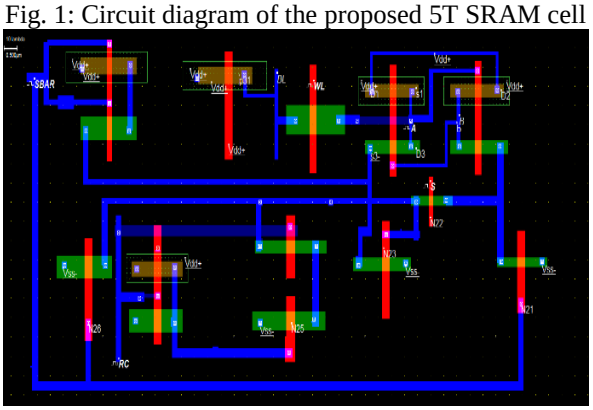


Fig. 2: Layout design of the proposed 5T SRAM memory cell using Microwind 3.1 software

IV. Simulation Result

The simulated output waveform of 5t SRAM cell for voltage vs. time is shown in Fig3.It is evident that the proposed 5T SRAM cell provides cells an efficient solution to the write '1' issue, that is the proposer 5T SRAM cell enabling a logic '1' to be easily written to the SRAM cell, as compared to the traditional 5T SRAM cells. The total power consumed by chip is 0.245 microwatt.

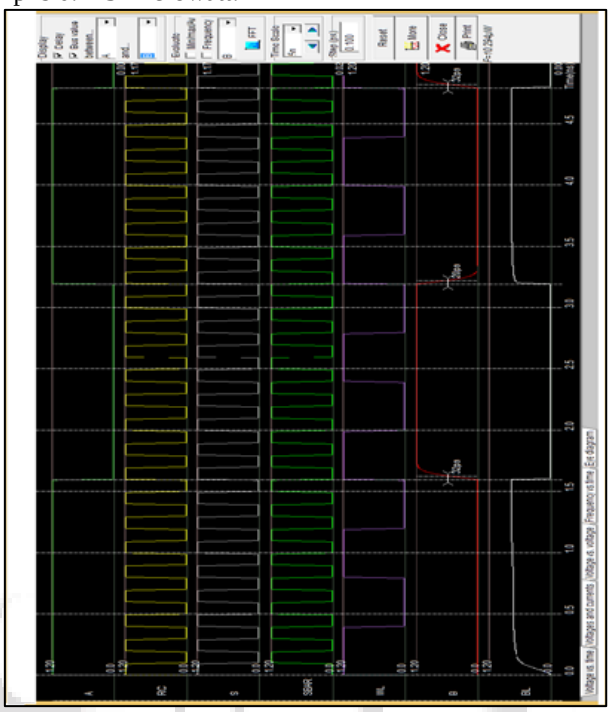


Fig. 3: Simulation for the proposed 5T SRAM cell

A. Characteristics Curve of Proposed 5t SRAM Cell

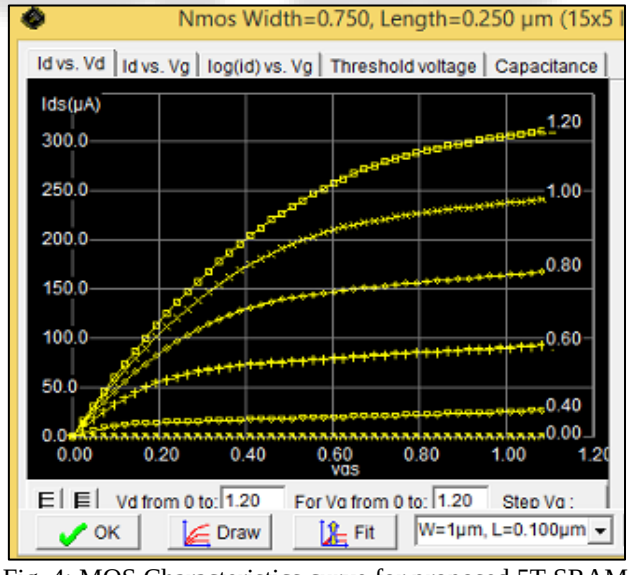


Fig. 4: MOS Characteristics curve for proposed 5T SRAM cell"

From Fig.4,it is observed, characteristics curve for Proposed 5T SRAM cell shows the curve Ids (µA) verses Vds (V) at variable value of Ig (µA). However, we can also show the characteristics curve for N transistors and P transistors of proposed 5-T SRAM cell.

V. CONCLUSIONS

The Proposed 5T SRAM cell, we have successfully implemented with 32 nm CMOS technology. The total chip area is 28.9 um^2. The total power consumption is reduced as 0.245 microwatt and it can also operate on high frequency up-to 5 GHz. Following table shows comparison of all mention SRAM cell.

VI. FUTURE SCOPE

There are some obvious ways to continue the above described work. The first step is to fabricate a chip using the memory array layout created throughout the work with this thesis. This would be a way to validate all the simulation work, and show that the memory really works in its physical form. For instance a porting to a 22nm technology could be done to evaluate the impact of scaling on the 5T SRAM cell. The layout of the cells used in this thesis have been made using regular logic design rules. When a SRAM memory is fabricated these rules result in much too large cells. Therefore special SRAM rules are used by the foundries when memories are fabricated. These rules are the result of manufacturing many chips and then settling for rules that give a high enough yield. One interesting continuation of this work would be a yield evaluation, using tighter rules, and compare the results to the regular 6T SRAM. This would in fact be one of the most important factors regarding the viability of the 5T SRAM in real microprocessors. Also in future, by using this technology we can expand frequency nearer to 13GHz and also used for next generation of telecommunication technology.

VII. APPLICATIONS

1) 5T SRAM cell uses 1 wordline and 1 bitline and extra read line control.
2) Fast low power SRAM have become a many critical component of many VLSI chip.

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