A Study on Recent Advancements in VLSI Technology using FinFETs

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Abstract— In view of difficulties of the planar MOSFET technology to get the acceptable gate control over the channel FinFET technology based on multiple gate devices is better technology option for further shrinking the size of the planar MOSFET, For double gate SOI-MOSFET the gates control the channel created between source and drain terminals effictively .So the several short channel effects like DIBL, sunthreshold swing gate leakage current etc. Without increasing carrier concentration into the channel. Scaling is one of the key factors of any new technology and it governs the design metrics of the complete technology. With the scaling up to sub-micro region, single-gate MOSFETs has served the purpose but as designing moves down in ultra-sub-micro region, the further scaling of single gate MOSFETs leads to a number of short Channel Effects which directly affects the various performance criteria and to resolve these effects, Multi-gate MOSFETs are designed and one of the most widely used and efficient is FinFET. This paper contains the brief explaination of FinFET, its structure overview, features and some of the latest work that has been carried out using FinFET.

Key words: FinFET, NonPlanar Structure, Digital Circuits and Memories, CMOS Scaling, Threshold Voltage, Fin width

I. INTRODUCTION

When we shrinking further the size of the planar MOSFET technology several short channel effects are produced. So instead of planar MOSFET technology DG-MOSFETs technology based on multiple gates device have better controlling over the SCEs. Particularly the FinFET technology provides superior scalability of the DG-MOSFETs compare to the planar MOSFET. It provides better performance compare to the bulk Si-CMOS technology. Because of its compatibility with the recent CMOS technology FinFETs are seen to be strong candidate for replacing the bulk or planar Si-CMOS technology from 22nm node onwards. Many different ICs like digital logic, SRAM, DRAM, flash memory etc. have already been demonstrated. Due to their better controlling over subthreshold leakage current and current saturation FinFETs are advantages for the high gain analog applications and get better result in the RF applications.

Evalution & Comparision of FinFET Technology: As devices shrink further and further, the problems with conventional (planar) MOSFETs are increasing. Industry is currently at the 90nm node (ie. DRAM half metal pitch, which corresponds to gate lengths of about 70nm). As we go down to the 65nm, 45nm, etc nodes, there seem to be no viable options of continuing forth with the conventional MOSFET. Severe short channel effects (SCE) such as V_T rolloff and drain induced barrier lowering (DIBL), increasing leakage currents such as subthreshold S/D leakage, D/B (GIDL), gate direct tunneling leakage, and hot carrier effects that result in device degradation is plaguing the industry (at the device level; there are other BEOL (back-end of the line) problems such as interconnect RC delays which we won't discuss here). Reducing the power supply V_{dd} helps reduce power and hot carrier effects, but worsens performance. Performance can be improved back by lowering V_T but at the cost of worsening S/D leakage. To reduce DIBL and increase adequate channel control by the gate, the oxide thickness can be reduced, but that increases gate leakage. Solving one problem leads to another. Efforts are on to find a suitable high-k gate di electric so that a thicker physical oxide can be used to help reduce gate leakage and yet have adequate channel control, but this search has not been successful to the point of being usable. There are problems with band alignment (w.r.t Si) and/or thermal instability problems and/or interface states problems (with Si). The thermal instability problem has led researchers to search for metal gate electrodes instead of polysilicon (because insufficient activation leads to poly depletion effects). But metal gates with suitable work functions haven't been found to the point of being usable. In the absence of this, polysilicon continues to be used, whose work function demands that V_T be set by high channel doping. High channel doping in turn leads to random dopant fluctuations (at small gate lengths) as well as increased impurity scattering and therefore reduced mobility. Indeed, it is felt that instead of planar MOSFETs, a double gate device will be needed at gate lengths below 50nm in order to be able to continue forth on the shrinking path.

II. WHAT IS A DG-MOSFET?

Double gate MOSFETs (DG-FET) is a MOSFET that has two gates to control the channel. Currently standard CMOS technology can be replaced by DG MOSFETs technology to increase the integration capacity of silicon technology in the near future. A DGSOI Structure consists, basically, of a silicon slab sandwiched between two oxide layers. Its schematic is shown i

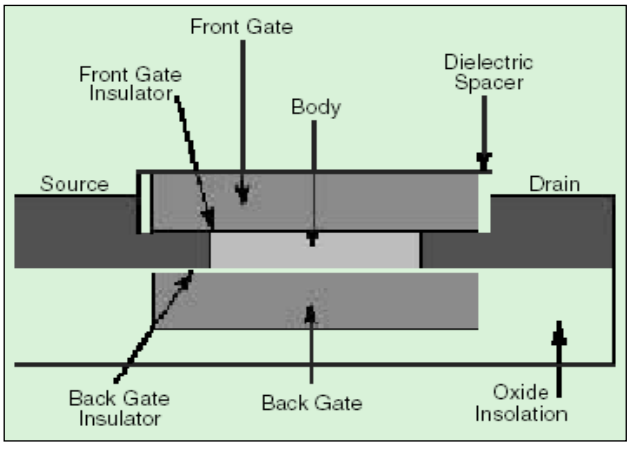

Fig. 1: Cross section of a generic planar DGFET

Its main advantage is that of improved gate-channel control. In conjunction with ultra-thin bodies in an SOI implementation (FDSOI DG-FET), it additionally offers reduced SCE, because all of the drain field lines are not able to reach the source. This is because the gate oxide has a lower dielectric constant than Si (assuming the oxide is SiO_2), and also because the body is ultra-thin. Because of its greater

resilience to SCE and greater gate-channel control, the physical gate thickness can be increased (compared to planar MOSFET). Thus it also brings along reduced leakage currents (gate leakage as well as S/D leakage).

Basically there are 2 kinds of DG-FETs: (1) Symmetric: - In Symmetric DG-FETs have identical gate electrode materials for the front and back gates means gate electrode material is same for both gate. When symmetrically driven, the channel is formed at both the surfaces.

Asymmetric: - In an asymmetric DG-FET, the top and bottom gate electrode materials can different. Channel is formed only in one surface.

Energy band diagrams for symmetrical and asymmetrical DG-FETs are shown in Figures 2 and 3.

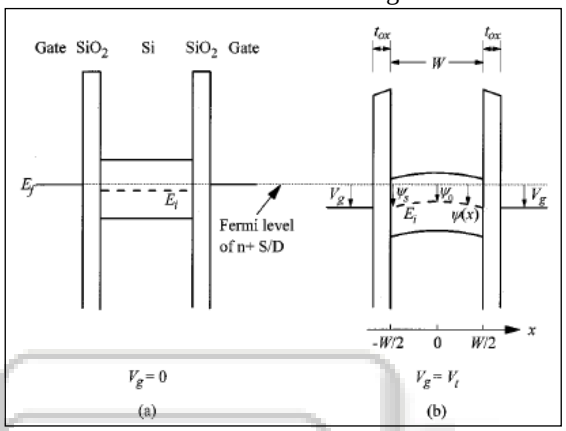

Fig. 2: Symmetrical DGFET energy band diagram

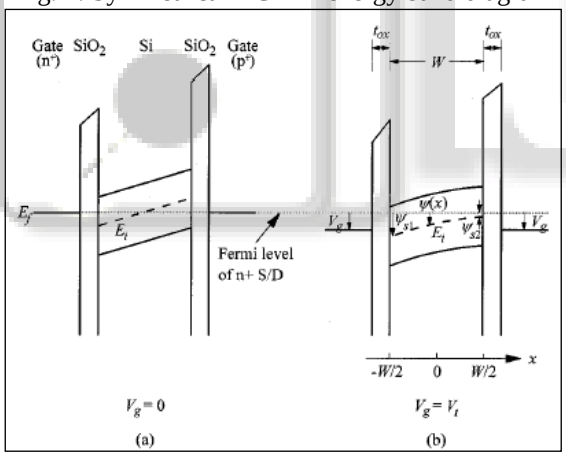

Fig. 3: Asymmetrical DGFET energy band diagram

III. FINFET STRUCTURE ANALYSIS

Type 3 DG-FETs are called FinFETs. Even though current conduction is in the plane of the wafer, it is not strictly a planar device. Rather, it is referred to as a quasi-planar device, because its geometry in the vertical direction (viz. the fin height) also affects device behavior. Amongst the DG-FET types, the FinFET is the easiest one to fabricate. Its schematic is shown in Fig. 4.

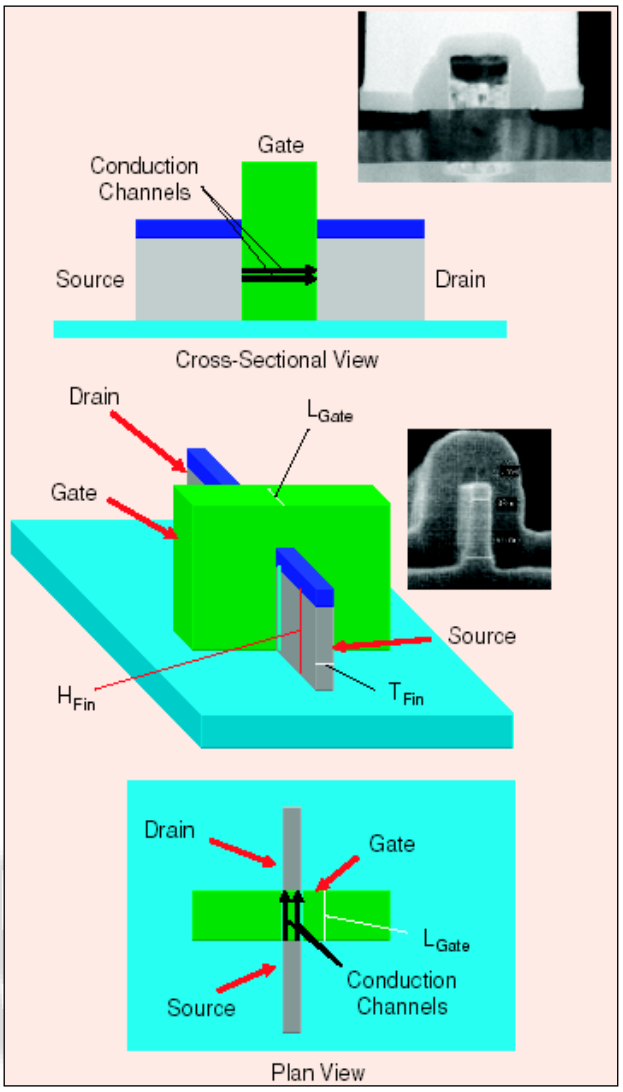

Fig. 4: FinFET structure, with dimensions marked (from [4])

Because of the vertically thin channel structure, it is referred to as a fin because it resembles a fish's fin; hence the name FinFET. A gate can also be fabricated at the top of the fin, in which case it is a triple gate FET. Or optionally, the oxide above the fin can be made thick enough so that the gate above the fin is as good as not being present. (This helps in reducing corner effects, discussed later in this report)

It should be noted that while the gate length L of a FinFET is in the same sense as that in a conventional planar FET, the device width W is quite different. W is defined as:

$$W = 2H_{fin} + T_{fin}$$

here H_{fin} and T_{fin} are the fin height and thickness respectively. Some literarefers to the fin thickness as the fin width). The reason for this is quite clear when one notices that W as defined above is indeed the width of the gate region that is in touch with (ie. in control of) the channel in the fin (albeit with a dielectric in between). This fact can especially be seen if one unfolds the gate (ie. unwraps it).

The above definition of device width is for a triple gate FinFET. If the gate above the fin is absent/ineffective, then the T_{fin} term in the above definition is taken out.

On the surface, this freedom in the vertical direction (of increasing H_{fin}) is a much desired capability since it lets

one increase the device width W without increasing the planar layout area! (Increasing W increases the I_{on}, a desirable feature). However, it will be seen in subsequent sections in this report, that there is a definite range (in relation to T_{fin}) beyond which H_{fin} should not be increased, else one encounters SCE.

IV. FABRICATION MECHANISM OF FINFET TECHNOLOGY

The key challenges in FinFET fabrication are the thin, uniform fin; and also in reducing the source-drain series resistance.

FinFET's have broadly been reported to have been fabricated in 2 ways

- Gate-first process: Here the gate stack is patterned/formed first, and then the source and drain regions are formed
- Gate-last process (also called replacement gate process): Here source and drain regions are formed first and then the gate is formed

Fig. 4 shows the FinFET fabrication process flow. As the starting material SOI wafer is used with a 400-nm thick buried oxide layer and 50-nm thick silicon film. The measured standard deviation of the silicon film thickness is around 20 A. Although the silicon film thickness determines the channel width, the variation is acceptable for the device uniformity. The larger source of process variation is the variation in gate length. As the gate length will vary process variation also vary.

The CVD SI_3N_4 and SiO_2 stack layer is deposited on top of the silicon film to make a hard mask or cover layer. The fine Si-fin is patterned by electron beam (EB) lithography with 100 keV acceleration energy. The resist pattern is slightly ashed at 5 W and 30 sec for the reduction of the Si-fin width. Then, using top SiO_2 layer as a hard etching mask, the SOI layer is etched. The Si is exposed only at the sides of the Si-fin as shown in Fig. 3(1). Fig. 4 shows the fabricated Si-fin width versus the design size with the EB dose as a parameter. Fine Si-fins down to 20 nm are obtained. Using EB lithography, the S/D pads with a narrow gap in between them are delineated. The SiO_2 and amorphous Si layers are etched and the gap between the S/D pads is formed as shown in Fig. 4(3). While the cover layer protects the Si-fin, the amorphous Si is completely removed from the side of the Si-fin. Fig. 7 shows the simulated current density distribution in the Si-fin and pad region of FinFET. The current density contour shows that the current quickly spreads into the pads. This suggests that the parasitic resistance is reduced as shown in Fig.5.

CVD SiO_2 is deposited to make spacers around the S/D pads. The height of the Si fin is 50 nm, and the total S/D pads thickness is 400 nm. Making use of the difference in the heights, the SiO_2 spacer on the sides of the Si-fin is completely removed by sufficient over etching of SiO_2 while the cover layer protects the Si-fin. The Si surface is exposed on the sides of the Si-fin again as shown in Fig. 4(4). During this over etching, SiO_2 on the S/D pads and the buried oxide are etched.

Notice that the channel width of the devices is twice the height of the Si-fins or approximately 100 nm. By oxidizing the Si surface, gate oxide as thin as 2.5 nm is grown. Because the area of Si-fin side surface is too small, we use dummy wafers to measure the oxide thickness. During gate oxidation, the amorphous Si of the S/D pads is crystallized. Also, phosphorus diffuses from the S/D pads into the Si-fin and forms the S/D extensions under the oxide spacers. Then, boron-doped $SI_{0.4}Ge_{0.6}$ is deposited as the gate material. Because the source and drain extension is already formed and covered by thick SiO_2 layer, no high temperature steps are required after gate deposition. Therefore, the structure is suitable to use with new high gate dielectric and metal gates that are not compatible with each other under high temperature. After delineating the gate electrode as shown in Fig. 4(5), the probing windows are etched through the oxide. We directly probe on the poly-Si and poly-SiGe pads, with no metallization used in this experiment. The total parasitic resistance due to probing is about 3000 ohms.

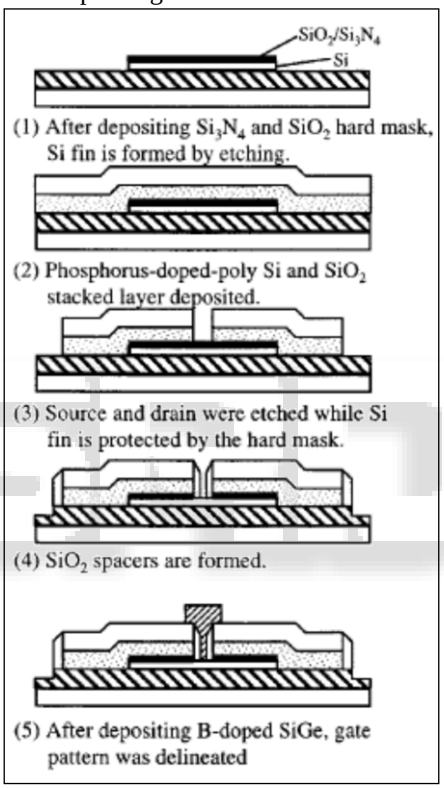

Fig. 5: FinFET fabrication process flow

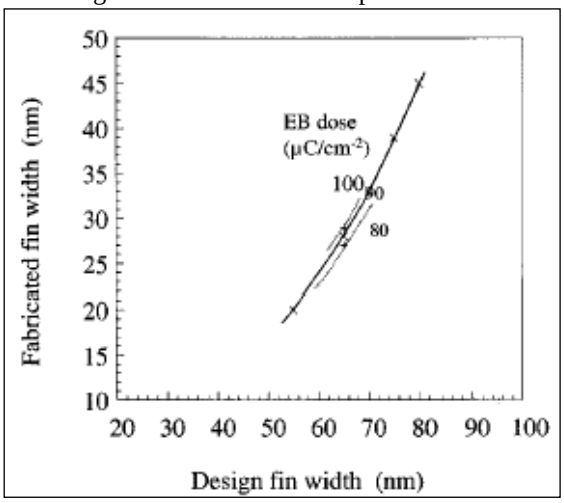

Fig.6: Relationship between designs Si-fin width practical size with EB dose as a parameter

V. CONCLUSION

FinFETs appear to be the device of choice in sub-50nm designs, because of their reduced short channel effects (SCE) and relative ease of integration into existing fabrication processes. They seem well suited to help us stay on track with Moore's law, for a little while longer.

A gate-first method of fabricating FinFETs is advantageous in that it is more akin to the conventional CMOS process. This is probably the reason why there is more literature on this method. On the other hand, a gate-last method of fabricating FinFETs is advantageous from a thermal stability point of view when introducing metal gates and high-k gate dielectrics.

Tall, thin fins help minimize SCE, but tend to increase series resistance. For best SCE, keeping manufacturability in mind, the ideal dimensions reported are a fin thickness of one third the channel length. Tall fin heights are desirable because they yield higher ON currents (increased W_{eff}), but it gets more difficult to manufacture them with uniformly steep sidewalls. So a fine balance needs to be struck.

FinFETs need to be used with metal gates with appropriate work function, for yielding desired V_T. Also, undoped fins need to be used to minimize corner effects. It was shown that Molybdenum with controlled Nitrogen doping is suitable for this.

On the modeling front, compact models for FinFETs need to evolve more.

Lastly, self heating problems, which are inherent in SOI devices and not limited to FinFETs, need to be handled before FinFETs can be adopted on a large scale.

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