# Hardwired BIST Architecture of SRAM

**Sonam Rawat[1] Shikha Goswami[2] Vikas Gupta[3]**
[1,2,3]Department of VLSI Design
[1,2,3]P. K. University, Thanra Karera, Shivpuri, MP, India

*Abstract*— As the compactness of system on chip (SoC) increase, it becomes striking to integrated test logic on a chip. Starting with a broad idea of test problems, this survey paper on focus on "Chip" Built in Self-Test (BIST) study and its promotion for board and system level application. It became highly important to test various kinds of defects rapidly and precisely to reduce the testing cost and to improve the memory quality especially in a SoC (System on a Chip)design environment .memory defects can be moduled as struck-at, coupling, transition address decoder, and pattern sensitive feels. Recently BIST research is being highly used in VLSI and SoC testing for the detection fault coverage.

***Key words:*** Built in Self-Test Circuit under Test, Device under Test, IC, SOC, Register Faults, CRC

## I. INTRODUCTION

Built in Self-Test (BIST) technique constitute a group of technique that provide the capability of performing high fault coverage with speed testing ,whereas simultaneously they relax the reliance on expensive external tols. Hence they constitute an attractive solution to the crisis of testing VLSI devices. BIST technique are typically classified into online and offline. Offline architectures operate in either test mode or normal mode. During test mode, the input generated by a test generator unit are applied to the inputs to the circuit under test and a result are captured into a response verifier. the functionality of gadgets and electronics equipment's has achieved a phenomenal growth over the last two decades while their physical sizes have come down significantly .the main reason is, due to the rapid advanced in IC technologies, which enables fabrication of several millions of transistors in a single chip or integrated circuit. According to Moore's law, number of transistors in a chip doubles in every 1.5 years with the recent in the technology, device shrinks to nanometer scale, but complexibility and density to the chips keep on increasing. VLSI testing is becoming more and more important and challenging to verify a device functions are properly or not .the Built in self-test is widely used in the online testing while chip in normal operation. Memories are the most universal component today. Almost all system chips contain some type of embedded such as Rom, SRAM, DRAM and flash memory.

### *A. Background & Motivation of Research*

The built in self-test concept originated with the idea of including a pseudorandom number generator (PRNG) and cyclic redundancy check on the chip. if all the registers that hold state in an chip are on several internal scan chains then the task of registers and the combinational logic between them will generate a unique CRC.

## II. BIST (BUILT IN SELF-TESTING)

BIST places the job of devices testing inside the device itself and generates its own stimulus and analyzes its own response. the trendto include more test logic on an ASIC has already been mentioned BIST.it is a structured test technique for combinational and sequential logics, memories, multiplier and other embedded logics block.in each case the principle is to generate test vectors apply them to device under test or circuit under test.

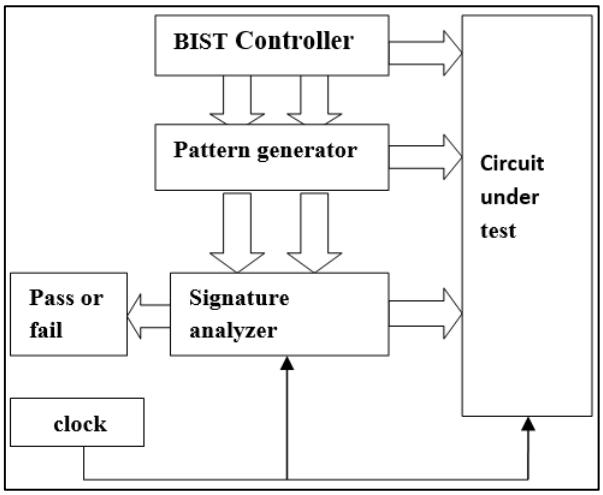


Fig. 1: Architecture of BIST Technique

Testing in its broadest sense means to examine a product and to ensure its functioning .the testing scheme in which all the components of external tester are integrated to into a chip.so that an external tester is eliminated is known as BIST. This requires connecting external equipment to the CUT. It increase the testing time. There are three type of BIST available they programmable BIST, micro coded BIST and hardwired BIST /on chip BIST. Among these BIST the hardwired BIST takes less time in fault detection and these BIST works for an application specific detection. In this case, the detection of faults is restricted to storage. Table I reviews the different type of BIST applied to SRAM.

| scheme | Parameter of BIST | | |
|---|---|---|---|
| | Test length | complexity | Fault coverage |
| Hardwired | short | High | medium |
| microcode | average | Medium | Low. |
| processor | Long | Low | high |

Table 1: Different BIST Scheme

Although, from table Iit can be concluded as the main advantage of hardware BIST is short test length which result is reducing the testing cost. But, it has some disadvantages like optimum logic overhead or less flexibility. This result in huge investments for redesign and reimplementation of the on chip BIST for any minor change or detecting other faults. Hence, there is a tradeoff between area overhead and cost of testing as, it depends on the test length.

The increasing complexibility in testing memories has given rise to develop smarter test techniques in different BIST schemes such as programmable or micro code and processor level. In programmable and processor based memory BIST schemes the

 

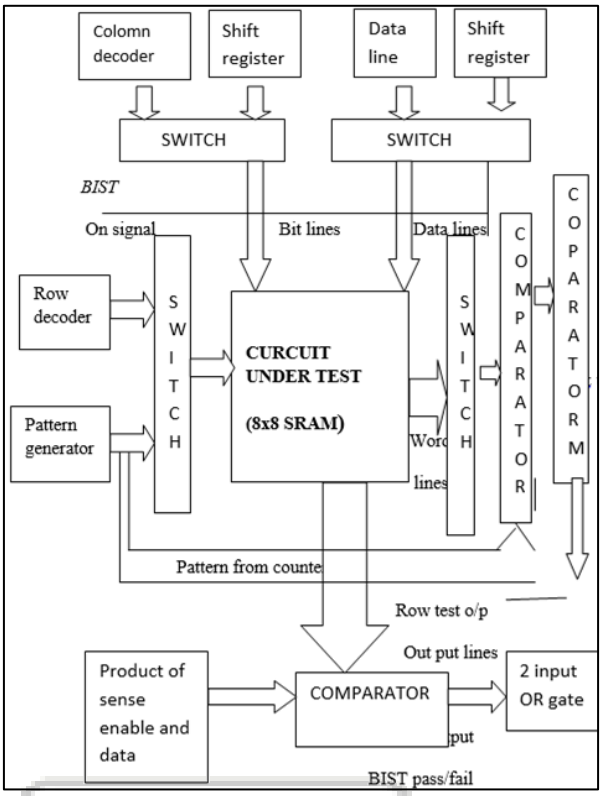


Fig.2. Proposed Hardwired BIST Architectu

1time is reduced by the use of parallelism within the memory device. By the use of parallelism a massive reduction in test time is achieved, which simultaneously reduces the testing cost also.

In this paper, it has been tried to make a hardwired BIST which can detect the storage and retrieval faults of SRAM. The proposed BIST architecture's objective is to decrease test length and complexity of the circuit by replacing linear feedback shift register through counter based pattern generator which help us to eliminate look up table or storing the data and then, comparing that with Implementation of the testing logic is done via both ways is done between the output result and reference data, which facilities to detect the storage and retrieval faults easily. Therefore, emphasizes was given on detecting faults during reading and writing of the memory cell array.

The paper concludes description of designing, working and feasibility of the hardwired memory BIST. The proposed BIST architecture is shown in fig. 2.

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There are basically five parts of the proposed BIST architecture which are test pattern generator, cut, switches, comparator and compactor. They are illustrated as:

### *A. Test Pattern Generator*

This block consist of two parts which are addresses counter for row address and shift registor for dataand column address. The address counter is formed by combination of up and down counter and, it generate 8-bit sequence stated as:

00,FF,11,EE,22,DD,33,CC,44,BB,55,AA,66,99,88, 77. The output sequence is based on control signal and thus, output of two counter are selected by control signal. when control signal is "on" the sequencial up-counter goes to output and, when control signal is" off". The sequence of down counter goes to output. The design of address counter is stated is fig.3.

Another is serial in parrelor out registor, employed for data and the column address. The column addres s is used for selecting the whole column sequencially with the help of shift register. The schematic of shift registor are shown in fig.4.

### *B. Circuit-under-test (CUT).*

The 8*8 SRAM cell is being tested. the input of this CUT are data lines, column and row address corresponding with the read and write signals utilized for storing of data from a desired SRAM cell and the data out is output line.

### *C. Test Pattern Comparator an Compactor*

The comparator block compares the references data with output of the circuit. It is an essential part of memory testing. This block is made by XOR which is used for comparison purpose. In this case, of comparator, the output pattern are compressed using 8-bit OR gate. Fig.5 and fig.6shown block diagram of test pattern comparator and compactor which are used in this hardwired BIST.

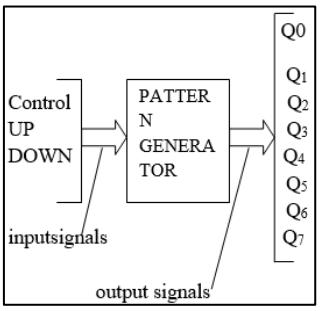


Fig. 3: Block Diagram of Address Counter

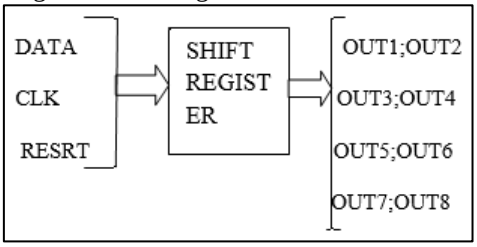


Fig. 4: Schematic of Shift Registor

 

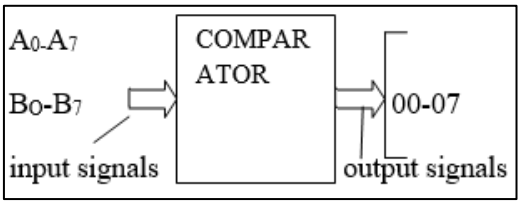


Fig. 5: Block Diagram of Comparator

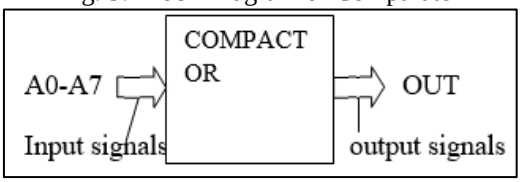


Fig. 6: Block Diagram of Compactor

*D. Switch*

It essential, switches from the routine memory operation to BIST operation; by isolating the normal operation signals and sending the BIST signal. two types of switches are used here- one which acts when it is in "on" condition, the signals essential for BIST operations goes from the input side to the output side and ,in the other one i.e "off" condition, it become in-active. The schematic are shown in fig. 7.

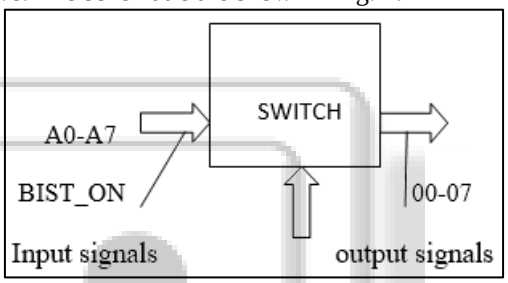


Fig. 7: Schematic of Switch

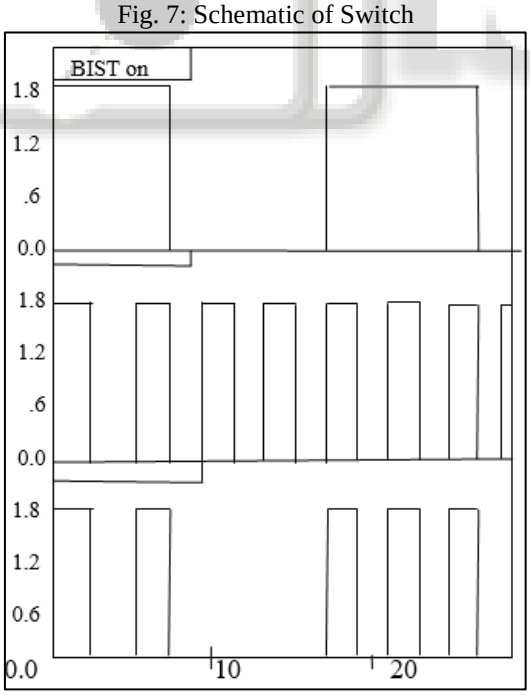


Fig. 8: Waveform of Switch

Another type of switch which is used in this architecture is isolating switch. It has two condition, when it is "on" condition then, the essential signals for BIST operation goes to the output side and, in the "off" condition, the routine signals for memory functions goes to output side.

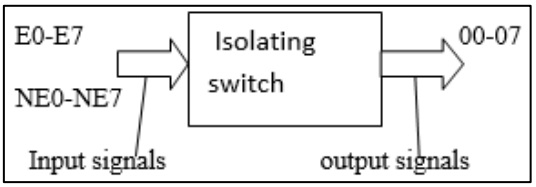


Fig. 9: schematic of Isolating Switch

## III. FUNCTIONING OF MEMORY BIST

The proposed BIST scheme has the ability to test column and row wise. The functioning of the BIST architecture is explained by the flow graph which has shown in fig.10. Further the testing procedure is elaborately described they are follow in fig. 10.

*A. Row Wise Detection*

The row wise faulat is determined by making the column serially on and, then, serially off and subsequently, giving data on them.

In this method the transition of 1-0-1-0-1-0 is given to see the transient fault also, by given this type of transition to the address, the robustness of CUT can be tested. In this way , one can find the fault in row wise only by observing the output of the row comparator i.e. if 1 comes CUT is faulty and if 0 comes CUT is non faulty.

*B. Column Wise Detection*

In this phase, it has been seen that the output of the column is correct or not. The sense amplifier is giving output whenever the sense enable is on. For the reading of data from the SRAM, the sense amplified should be on. Therefore, the reading time depends on the value stored and sense enable signal. Thus during the read time, both data and sense enable should be on. Therefore by taking this concept in mind the circuit has been designed to determine the fault in column circuity. The resultant output is compared with the help of comparator block and simultaneously compacted using OR gate. Thus, the resultant output will be column BIST output.

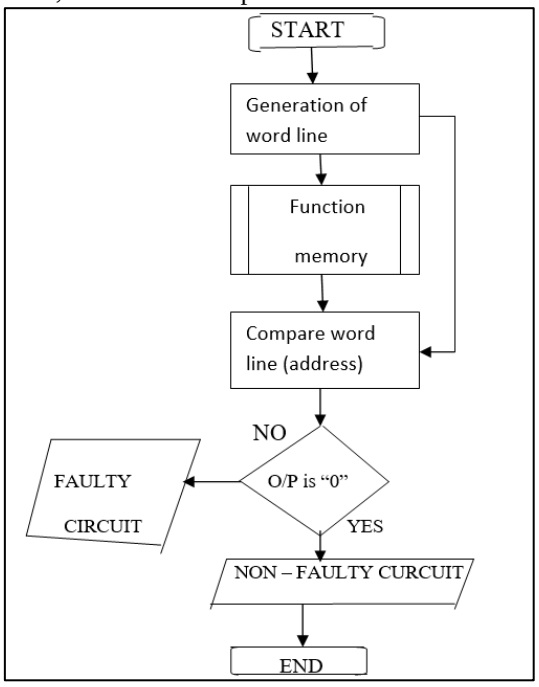


Fig. 10: Flow Graph Showing the Row Testing

 

## IV. RESULT & DISCUSSIONS

The finding of the work has two aspects-one is determination of non-faulty/faulty CUT on the basis of storage and retrieval faults, though, the simulation and analysis of proposed BIST architecture. The result of this analysis shows that the circuit. The BIST scheme is working correctly. The second aspect is the feasibility test for area and power overhead calculation of the additional BIST circuit. Therefore, the proposed on-chip BIST can be easily feasible for the larger memory size.

## V. CONCLUSION

On-chip BIST architecture is used to detect the storage and retrieval faults in the SRAM cell array. Hardwired approach is used in place of an algorithmic approach which provides the advantage of short test time and small overhead area. This scheme is useful to detect which column/row is faulty. The overhead area and power has increases due to additional on – chip BIST architecture for small size memory but as it has been shown in feasibility test that the increments are nominal with respect to the large size memory.as this feasibility check it will be done in future. Presently, the fault coverage is less due to dynamic faults not considered through this architecture.

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