Design of Four Quadrant Current Mode Analog Multiplier at 0.25 µm CMOS Technology

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Abstract— For analog signal processing non-linear operation on signal is required there are several applications where analog signals need to be multiply/ divide and squaring is required such as modulation, AGC etc. The non-linearity of conventional bipolar transistor can be used for multiplication by using trans-linear operation but the large size and power consumption limits the use of BJT. Extension of trans-linear operation to MOS transistors solves the issue of size and power consumption but the scaling of MOS transistor produces several errors. Such error can be resolved by using two transistor and a resistor in trans-linear loop. In this paper a current mode four quadrant current multiplier was designed that uses current squaring and subtract identity to achieve multiplication. The circuit is designed at 0.25 µm CMOS technology at 1.8 V dual power supply.

Key words: Analog Multiplier, CMOS Technology

I. INTRODUCTION

There is wide application of multiplier in analog signal processing such as modulation, frequency doubler, Automatic gain control (AGC), artificial networks etc. There are two categories of analog multiplier one is voltage multiplier where voltage is the input and other is current multiplier for current as input [2]. Low non-linearity error, low power and lower supply voltage operation made current mode multiplier more popular.

Multiplier takes two inputs x and y and produces output z = Kxy, where k is multiplication constant. Dual power supply V_{DD} and V_{SS} is required for dual mode four quadrant multiplier [1], and also provides better common mode noise cancellation.

Trans-linear operation is used in designing of current mode circuit extension of trans-linear operation to MOS transistors (MTL) [3] enable MOS transistors to use in non-linear signal processing.

Reduction of MOS size many effects become significant such as second order effects, reduction in carrier mobility, body effect and channel length modulation that causes distortion and error at the output. Few techniques has been proposed in the literature to reduce the alteration of carrier mobility and body effect [4-5]. Mobility reduction can be cancelled by adding two transistors and a resistor in the squarer circuit. Smaller transistor size and low supply voltage is used in this design rest of the paper is organized as follows section II will cover the designing of current multiplier, section III will discuss the results of the design and section IV will conclude the design.

II. CIRCUIT DESIGN

MOS transistor drain current in saturation region is given by the equation 1

$$I_D = \frac{K}{2}\left(V_{gs} - V_{th}\right)^2 \qquad (1)$$

The above equation can be rearranged to derive the gate to source voltage of MOS transistor

$$V_{gs} = V_{th} + \sqrt{\frac{2I_D}{K}} \qquad (2)$$

Where $K = \mu_0 C_{ox}\frac{W}{L}$ is the trans-conductance of MOS transistor.

Taking carrier mobility in account the MOS current in saturation region is given by

$$I_D = \frac{K}{2}\frac{\left(V_{gs} - V_{th}\right)^2}{1+\theta\left(V_{gs} - V_{th}\right)} \qquad (3)$$

Where θ is the mobility reduction parameter. From equation (3)

$$V_{gs} - V_{th} = \frac{I_D\theta}{K} + \sqrt{\left(\frac{I_D\theta}{K}\right)^2 + \frac{2I_D}{K}} \qquad (4)$$

Considering $\left(\frac{I_D\theta}{K}\right)^2 << \frac{2I_D}{K}$ equation (4) can be approximated as

$$V_{gs} - V_{th} \approx \frac{I_D\theta}{K} + \sqrt{\frac{2I_D}{K}} \qquad (5)$$

Applying KCL at node 1following result can be achieved

$$I_{OUT} = I_{D8} + I_{D9} - I_B = \frac{I_{in}^2}{4I_B} \qquad (6)$$

The four quadrant multiplier is based on the square difference identity. Let X and Y are the two inputs the above said identity can lead to following result

$$\left(X+Y\right)^2 - \left(X-Y\right)^2 = X^2 + Y^2 + 2XY - X^2 - Y^2 + 4XY$$
$$= 4XY$$

The block diagram of current mode multiplier is shown in the figure 1

A. (I_X+I_Y) AND (I_X-I_Y) Current Generator

The adder and substractor of the two currents I_X and I_Y is shown in the figure 2.

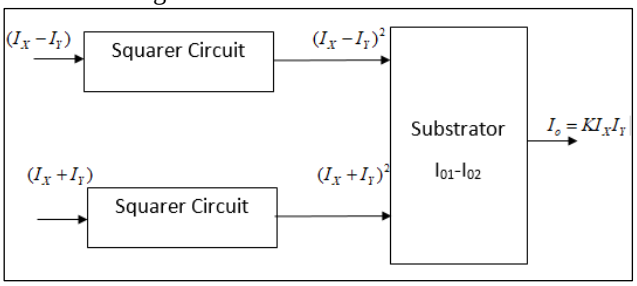


Fig. 1: Block diagram of four quadrant current multiplier

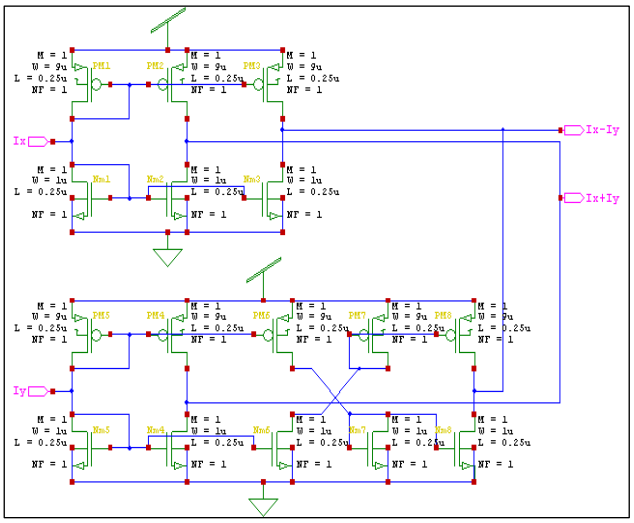


Fig. 2: $(I_X + I_Y)$ and $(I_X - I_Y)$ generator

A set of transistor is in current mirror mode and PM3 and NM3 works as buffer to provide certain gain. The first half of the circuit provide the $(I_X + I_Y)$ and the second section provides $(I_X - I_Y)$ by inverting the I_Y and later added to I_X. The resultant output of this circuit fed to current squarer circuit that squares the $(I_X + I_Y)$ and $(I_X - I_Y)$.

B. *Current Squarer Circuit*

Current squarer circuit takes the $(I_X + I_Y)$ and $(I_X - I_Y)$ as input. The circuit diagram of current squarer is shown in figure 3. A constant current source along with current mirror circuit is used to provide constant and stable bias current. MOS transistor works in saturation region that provides drain current as shown in equation 1.

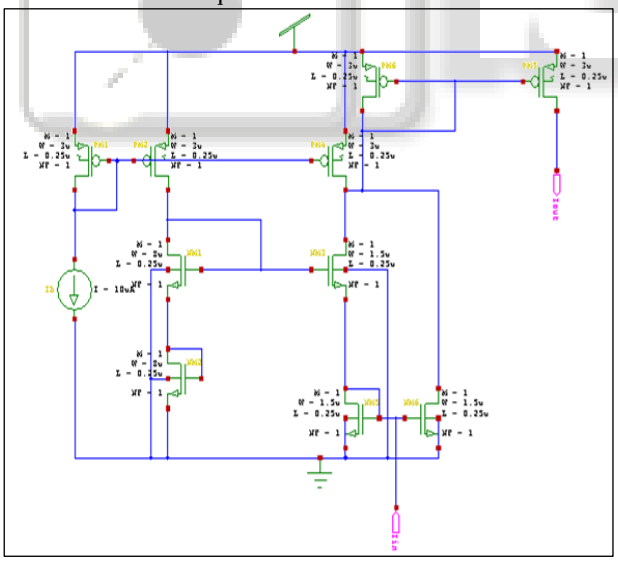


Fig. 3: Current squarer circuit

The change in the voltage of transistor NM2 produces change in the gate to source voltage of transistor NM3-NM4, thus the current trough it can be given by

$$I_3 = \frac{K}{2}\left(V_{23} - V_t\right)^2$$

Where V_{23} is the gate to source voltage of transistor NM3-NM4 and V_t is the threshold voltage of MOS transistor. Voltage at node 1 is given by

$$V_1 = R\left(I_{in} + I_{bias}\right)$$

Where I_{in} the input is current, I_{bias} is constant current and R is the resistance offered by the NM2 MOS transistor that operates in linear region determines the voltage at node 2.

$$V_2 = R\left(I_{in} + I_{bias}\right) + V_t + \sqrt{\frac{2I_{bias}}{K}}$$

$$V_0 = RI_{bias} + V_t + \sqrt{\frac{2I_{bias}}{K}}$$

$$V_E = V_0 - V_t$$

From equation the output current can be shown as

$$I_0 = K\left(RI_{in} + V_0 - V_t\right)^2 = K\left(RI_{in} + V_E\right)^2$$

C. *Current Multiplier*

The schematic of current multiplier is shown in figure 4. The mobility reduction in carrier is compensated by adding a resistor R that is designed by using a MOS transistor its value can be changed by varying its aspect ratio. For this design resistor R is set at 10 KΩ.

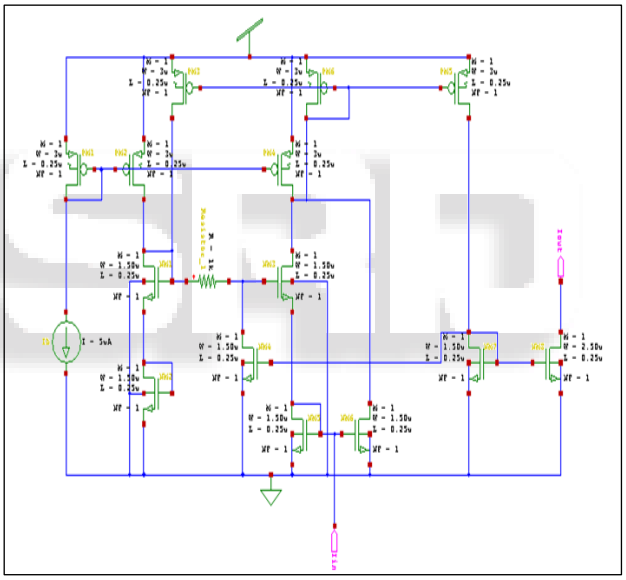


Fig. 4: Current Multiplier

The output current is of the circuit is given by

$$I_{o1} = \frac{\left(I_X + I_Y\right)^2}{4I_B}$$

$$I_{o2} = \frac{\left(I_X - I_Y\right)^2}{4I_B}$$

After subtracting both the output currents the resultant current can be given as

$$I_{out} = \frac{I_X I_Y}{I_B}$$

Here $K = \frac{1}{I_B}$ multiplication factor thus the resultant output current is given by

$$I_{out} = KI_X I_Y$$

III. SIMULATION RESULT

The transient response of the current adder and substarctor circuit for Ix = 10 µA at 100 kHz and I_Y = 5 µA with 10 kHz is shown in the figure 5. The simulation is done on Tanner EDA W edit at 1.8 V dual power supply using 0.25 µm CMOS technology.

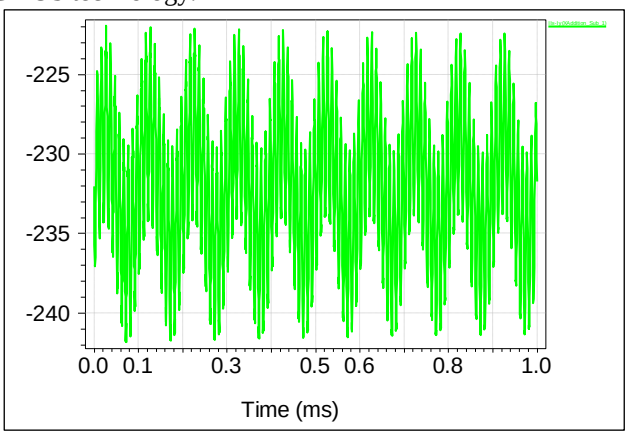


Fig. 5: Transient response of (I_X –I_Y)

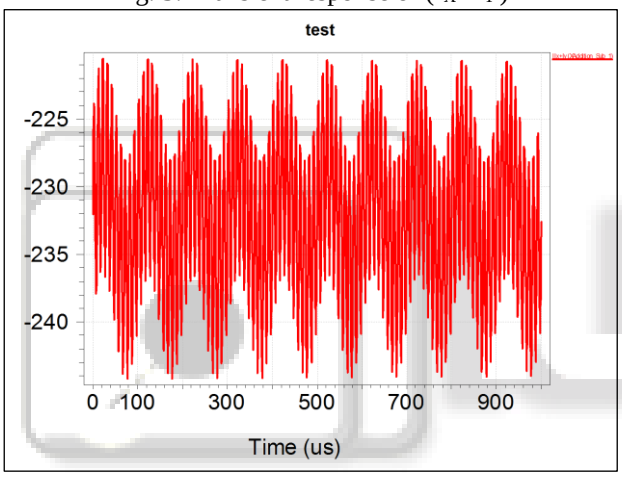


Fig. 6: Transient response of (I_X +I_Y)

DC transfer characteristics of current squarer circuit is done at 1.8 V power supply with bias current of 10 µA. Both the input current I_X and I_Y are swept from -10 µA to 10 µA with step size of 0.1 µA. The control voltage is taken 1.2 V and the passive resistance of 10 kΩ. The transfer characteristics of current squarer is shown in figure 7.

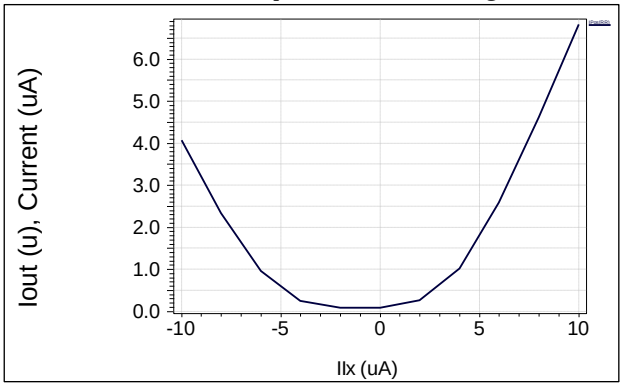
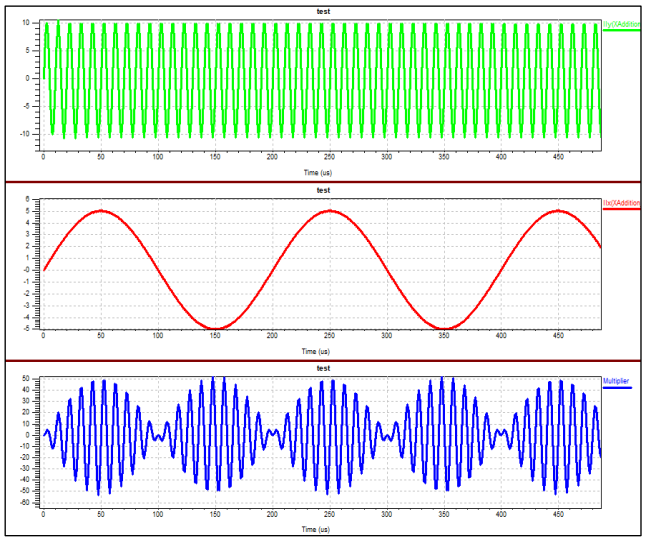


Fig. 7: DC simulation result for the output currents

The Transient response of current mode multiplier is shown in figure 8 for I_X = 10 µA at 100 kHz and I_Y = 5 µA at 1 kHz, the supply used is 1.8 V simulated using 0.25 µm CMOS technology.



IV. CONCLUSION

A low voltage current mode four quadrant analog multiplier was design in this paper. Mobility reduction due to transistor scaling and other parasitic effects has been cancelled by using MOS transistor in trans-linear loop. The design linear current squarer circuit and square difference identity to produce current multiplication.

The circuit was designed at 1.8 V dual power supply at 0.25 µm CMOS technology and simulated on Tanner EDA.

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