Design of Differential Low Noise Amplifier using Different CMOS Process: A Review

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Abstract— The objective of this paper is to design differential low noise amplifier using different technologies. We have designed 2.4 GHz DLNA using 0.18µm CMOS process, the DLNA is biased at 1.8 v supply and perfectly matched with input impedance of 50Ω.Then designed 21GHz UWB DLNA using 0.13µm CMOS process , the amplifier is driven by 1.2v power supply and after that designed 4.1 GHz narrowband DLNA using 0.18 CMOS process, applicable for global positioning system receivers with bandwidth 90MHz and stability of design is also verified.

Key words: DLNA, Impedance Matching, CMOS Technology, Noise Figure, Gain

I. INTRODUCTION

Communication system can't be possible without a Low Noise Amplifier (LNA). LNA is the basic building block of every communication system. In modern communication field, Radio Receiver plays a very important role, and a Radio Receiver is made from LNA, Mixer and Filter, where LNA plays a very important role. LNA is an electronic amplifier used to amplify a very weak signal and it is the first stage of radio receiver. A good LNA has large gain, low noise figure and higher intermodulation and compression point.

This paper presents the designing of DLNA using different technologies .Three parts are there first is design of 2.4 GHz DLNA using 0.18µm technology , second is design of 21 GHz UWB DLNA using 0.13µm technology and third is design of 4.1GHz narrowband DLNA .

A. Design of 2.4GHz differential low noise amplifier using 0.18µm CMOS process

Generally s-parameter and normal devices are used to design LNA. Advantage of s-parameter type device is it is built in device with no external bias so it is widely used. A good LNA provides very high gain, good input output matching, high linearity and very low power consumption. To design DLNA single ended source degenerated LNA is used.

Advantage of differential LNA is that it avoids the even harmonic term in output so reduces noise to a very small value. In designing of LNA proper selection of transducer is required so that it can provide maximum gain and low noise figure, because signal received at the antenna of receiver is comparatively weak.

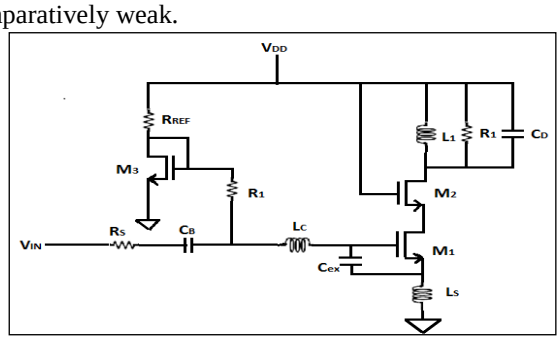

Fig. 1: Single ended source degenerated LNA

Single ended source degenerated LNA is shown in fig. 1. Operating frequency is the resonance frequency, given by the Ld with the drain node capacitance of M2. Proposed circuit is low power circuit. M3 is in current mirror connection with M1 which is used for biasing the LNA circuit. Gate source voltage of M1 is decided by the proper selection of width of M1.M1 provides the cascode amplifier with an infinite input resistance. Cascode is able to reduce the gate to drain capacitance of M1, this is because the input resistance of M2 is much smaller than output resistance of M1. To obtain the width of M1,

$$W_{opt} = 1.5(\omega_0 L C_{0X} R_s Q_{in,opt})^{-1}$$

Here W_{opt} is width of transistor M1, L, C_{ox} and Q is effective channel length, oxide capacitance and circuit quality factor.

Quality factor is given by,

$$Q = \frac{1}{SC_{gs}\left(SL_g + \frac{1}{SC_{gs}}\right) + SL_s(g_m + SC_{gs})}$$

Gain is given by,

$$\frac{V_{out}}{V_{in}} = -\frac{L_d}{L_s}$$

With the help of single source degenerated circuit we have designed a differential LNA shown as

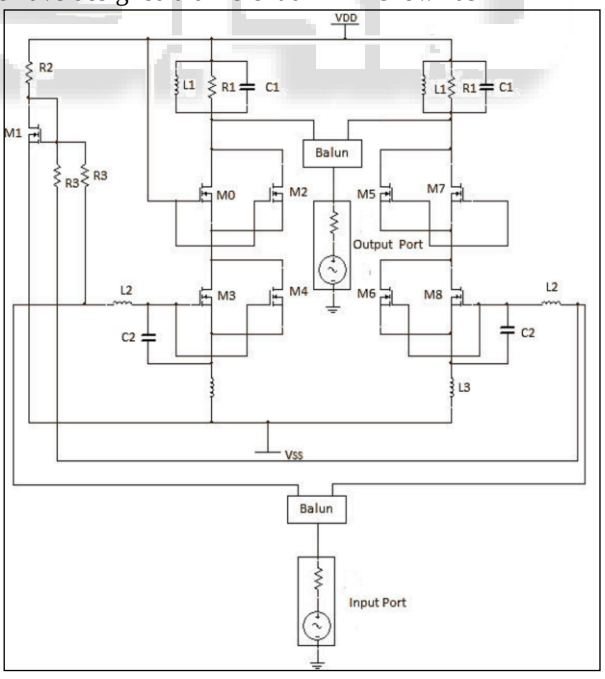

Fig. 2: Schematic of DLNA

Design specifications are supply voltage is 1.8v, gain is >20dB, noise figure is < 2.5dB, input impedance is <-20dB and output impedance is <-10dB.

B. Design of 21GHz UWB DLNA using 0.13µm CMOS process

A passive matching technique is used at the output to circumvent the degrading effect of the low quality factor of on-chip inductors. It also helps us to avoid the use of multiple stages or transmission line based matching technique which are inherently space consuming.

The circuit of the 21 GHz differential LNA is shown in Fig 3. In this common source configuration Ld1 and Ld2 resonate with the gate-drain capacitances of M3 and M4 respectively to define the central operating frequency of the LNA. M1 and M2 perform the role of the driving transistors and M3 and M4 isolates the output from the input.

At input of the amplifier,

$$\text{Zin} = \frac{\text{gm1Ls1}}{\text{Cgs1}} = 50\Omega$$

Where, Rs is the signal source or the antenna resistance.

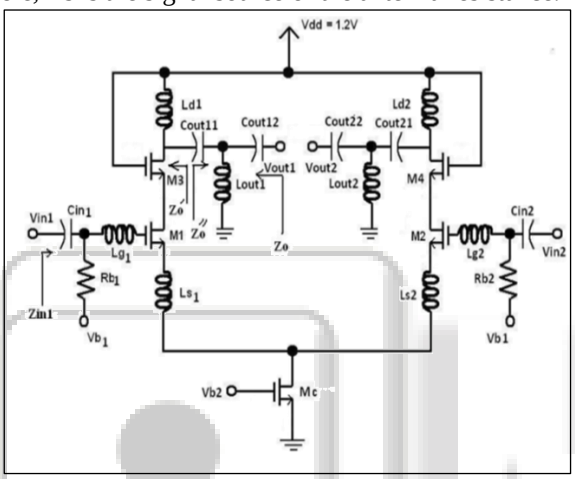

Fig. 3: 21GHz UWB DLNA

Gain of the amplifier depends on the load resistance of the resonance tank formed by the parallel combination of the load inductors (Ld1 and Ld2) and gate-drain capacitors of isolating transistors M3 and M4, diminishes with increasing frequency. Now if 50Ω low resistance is connected directly without any matching network, the effective resistance would get reduced and gain would follow.

It may be noted that Vb1 is provided by the gate of a PMOS whereas Vb2 is provided by an NMOS gate, because the Vb1 and Vb2 voltages are nearer to the Vdd and ground voltages respectively. For a 0.13µm CMOS process Vdd is set to 1.2V.

C. Design of 4.1GHz narrowband DLNA using 0.18µm CMOS process

In this a number of constraints are used in designing of LNA. The main constraint used is that LNA mostly needs to deal with limited channel bandwidth allocated to each user. That is why the proposed LNA would be narrowband. Narrowband LNA avoids leakage to the adjacent channel.

The noise figure of LNA directly adds to that of receiver. For a typical RX noise figure of 6 to 8 dB, it is expected that the LNA contributes about 2 to 3 dB, and the remainder of the chain about 4 to 5 dB.

The gain of the LNA must be large enough to minimize the noise contribution of the subsequent stages. The forward gain parameter, S21 is required to be 10dB or more for a good performance. The Reverse Isolation parameter, S12 is expected to be -10dB or less. Proper matching must be ensured at the interface between the antenna and the LNA. Poor matching at the RX input leads to significant reflection, which, in turn, reduces gain. For the same reason, the LNA output must also be matched to the input impedance of the subsequent stage .

Finally, the LNA must remain stable for all source impedances at all frequencies. Stern Stability Factor, K is a parameter which characterizes the stability of circuits

$$\text{K} = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|}$$

Where,

$$\Delta = S_{11}S_{22} - S_{21}S_{12}$$

If , K>1 and Δ<1, then the circuit is unconditionally stable.

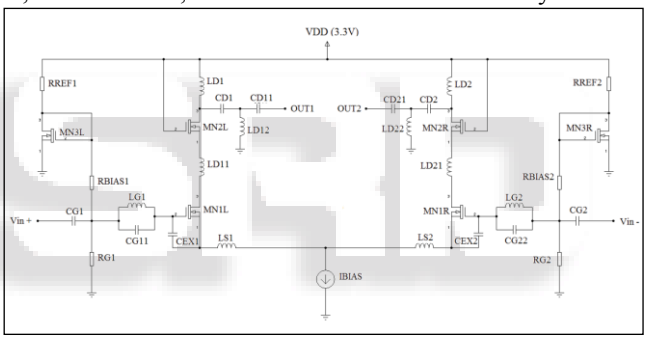

Fig. 4: Schematic diagram of 4.1GHz narrowband DLNA

Inductive Source Degeneration topology offers the most satisfactory Noise performance. However, an inherent problem in this topology is a sensitivity to gate induced current noise. So, in order to reduce this noise effect, a capacitor Cext is inserted in parallel to Cgs . For having a substantial control over the gain of LNA an inductor is introduced between MN1 and MN2. This inductor has a direct influence on the forward gain of the amplifier and thus the overall chip size is supposed to get increased. To minimize power consumption in circuit the width of MN3 would be tenth of width of MN1.

II. COMPARISONS

Technology	0.18µm	0.18µm	0.25µm	0.13µm	0.35µm	0.18µm
Frequency (GHz)	2.44	2.45	1.22	21	18.2	14.4
Bandwidth (GHz)	6.9	5.0	5.3	4.0	7.9	0.6
NoiseFigure (dB)	0.5	2.27	0.8	4.4	0.42	8
S_{11} (dB)	-23.64	<-20.88	-11	-26	-16.3	-8
S_{22}(dB)	<-1.416	-4.46	-11.5	-19.5	-7.71	-15
S_{12}(dB)	-	-	-31	-26.4	-6.67	-
S_{21}(dB)	24.92	9.36	20	9.72	3.62	21
Power consumption (mW)	29.392	15	15	20.75	0.5	28

Table 1: Comparison table of DLNA

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