Behavior of Wideband Digital AGC for 16-QAM, 8-PSK Constellations & Two-Tone IMD

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Abstract— Digital Automatic Gain Control (AGC) is required to control the variations in amplitude of the signal to maintain a constant level at the output. Now-a-days in modern communication receivers mostly processing is done in digital domain. In this project, digital AGC is designed for wideband communication systems. Here the implementation of digital AGC is done in FPGA using Xilinx ISE software in VHDL (Very High Speed Integrated Circuit Hardware Description Language). Input from VSG is given to ADC of 14 bits resolution, thereafter power is calculated which provides the memory address for the LUT, in which attenuating factor is stored. Then the input signal is multiplied with the LUT output in multiplication block; to give constant output which is given to DAC of 16 bits and analysed in VSA. Finally the behavior of this Digital AGC is observed in QAM, PSK and Two-tone signals. Here the dynamic range obtained is around 45 dB to 50 dB.

Key words: Digital AGC, 16-QAM, 8-PSK Constellations, Two-Tone IMD

I. INTRODUCTION

The function of automatic gain control circuit is to automatically adjust the gain of variable gain amplifier (VGA) or programmable gain amplifier (PGA); so as to provide constant signal power for varying level of input signal.

The AGC function can be categorized in two ways as feedback & feedforward loop.

A. Feedback AGC

In this type of AGC loop, the output is sensed and the AGC loop moves it back; opposite to that of the signal direction. The schematic of feedback loop AGC is shown below. Here, VGA output signal peak is detected and compared with reference voltage. The output of comparator is the error signal; which is further filtered and integrated back to variable gain amplifier.

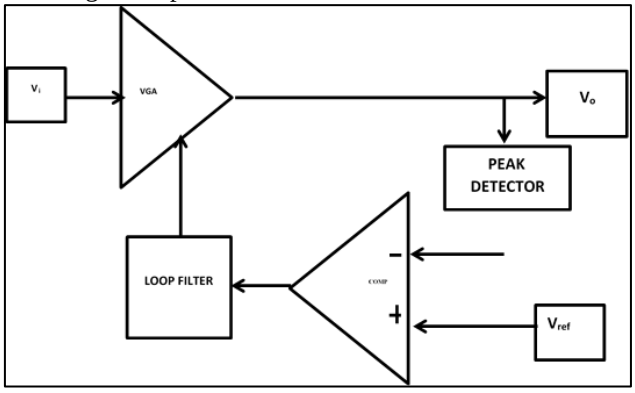

Fig. 1: Feedback AGC Architecture

B. Feed Forward AGC

In this type of AGC loop, the input of VGA is sensed and loop moves it forward in the signal direction, hence is called as feedforward loop. The schematic diagram of feedforward loop AGC is shown below. Here, the input signal's peak is detected and compared with reference voltage in a comparator circuit. The comparator generates the error signal which is then filtered and fed back to the VGA.

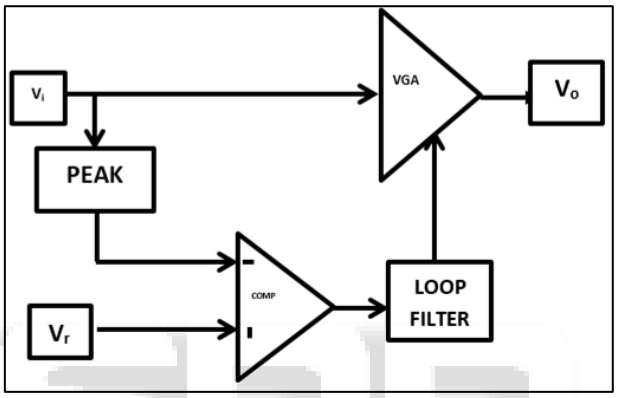

Fig. 2: Feedforward AGC Architecture

II. IMPLEMENTATION OF DIGITAL AGC

The board used for programming is Virtex-4 MB Development Board which has ADC (ADS5500) and DAC (5687). Internal clock available is 500MHz. Firstly, the input from the signal generator is given to ADC. Output of ADC is of 14 bits. Thereafter, power is calculated for the digital samples. This calculated power will be the address for the block memory in which look up table (LUT) is stored. LUT has attenuating factor stored for each power level. Corresponding to input power level, the corresponding attenuating voltage level is generated. This attenuating factor will then be multiplied with the output of ADC. So, the output of multiplier will be constant for certain input range called as dynamic range of AGC which in turn depends on the LUT. Finally the output of multiplier is given to DAC; which is analyzed using signal analyzer. The basic AGC circuit is shown below.

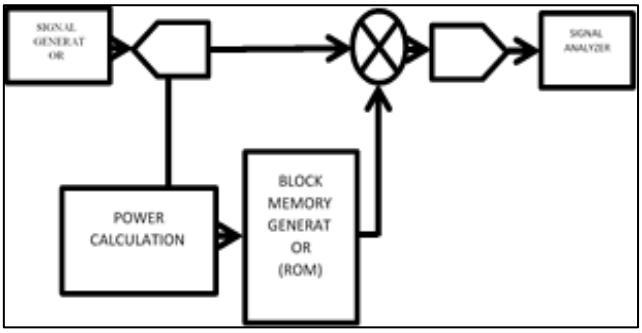

Fig. 3: AGC implementation

A. Power Calculation

Power calculation of signal is done in simple steps. Firstly, squaring of signal is done using multiplier. Thereafter, summation of 2^N samples is done; which is stored in the accumulator and finally divided by N samples. The calculated power is verified using Logic Analyzer. Using the calculated power for different inputs, the Look-up-table (LUT) is generated.

The mathematical form of power calculation is expressed below.

$$P(x)= \frac{1}{N} \sum_{N=0}^{N-1} x^2$$

Where,

P(x) = Signal power

x= Input signal from ADC

The block diagram of power calculation is shown below.

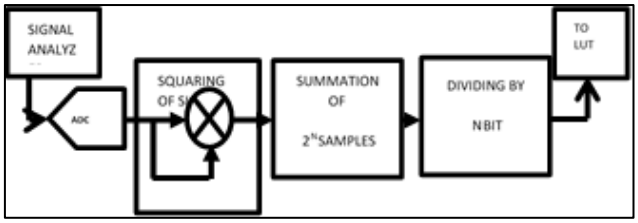

Fig. 4: Power Calculation

The dynamic range obtained for the basic AGC circuit is around 45dB. For an unmodulated signal, the AGC graph is shown below.

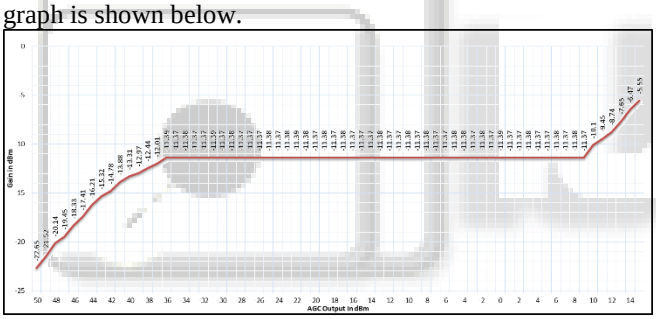

Fig. 5: AGC Graph of Unmodulated Signal

In the graph it is observed that till -36 dBm input power, the output is linear. After that increasing till 9dBm input power the output of AGC is constant in -11.37 $\pm$0.1 dBm. Thereafter power is increased with respect to input power.

III. BEHAVIOR OF AGC FOR DIFFERENT DATA RATES

For the modulated input signal, constellation diagram has been observed for 16 QAM and 8 PSK modulations; at different data rates. Constellation diagram represents the digital bits in terms of symbols where each symbol has magnitude and phase. In case of 16 QAM, there are 3 magnitude levels and 12 phase levels. It is observed that for low data rates the constellation is not clear in case of 16 QAM; while for high data rate it is near to ideal constellation.

This is attributed to the fact that in case of multi-level and multi-phase systems, at high data rates it is plotting the average symbol values as it cannot match with the different levels so fast; leading to fair constellation and at low data rates; it tries to match with each and every input symbol leading to poor constellation diagram.

The 16QAM constellation diagram output from vector signal analyzer of different data rates 1 ksps, 10 ksps, 100 ksps and 1 Msps with input power of 0 dBm which is in dynamic range of designed automatic gain control in fpga. Reference amplitude od VSG is 0 dBm, modulation mapping selected is 16 QAM.

Fig. 6: 16QAM Constellation for 1ksps

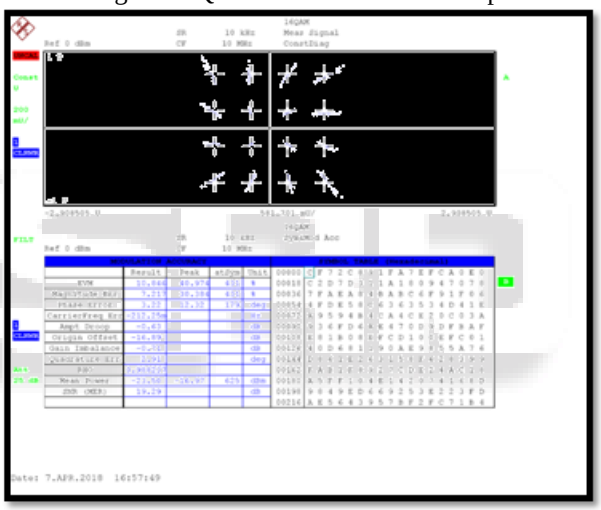

Fig. 7: 16QAM Constellation for 10ksps

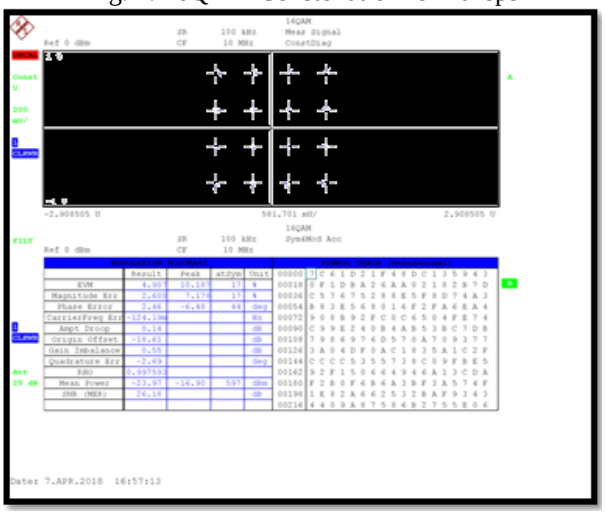

Fig. 8: 16QAM Constellation for 100ksps

Fig. 9: 16QAM Constellation for 1Msps

In 8 PSK, for high data rates; constellation is poor but for low data rates; it is near to ideal constellation. This is so because in 8 PSK there is only one amplitude level and 8 phase levels; in contrast to that of 16 QAM which is multi-level and multi-phase system. So, it is easy to match the incoming input data with ideal symbol locations in the constellation at low data rates as compared to high data rates.

Overall, error wise 8 PSK is better choice over 16 QAM because of less number of amplitude levels. The constellation diagram for 8 PSK modulation scheme at different data rates are shown below.

The 8PSK constellation diagram output from vector signal analyzer of different data rates 1 ksps, 10 ksps, 100 ksps and 1 Msps with input power of 0 dBm which is in dynamic range of designed automatic gain control in fpga. Reference amplitude of VSG is 0 dBm and modulation mapping selected is 8PSK.

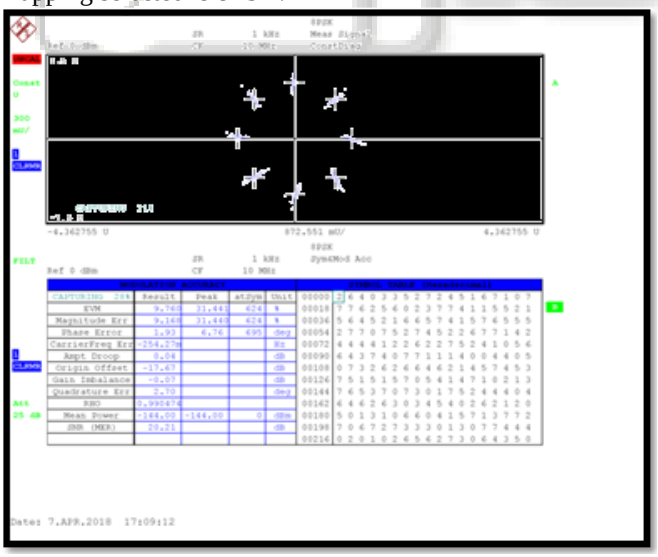

Fig. 10: 8PSK Constellation for 1ksps

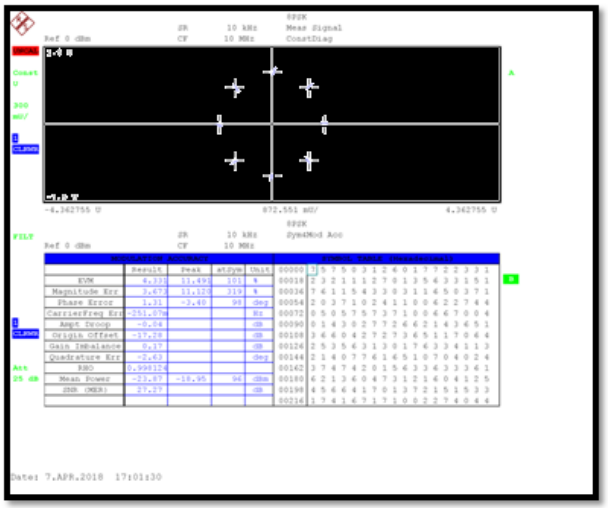

Fig. 11: 8PSK Constellation for 10ksps

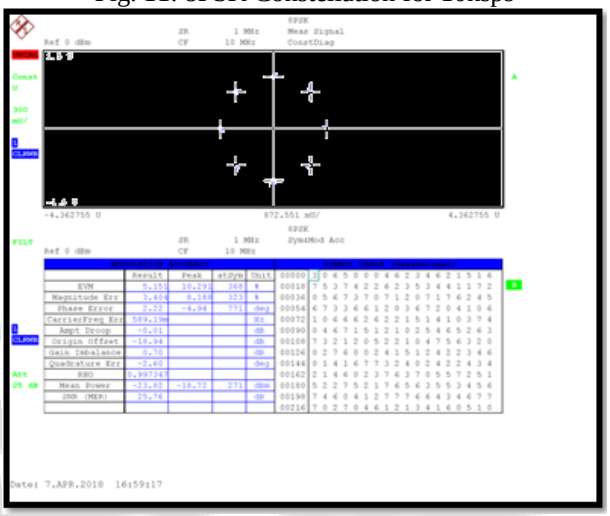

Fig. 12: 8PSK Constellation for 1Msps

IV. TWO-TONE IMD MEASUREMENT

Here, two tone modulated signal is given as the input. Intermodulation distortion (IMD) is observed with the variation in the frequency separation between the two tones/carriers. IMDs are generated because of the nonlinearity of the system. Other than IMDs, there are harmonic distortions, but they are of less concern as they usually fall out of the desired band. It is observed that as the frequency separation increases, IMDs level degraded. This happens so because as the frequency separation increases, time period of the message signal decreases thereby becoming more and more smaller than the time constant of AGC which is highly desirable. This in turn results in the better performance of AGC. In the below graph, IMDs are plotted against frequency separation for different time constant of the AGC. It is clear from the graph that for large time constant, the IMDs are poor; resulting in a better AGC system.

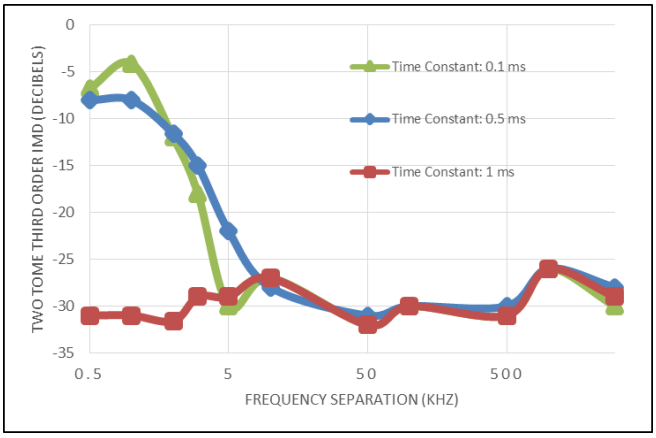

Fig. 13: Two Tone Third Order IMD Chart

V. CONCLUSION

Digital Automatic Gain Control (AGC) circuit has been implemented in FPGA kit using VHDL. The dynamic range achieved for the digital AGC is around 45dB and the time constant of AGC is 1ms. The two tone IMD measurement is performed to check the effect of frequency separation on IMDs. The AGC is performing better with small intermodulation distortion at large time constants against smaller ones as the message signal's time period is much smaller than the time constant of AGC. The other measurement is the effect of varying data rates on different modulation schemes like 8PSK and 16QAM. For 8PSK, at low data rates, constellation is near ideal but at high data rates it deteriorates, whereas in case of 16QAM, at low data rates, constellation is poor and at high data rates constellation is near ideal. This in turn is attributed to the fact that in multi-level, multi-phase system, it is difficult to match the incoming data rate with the multiple levels so it takes the average of the symbols, resulting in better constellation than low data rate in 16QAM. In single level system like 8PSK, case is opposite as it is easier to place the symbols in constellation at low data rate as compared to high data rates. Above all, single level systems are preferred because of the low probability of error.

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