Improvement of Power Quality by using Multi Converter Unified Power Quality Conditioner

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Abstract— This project presents a new unified power-quality conditioning system (MC-UPQC), capable of simultaneous compensation for voltage and current in multi-bus/multi-feeder systems. By using one shunt voltage-source converter (shunt VSC) and two or more series VSCs the configuration is made. The system can be applied to adjacent feeders to compensate for supply-voltage and load current imperfections on the main feeder and full compensation of supply voltage imperfections on the other feeders. The configuration will be designed as all converters are connected back to back on the dc side and share a common dc-link capacitor. Therefore, power can be transferred from one feeder to adjacent feeders to compensate for sag/swell and interruption. The proposed topology can be used for simultaneous compensation of voltage and current imperfections in both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected. The system is also capable of compensating for interruptions without the need for a battery storage system and consequently without storage capacity limitations. By the simulation the performance of MC-UPQC as well as the adopted control algorithm will be illustrated.

Key words: Power Quality, Multi Converter Unified Power Quality Conditioner (MC-UPQC)

I. INTRODUCTION

With increasing applications of nonlinear and electronically switched devices in distribution systems and industries, Power Quality (PQ) problems, such as harmonics, flicker, and imbalance have become serious concerns. In addition, lightning strikes on transmission lines, switching of capacitor banks, and various network faults can also cause PQ problems, such as transients, voltage sag/swell, and interruption. On the other hand, an increase of sensitive loads involving digital electronics and complex process controllers requires a pure sinusoidal supply voltage for proper load operation.

In order to meet PQ standard limits, it may be necessary to include some sort of compensation. Modern solutions can be found in the form of active rectification or active filtering. A shunt active power filter is suitable for the suppression of negative load influence on the supply network, but if there are supply voltage imperfections, a series active power filter may be needed to provide full compensation. In recent years, solutions based on Flexible AC Transmission Systems (FACTS) have appeared. The application of FACTS concepts in distribution systems has resulted in a new generation of compensating devices. A Unified Power Quality Conditioner (UPQC) is the extension of the Unified Power-Flow Controller (UPFC) concept at the distribution level. It consists of combined series and shunt converters for simultaneous compensation of voltage and current imperfections in a supply feeder.

Recently, multi converter FACTS devices, such as an Interline Power-Flow Controller (IPFC) and the Generalized Unified Power-Flow Controller (GUPFC) are introduced. The aim of these devices is to control the power flow of multiline or a sub network rather than control the power flow of a single line by, for instance, a UPFC.

When the power flows of two lines starting in one substation need to be controlled, an IPFC can be used. An IPFC consists of two series Voltage Source Converter (VSC)s whose dc capacitors are coupled. This allows active power to circulate between the VSCs. With this configuration, two lines can be controlled simultaneously to optimize the network utilization. The GUPFC combines three or more shunt and series converters. It extends the concept of voltage and power-flow control beyond what is achievable with the known two-converter UPFC. The simplest GUPFC consists of three converters one connected in shunt and the other two in series with two transmission lines in a substation. The basic GUPFC can control total five power system quantities, such as a bus voltage and independent active and reactive power flows of two lines. The concept of GUPFC can be extended for more lines if necessary. The device may be installed in some central substations to manage power flows of multiline or a group of lines and provide voltage support as well. By using GUPFC devices, the transfer capability of transmission lines can be increased significantly.

Furthermore, by using the multiline-management capability of the GUPFC, active power flow on lines cannot only be increased, but also be decreased with respect to operating and market transaction requirements. In general, the GUPFC can be used to increase the transfer capability and relieve congestions in a flexible way. This concept can be extended to design multiconverter configurations for PQ improvement in adjacent feeders. For example, the Interline Unified Power-Quality Conditioner (IUPQC), which is the extension of the IPFC concept at the distribution level, has been proposed in the IUPQC consists of one series and one shunt converter. It is connected between two feeders to regulate the bus voltage of one of the feeders, while regulating the voltage across a sensitive load in the other feeder. In this configuration, the voltage regulation in one of the feeders is performed by the shunt-VSC. However, since the source impedance is very low, a high amount of current would be needed to boost the bus voltage in case of a voltage sag/swell which is not feasible. It also has low dynamic performance because the dc-link capacitor voltage is not regulated.

In this project, a new configuration of a UPQC called the Multiconverter Unified Power-Quality Conditioner (MC-UPQC) is presented. The system is extended by adding a series-VSC in an adjacent feeder. The proposed topology

can be used for simultaneous compensation of voltage and current imperfections in both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected. The system is also capable of compensating for interruptions without the need for a battery storage system and consequently without storage capacity limitations.

II. LITERATURE SURVEY

Major research efforts in power quality were first conducted by H. Akagi and F.Z. Peng by using active filtering and active rectification. Even though by using active filtering and rectification power quality is not improved as expected.

As the new era started in Electrical Engineering, FACTS devices (the improved version of thyristor family) are replaced by active filters and active rectifiers, the quality of power further improved. This was explained in "UPFC: A new approach to control power", IEEE Trans. power Del., presented by L. Gyugyi in 1990's.The devices like UPFC, UPQC, IPFC, GUPFC and IUPQC are used to improve the power quality by compensating voltage and current, the power was compensated in one feeder through many lines.

In this project, a new configuration of a UPQC called the MC – UPQC device is presented which can further improves the quality of power. This was referred from IEEE paper "Multiconverter Unified Power Quality Conditioner System: MC – UPQC" by Hemid Reza Mohammedi in 2009. MC – UPQC which is a device will improves the quality of power up to maximum level in two feeders simultaneously. The description about MC – UPQC is described by Hemid Raza Mohammadi in IEEE paper which is a hand book published in 2009.

III. MODELLING OF PROPOSED MC-UPQC SYSTEM

The single-line diagram of a distribution system with an MC-UPQC is shown in Fig.

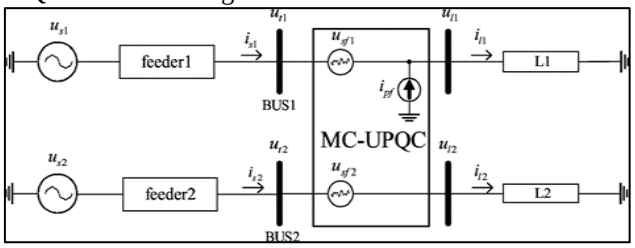


Fig. 1: Single-Line Diagram of a Distribution System with an MC-UPQC

As shown in figure.1, two feeders connected to two different substations supply the loads L_1 and L_2. The MC-UPQC is connected to two buses BUS_1 and BUS_2 with voltages of u_{t1} and u_{t2}, respectively. The shunt part of the MC-UPQC is also connected to load L_1 with a current of i_{l1}. Supply voltages are denoted by u_{s1} and u_{s2} while load voltages are u_{l1} and u_{l2} finally, feeder currents are denoted by i_{s1} and i_{s2} load currents are i_{l1} and i_{l2} Bus voltages u_{t1} and u_{t2} are distorted and may be subjected to sag/swell. The load L_1 is a nonlinear/sensitive load which needs a pure sinusoidal voltage for proper operation while its current is non-sinusoidal and contains harmonics. The load L_2 is a sensitive/critical load which needs a purely sinusoidal voltage and must be fully protected against distortion, sag/swell, and interruption. These types of loads primarily include production industries and critical service providers, such as medical centers, airports, or broadcasting centers where voltage interruption can result in severe economic losses or human damages.

A. MC–UPQC Structure

The internal structure of the MC–UPQC is shown in Fig...2. It consists of three VSCs (VSC_1, VSC_2, and VSC_3) which are connected back to back through a common dc-link capacitor.

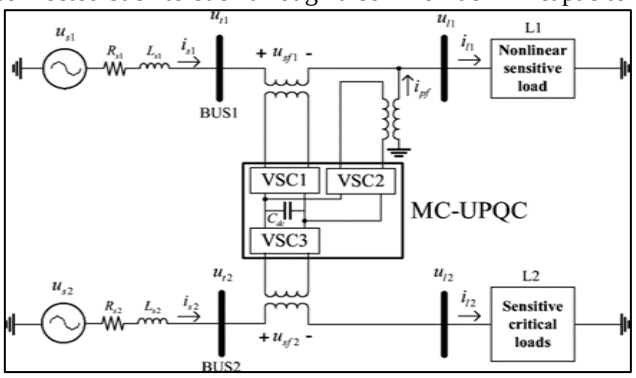


Fig. 2: Typical MC-UPQC used in a Distribution System

In the proposed configuration, VSC_1 is connected in series with BUS_1 and VSC_2 is connected in parallel with load L_1 at the end of $Feeder_1$. VSC_3 is connected in series with BUS_2 at the $Feeder_2$ end. Each of the three VSCs in Fig. 3 is realized by a three-phase converter with a commutation reactor and high-pass output filter as shown in Fig. 3.

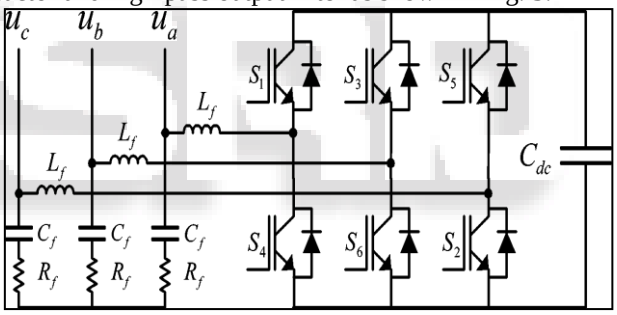


Fig. 3: Schematic Structure of a VSC

The commutation reactor (L_f) and high- pass output filter (R_f , C_f) connected to prevent the flow of switching harmonics into the power supply. As shown in Fig 2, all converters are supplied from a common dc-link capacitor and connected to the distribution system through a transformer.

Secondary (distribution) sides of the series-connected transformers are directly connected in series with BUS_1 and BUS_2, and the secondary (distribution) side of the shunt-connected transformer is connected in parallel with load L_1.

The aims of the MC-UPQC shown in Fig .2 are:

1) To regulate the load voltage (u_{l1}) against sag/swell and disturbances in the system to protect the nonlinear/sensitive load L_1,
2) To regulate the load voltage u_{l2} against sag/swell, interruption, and disturbances in the system to protect the sensitive/ critical load L_2,
3) To compensate for the reactive and harmonic components of nonlinear load current (i_{l1}).
4) In order to achieve these goals, series VSCs (i.e., VSC_1 and VSC_3) operate as voltage controllers while the shunt VSC (i.e., VSC_2) operates as a current controller.

IV. CONTROL STRATEGY

As shown in Fig.2, the MC-UPQC consists of two series VSCs and one shunt VSC which are controlled independently. The switching control strategy for series VSCs and the shunt VSC are selected to be sinusoidal pulse width-modulation (SPWM) voltage control and hysteresis current control, respectively. Details of the control algorithm, which are based on the d–q method, will be discussed later. Shunt-VSC: Functions of the shunt-VSC are:

1) To compensate for the reactive component of load L_1 current;
2) To compensate for the harmonic components of load L_1 current;
3) To regulate the voltage of the common dc-link capacitor.

Fig. shows the control block diagram for the shunt VSC. The measured load current (i_{l_dq0}) is transformed into the synchronous dq0 reference frame by using

$$i_{l\_dq0} = T_{abc}^{dq0} i_{l\_abc}. \quad \dots 1$$

$$T_{abc}^{dq0} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - 120^0) & \cos(\omega t + 120^0) \\ -\sin(\omega t) & -\sin(\omega t - 120^0) & -\sin(\omega t + 120^0) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad \dots 2$$

Where the transformation matrix is shown in eq(2), By this transform, the fundamental positive-sequence component, which is transformed into dc quantities in the d and q axes, can be easily extracted by low-pass filters (LPFs). Also, all harmonic components are transformed into ac quantities with a fundamental frequency shift.

$$i_{l\_d} = \bar{i}_{l\_d} + \tilde{i}_{l\_d} \quad 3$$

$$i_{l\_q} = \bar{i}_{l\_q} + \tilde{i}_{l\_q} \quad 4$$

Where, i_{l_d}, i_{l_q} are d-q components of load current, $\bar{i}_{l\_d}, \bar{i}_{l\_q}$ are dc components, and $\tilde{i}_{l\_d}, \tilde{i}_{l\_q}$ are the ac components of i_{l_d}, i_{l_q}. If i_s is the feeder current and i_{pf} is the shunt VSC current and knowing $i_s = i_l - i_{pf}$, then d–q components of the shunt VSC reference current are defined as follows:

$$i_{pf\_d}^{ref} = \tilde{i}_{l\_d} \quad 5$$

$$i_{pf\_q}^{ref} = i_{l\_q} \quad 6$$

Consequently, the d–q components of the feeder current are

$$i_{s\_d} = \tilde{i}_{l\_d} \quad 7$$

$$i_{s\_q} = 0 \quad 8$$

This means that there are no harmonic and reactive components in the feeder current. Switching losses cause the dc-link capacitor voltage to decrease. Other disturbances, such as the sudden variation of load, can also affect the dc link. In order to regulate the dc-link capacitor voltage, a proportional–integral (PI) controller is used as shown in Fig 4. The input of the PI controller is the error between the actual capacitor voltage u_{dc} and its reference value(u_{dc}^{ref}). The output of the PI controller $(ie., \Delta i_{dc})$ is added to the d component of the shunt-VSC reference current to form a new reference current as follows:

$$\begin{cases} i_{pf\_d}^{ref} = \tilde{i}_{l\_d} + \Delta i_{dc} \\ i_{pf\_q}^{ref} = i_{l\_q} \end{cases} \quad 9$$

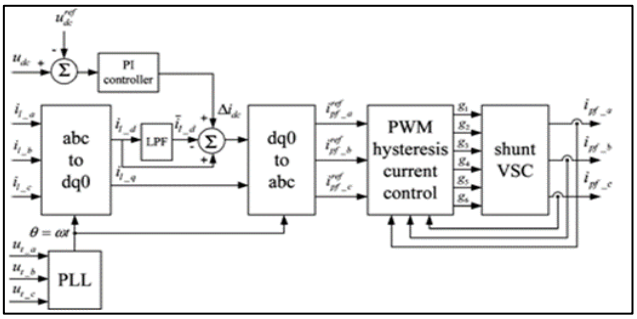


Fig. 4: Control Block Diagram of the Shunt VSC

As shown in Fig.4, the reference current in eq(9) is then transformed back into the abc reference frame.

By using PWM hysteresis current control, the output-compensating currents in each phase are obtained.

$$i_{pf\_abc}^{ref} = T_{dq0}^{abc} i_{pf\_dq0}^{ref}; (T_{dq0}^{abc} = T_{abc}^{dq0^{-1}}) \quad \dots 10$$

Series-VSC: Functions of the series VSCs in each feeder are:

1) To mitigate voltage sag and swell;
2) To compensate for voltage distortions, such as harmonics;
3) To compensate for interruptions (in Feeder2 only).

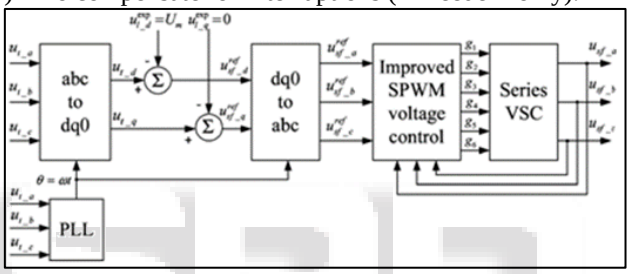


Fig. 5: Control block diagram of the series VSC

The control block diagram of each series VSC is shown in Fig 5. The bus voltage (u_{t-abc}) is detected and then transformed into the synchronous dq0 reference frame using

$$u_{t_{dq0}} = T_{abc}^{dq0} u_{t_{abc}} = u_{t1p} + u_{t1n} + u_{t10} + u_{th}. \quad 11$$

$$\text{Where, } \begin{cases} u_{t1p} = [u_{t1p\_d} \;\; u_{t1p\_q} \;\; 0]^T \\ u_{t1n} = [u_{t1n\_d} \;\; u_{t1n\_q} \;\; 0]^T \\ u_{t10} = [0 \;\; 0 \;\; u_{00}]^T \\ u_{th} = [u_{th\_d} \;\; u_{th\_q} \;\; u_{th\_0}]^T \end{cases} \quad 12$$

u_{t1p}, u_{t1n} and u_{t10} are fundamental frequency positive-, negative-, and zero-sequence components, respectively, and u_{th} is the harmonic component of the bus voltage. According to control objectives of the MC-UPQC, the load voltage should be kept sinusoidal with constant amplitude even if the bus voltage is disturbed. Therefore, the expected load voltage in the synchronous dq0 reference frame $u_{l\_dq0}^{exp}$ only has one value.

$$u_{l\_dq0}^{exp} = T_{abc}^{dq0} u_{l\_abc}^{exp} = \begin{bmatrix} u_m \\ 0 \\ 0 \end{bmatrix} \quad 13$$

Where the load voltage in the abc reference frame $u_{l_{abc}}^{exp}$ is

$$u_{l_{abc}}^{exp} = \begin{bmatrix} u_m \cos(\omega t) \\ u_m \cos(\omega t - 120^0) \\ u_m \cos(\omega t + 120^0) \end{bmatrix} \quad 14$$

The compensating reference voltage in the synchronous dq0 reference frame $u_{sf\_dq0}^{ref}$ is defined as

$$u_{sf\_dq0}^{ref} = u_{t\_dq0} - u_{l\_dq0}^{exp} \quad 15$$

This means u_{t1p_d} in eq(12) should be maintained at u_m while all other unwanted components must be eliminated. The compensating reference voltage is then transformed back into the abc reference frame. By using an improved SPWM voltage control technique the output compensation voltage of the series VSC can be obtained.

V. POWER-RATING ANALYSIS OF THE MC-UPQC

The power rating of the MC-UPQC is an important factor in terms of cost. Before calculation of the power rating of each VSC in the MC UPQC structure, two models of a UPQC are analyzed and the best model which requires the minimum power rating is considered. All voltage and current phasors used in this section are phase quantities at the fundamental frequency. There are two models for a UPQC - quadrature compensation (UPQC-Q) and inphase compensation (UPQC-P). In the quadrature compensation scheme, the injected voltage by the series- VSC maintains a quadrature advance relationship with the supply current so that no real power is consumed by the series VSC at steady state. This is a significant advantage when UPQC mitigates sag conditions. The series VSC also shares the volt ampere reactive (VAR) of the load along with the shunt-VSC, reducing the power rating of the shunt-VSC.

Fig 6 shows the phasor diagram of this scheme under a typical load power factor condition with and without a voltage sag.

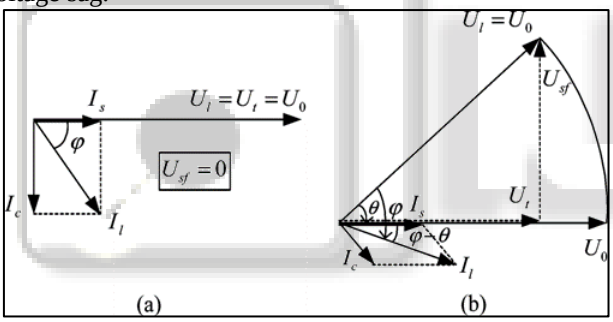


Fig. 6: Phasor Diagram of Quadrature Compensation. (A) Without Voltage Sag. (B) With Voltage Sag

When the bus voltage is at the desired value($U_l = U_t = U_0$), the series-injected voltage (U_{sf}) is zero Fig...6. (a). The shunt VSC injects the reactive component of load currentI_c, resulting in unity input-power factor. Furthermore, the shunt VSC compensates for not only the reactive component, but also the harmonic components of the load currentI_c. For sag compensation in this model, the quadrature series voltage injection is needed as shown in Fig. 6.(b)The shunt VSC injects I_c in such a way that the active power requirement of the load is only drawn from the utility which results in a unity input-power factor. In an in phase compensation scheme, the injected voltage is in phase with the supply voltage when the supply is balanced. By virtue of in phase injection, series VSC will mitigate the voltage sag condition by minimum injected voltage. The phasor diagram of Fig. explains the operation of this scheme in case of voltage sag.

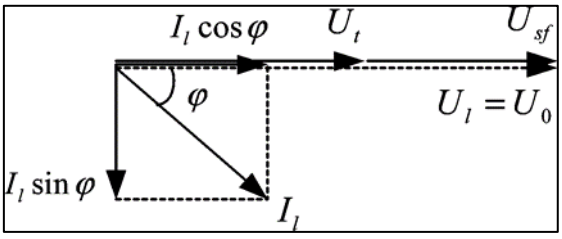


Fig. 7: Phasor Diagram of in phase Compensation (Supply Voltage Sag)

A comparison between in phase (UPQC-P) and quadrature (UPQC-Q) models is made for different sag conditions and load power factors. It is shown that the power rating of the shunt-VSC in the UPQC-Q model is lower than that of the UPQC-P, and the power rating of the series-VSC in the UPQC-P model is lower than that of the UPQC-Q for a power factor of less than or equal to 0.9. Also, it is shown that the total power rating of UPQC-Q is lower than that of UPQC-P where the VAR demand of the load is high.

As discussed in Section II, the power needed for interruption compensation in $Feeder_2$ must be supplied through the shunt VSC in Feeder1 and the series VSC in $Feeder_2$. This implies that power ratings of these VSCs are greater than that of the series one in Feeder1. If quadrature compensation in $Feeder_1$ and in phase compensation in $Feeder_2$ is selected, then the power rating of the shunt VSC and the series VSC (in $Feeder_2$) will be reduced. This is an important criterion for practical applications.

Based on the aforementioned discussion, the power-rating calculation for the MC-UPQC is carried out on the basis of the linear load at the fundamental frequency. The parameters in Fig. are corrected by adding suffix "1," indicating Feeder1, and the parameters in Fig. are corrected by adding suffix "2," indicating $Feeder_2$. As shown in Figs. 6 and 7, load voltages in both feeders are kept constant at U_0 regardless of bus voltages variation, and the load currents in both feeders are assumed to be constant at their rated values (i.e., I_{01} and I_{02} respectively)

$$U_{t1} = U_{t2} = U_0 \quad (16)$$

$$\begin{cases} I_{l1} = I_{01} \\ I_{l2} = I_{02} \end{cases} \quad (17)$$

The load power factors in $Feeder_1$ and $Feeder_2$ are assumed to be $\cos\varphi_1$ and $\cos\varphi_2$ and the per-unit sags, which must be compensated in $Feeder_1$ and $Feeder_2$, are supposed to be x_1 and x_2, respectively.

If the MC-UPQC is lossless, the active power demand supplied by $Feeder_1$ consists of two parts:

1) The active power demand of load in $Feeder_1$.
2) The active power demand for sag and interruption compensation in $Feeder_2$.

Thus, $Feeder_1$ current I_{s1} can be found as

$$U_{t1}I_{s1} = U_{t1}I_{t1}\cos\varphi_1 + U_{sf2}I_{l2}\cos\varphi_2 \quad (18)$$

$$(1 - x_1)U_0 I_{s1} = U_0 I_{01}\cos\varphi_1 + x_2 U_0 I_{02}\cos\varphi_2 \quad (19)$$

$$(1 - x_1)I_{s1} = I_{01}\cos\varphi_1 + x_2 I_{02}\cos\varphi_2 \quad (20)$$

$$I_{s1} = \frac{I_{01}\cos\varphi_1}{(1-x_1)} + \frac{x_2 I_{02}\cos\varphi_2}{(1-x_1)} \quad (21)$$

From Fig., the voltage injected by the series VSC in $Feeder_1$ and thus the power rating of this converter (S_{VSC1}) can be calculated as

$$U_{sf1} = U_{t1}\tan\theta = U_0(1 - x_1)\tan\theta \quad (22)$$

$$S_{VSC1} = 3U_{sf1}I_{s1} = 3U_0(1 - x_1)\tan\theta\left(\frac{I_{01}\cos\varphi_1}{(1-x_1)} + \frac{x_2 I_{02}\cos\varphi_2}{(1-x_1)}\right) \quad (23)$$

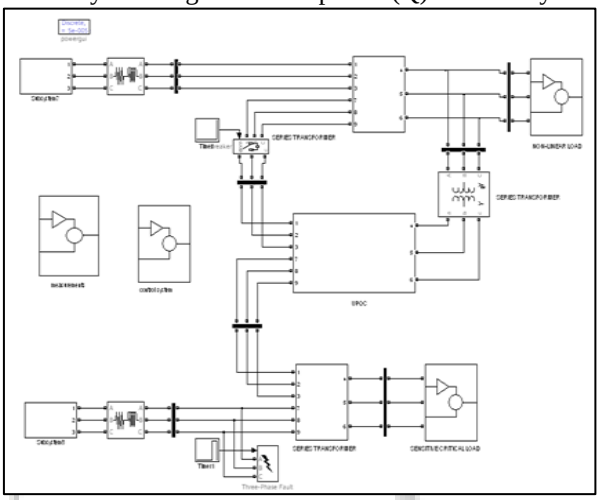
The shunt VSC current is divided into two parts:

1) The first part (i.e., I_{c1}) compensates for the reactive component (and harmonic components) of Feeder1 current and can be calculated from Fig. 6. as

$$I_{c1} = \sqrt{I_{l1}^2 + I_{s1}^2 - 2I_{l1}I_{s1}\cos(\varphi_1 - \theta)}$$

$$I_{c1} = \sqrt{I_{01}^2 + I_{s1}^2 - 2I_{01}I_{s1}\cos(\varphi_1 - \theta)} \quad \ldots .24$$

Where I_{s1} is calculated. This part of the shunt VSC current only exchanges reactive power (Q) with the system.



2) The second part provides the real power (P), which is needed for a sag or interruption compensation in Feeder$_2$. Therefore, the power rating of the shunt VSC can be calculated as

$$S_{VSC2} = 3U_{l1}I_{pf} = 3\sqrt{Q^2 + P^2}$$
$$= 3\sqrt{(U_{l1}I_{c1})^2 + (U_{sf2}I_{l2}\cos\varphi_2)^2}$$
$$= 3U_0\sqrt{I_{c1}^2 + (x_2 I_{02}\cos\varphi_2)^2} \quad \ldots 25$$

Where I_{c1} is calculated. Finally, the power rating of the series-VSC in Feeder$_2$ can be calculated. For the worst-case scenario (i.e., interruption compensation), one must consider

$x_2 = 1$. Therefore,

$$S_{VSC3} = 3U_{sf2}I_{l2} = 3x_2U_0I_{02} \quad \ldots 26$$

VI. MATLAB DESIGN OF MC-UPQC STUDY & RESULTS

Fig 8 Simulation diagram of MC-UPQC for showing results under distortion, sag/swell, upstream fault and load change

A. Distortion & Sag/Swell on the Bus Voltage

Let us consider that the power system in consists of two three-phase three-wire 380(v) (rms, L-L), 50-Hz utilities. The BUS1 voltage contains the seventh-order harmonic with a value of 22%, and the BUS2 voltage contains the fifth order harmonic with a value of 35%. The BUS1 voltage contains 25% sag between s and 20% swell between. The BUS2 voltage contains 35% sag between and 30% swell between. The nonlinear/sensitive load L1 is a three-phase rectifier load which supplies an RC load of 10 and 30 F. Finally, the critical load L2 contains a balanced RL load of 10 and 100 mH.

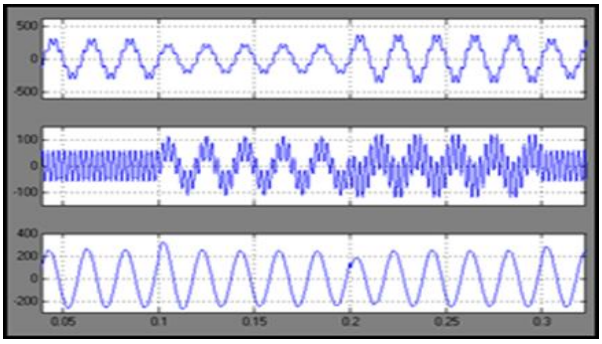


Fig. 9: BUS$_1$ Voltage, Series Compensating Voltage, and load Voltage in Feeder$_1$.

Similarly, the BUS2 voltage, the corresponding compensation voltage injected by VSC3, and finally, the load L2 voltage are shown in Fig. 10. As shown in these figures, distorted voltages of BUS1 and BUS2 are satisfactorily compensated for across the loads L1 and L2 with very good dynamic response.

The MC–UPQC is switched on at 0.02 s. The BUS1 voltage, the corresponding compensation voltage injected by VSC1, and finally load L1 voltage are shown in Fig. 9 In all figures, only the phase waveform is shown for simplicity.

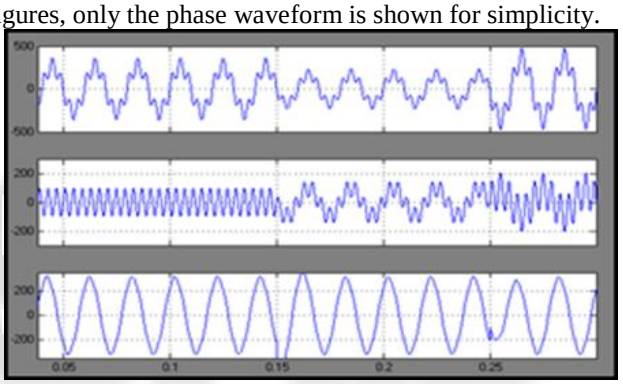


Fig. 10: BUS$_2$ voltage, series compensating voltage, and load voltage in Feeder$_2$

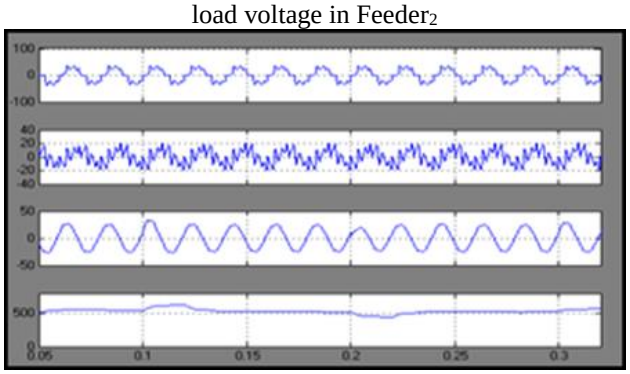


Fig. 11: Nonlinear load current, compensating current, Feeder$_1$ current, and capacitor voltage.

The nonlinear load current, its corresponding compensation current injected by VSC2, compensated Feeder1 current, and, finally, the dc-link capacitor voltage are shown in Fig. 6.4. The distorted nonlinear load current is compensated very well, and the total harmonic distortion (THD) of the feeder current is reduced from 28.5% to less than 5%. Also, the dc voltage regulation loop has functioned properly under all disturbances, such as sag/swell in both feeders.

B. Upstream Fault on Feeder2

When a fault occurs in Feeder2 (in any form of L-G, L-L-G, and L-L-L-G faults), the voltage across the sensitive/critical load L2 is involved in sag/swell or interruption. This voltage imperfection can be compensated for by VSC2.

In this case, the power required by load L2 is supplied through VSC2 and VSC3. This implies that the power semiconductor switches of VSC2 and VSC3 must be rated such that total power transfer is possible. This may increase the cost of the device, but the benefit that may be obtained can offset the expense.

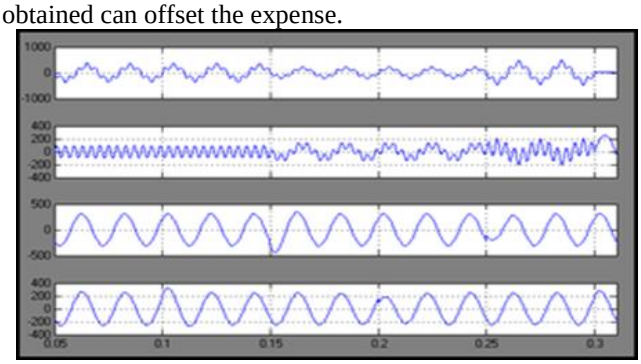


Fig. 12: Simulation Results for an Upstream Fault on Feeder$_2$: BUS$_2$ Voltage, Compensating Voltage, and loads L$_1$ and L$_2$ Voltages.

The performance of the MC-UPQC under a fault condition on Feeder2 is tested by applying a three-phase fault to ground on Feeder2 between s. Simulation results are shown in Fig.12

In the proposed configuration, the sensitive/critical load on Feeder2 is fully protected against distortion, sag/swell, and interruption. Furthermore, the regulated voltage across the sensitive load on Feeder1 can supply several customers who are also protected against distortion, sag/swell, and momentary interruption. Therefore, the cost of the MC-UPQC must be balanced against the cost of interruption, based on reliability indices, such as the customer average interruption duration index (CAIDI) and customer average interruption frequency index (CAIFI). It is expected that the MC-UPQC cost can be recovered in a few years by charging higher tariffs for the protected lines.

C. Load Change

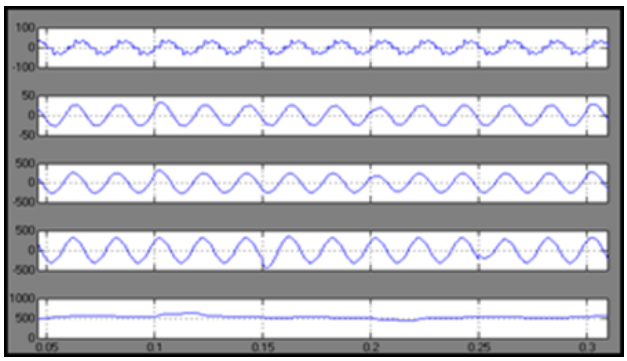


Fig. 13: Simulation results for load change: nonlinear load current, Feeder$_1$ current,

To evaluate the system behavior during a load change, the nonlinear load L1 is doubled by reducing its resistance to half at 0.5 s. The other load, however, is kept unchanged. The system response is shown in Fig. 6.6. It can be seen that as load L1 changes, the load voltages and remain undisturbed, the dc bus voltage is regulated, and the nonlinear load current is compensated. Load L$_1$ voltage, load L$_2$ voltage, and dc-link capacitor voltage.

D. Unbalance Voltage

The control strategies for shunt and series VSCs, which are introduced in Section II, are based on the – method. They are capable of compensating for the unbalanced source voltage and unbalanced load current. To evaluate the control system capability for unbalanced voltage compensation, a new simulation is performed. In this new simulation, the BUS2 voltage and the harmonic components of BUS1 voltage are similar to those given in Section IV. However, the fundamental component of the BUS1 voltage is an unbalanced three-phase voltage with an unbalance factor of 40%. This unbalance voltage is given by

$$Ut\,1,\ fundamenta\ \ l = \begin{bmatrix} 0.31\cos(\omega t + 46^0) \\ 0.31\cos(\omega t + 106^0) \\ 0.155\cos(\omega t + 210^0) \end{bmatrix}$$

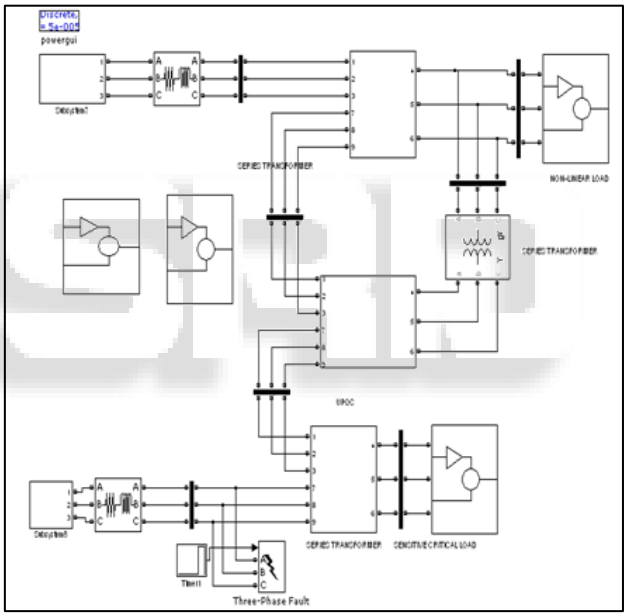


Fig. 14: Simulation Diagram of MC-UPQC for Showing Results in Unbalanced Condition

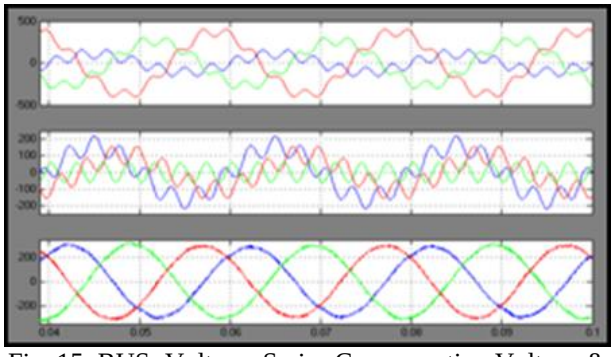


Fig. 15: BUS$_1$ Voltage, Series Compensating Voltage & Load Voltage in Feeder$_1$ under Unbalanced Source Voltage

The simulation results for the three-phase BUS1 voltage, series compensation voltage, and load voltage in feeder 1 are shown in Fig. 6.8. The simulation results show that the harmonic components and unbalance of under

unbalanced source voltage for by injecting the proper series voltage. In this figure, the load voltage is a three-phase sinusoidal balance voltage with regulated amplitude.

VII. CONCLUSION

In this project, a new configuration for simultaneous compensation of voltage and current in adjacent feeders has been proposed. The new configuration is named multi-converter unified power-quality conditioner (MC-UPQC). Compared to a conventional UPQC, the proposed topology is capable of fully protecting critical and sensitive loads against distortions, sags/swell, and interruption in two-feeder systems. The idea can be theoretically extended to multibus/multifeeder systems by adding more series VSCs. The performance of the MC-UPQC is evaluated under various disturbance conditions and it is shown that the proposed MC-UPQC offers the following advantages:

1) Power transfer between two adjacent feeders for sag/swell and interruption compensation;
2) Compensation for interruptions without the need for a battery storage system and, consequently, without storage capacity limitation;
3) Sharing power compensation capabilities between two adjacent feeders which are not connected.

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