Implementation of Minimum Delay and Low Power 32 Bit Arithmetic Logic Unit

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Abstract— In this paper VHDL implementation of 64-bit arithmetic logic unit is presented. The design was implemented using VHDL Xilinx Synthesis tool ISE 14.7 and targeted for virtex4 device. ALU was designed to perform arithmetic operation and logical operations such as addition, subtraction using 64-bit fast adder, logical operations such as AND, OR, XOR and NOT, NOR, NAND operations. ALU consist of two input registers to hold the data during operation, one output register to hold the result of operation. The maximum propagation delay is 33.468ns and power dissipation is 0.166nW.

Key words: Arithmetic Logic Unit, VHDL

I. INTRODUCTION

Recently, high performance digital signal processors have appeared on ASIC market, because of the increasing demands for multimedia data processing. Specially, a DSP core is one of a key component in the area of telecommunication, voice, video, three dimension graphics and so on. As shown in Fig. 1, a DSP core is composed of an arithmetic logic unit (ALU), memory unit, controller unit, and I/O unit. Further, the ALU of a DSP core is generally composed of an adder, multiplier and shifter. Thus, an ALU has a great role to improve the characteristic of DSP core. This paper describes a design methodology of 32-bit ALU for a DSP core that has a low-power consumption and high speed operation. In order to obtain a low power and high speed characteristics, therefore, novel architectures of adder, multiplier, and shifter with an adaptive leaf-cell based layout technique are proposed. In general, a leaf-cell based layout means a strong regular architecture with a basic cell library [1–[3]. However, it has some drawbacks that the chip area is somewhat larger and the power consumption is bigger than those of a full-custom layout are. On the contrary, the full-custom layout technique has a small chip area and a low power consumption, while it takes many hours. Thus we propose an adaptive leaf-cell based layout that has the advantages of the conventional leaf-cell layout and the full-custom layout. The contents of the paper are as follows. In the second section, a 64-bit conditional select adder with adaptive regular multiplexers is discussed. The most optimised data compressors and a novel compound logic for the design of a 32 £ 32-bit multiplier are described in the third section. In the fourth section, a 32-bit barrel shifter with a pre-mask decoder is discussed. An adaptive leaf-cell based layout generation process and experimental results are described in the fifth section. Finally, the conclusions are summarized in the sixth section.

II. DESIGN OF 32 BIT ALU

In our project "Design and Implementation of a 32-bit ALU on Xilinx FPGA using VHDL" we have designed and implemented a 32 bit ALU. Arithmetic Logic Unit is the part of a computer that performs all arithmetic computations, such as addition and subtraction, increment, decrement, shifting and all sorts of basic logical operations. The ALU is one component of the CPU (Central Processing Unit). Here, using VHDL we have designed a 32 bit ALU which can perform the various arithmetic operations of Addition, Subtraction, Increment, Decrement, Transfer, logical operations such as AND, OR, XOR, NOT and also the shift operation. All the above mentioned operations are then verified to see whether they match theoretically or not. The above given waveforms show that they match completely thereby verifying our results. Using VHDL we have designed a 32 bit ALU which can perform the various arithmetic operations of Addition, Subtraction, Increment, Decrement, Transfer, logical operations such as AND, OR, XOR, NOT and also the shift operation. This area efficient adder consume very less area about 1% and only 193 LUTs used out of 10944 .Here the RTL coding is done first using a VHDL and simulation is will be carried out by using ISIM 14.1.These area-efficient applications. By introducing operation of ALU better performance is acquire in terms of area. This work can be extended for the realization of the 128-Bit ALU and there is a extent for VLSI application32 bit ALU consists of an arithmetic unit, a logic unit, a shift unit, clock gating unit and an output multiplexer.

Where c_in represented as input clock of 32 bit ALU and i_a(31:0) represented as input of 32 bit ALU and i_b(31:0) represented as input of 32 bit ALU.

III. ALU IMPLEMENTATION

Execution of 32 bit ALU Which Perform Add/ Sub MUX And Shift using Xilinx 14.1 and simulator has commend out by I-Sim 14.1e tool. Shown in figure 7.1

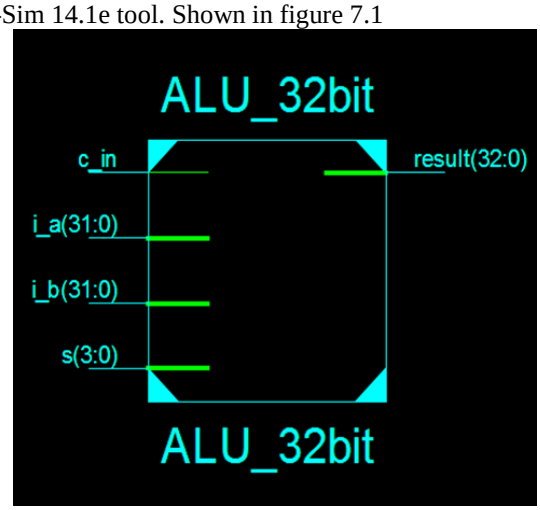

Fig. 1: RTL View of 32 Bit ALU

IV. 32 BIT ARITHMETIC UNIT

The Arithmetic unit performs 7 operations such as addition, addition with carry, subtraction, subtraction with borrow, increment, decrement, transfer. The circuit consists of a 32 bit parallel adder and thirty two numbers of single bits 4:1 multiplexer. A and B is a 32 bit input and the output is 33 bit result, there is 2 common selection lines S0 and S1, Cin is carry input of the parallel adder and the carry out is Cout.

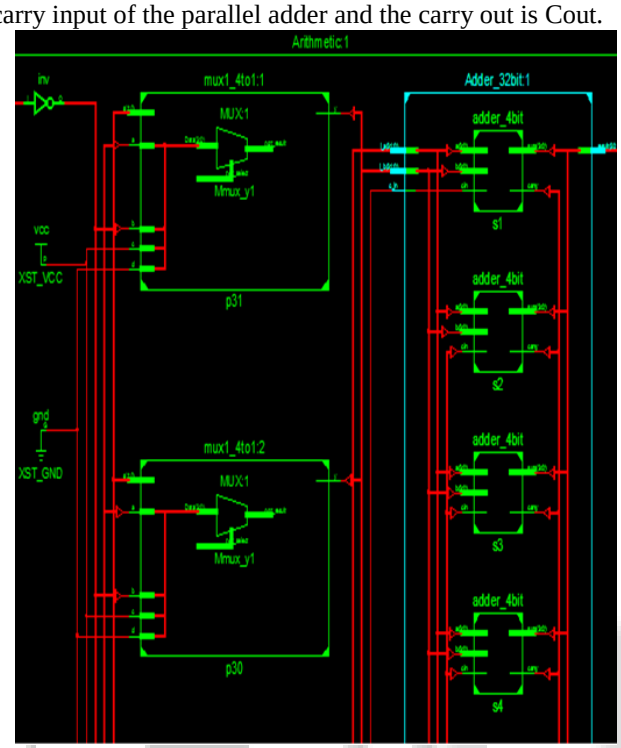

Fig. 2: RTL View of 32 Bit Arithmetic Unit

V. 32 BIT LOGIC UNIT

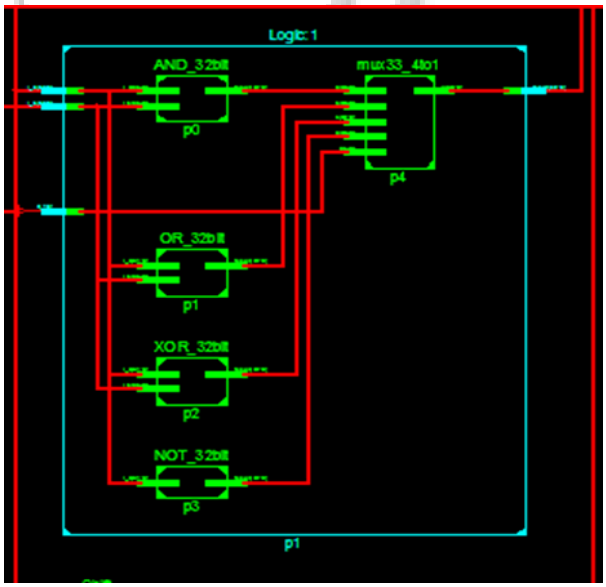

Fig. 3: RTL View of 32 Bit ALU

A Logic component does the subsequent undertaking: Logic AND, Logic OR, Logic XOR and Logic NOT operation. We will design a logic unit that can perform the four basic logic micro-operations: OR, AND, XOR and Complement, because from these four micro-operations, all other logic micro-operations can be derived. A one-stage logic unit for these four basic micro-operations is shown in the Fig. 7..3 The logic unit consists of four gates and a 4:1 multiplexer 32-bit ADDER, SUBTRACTOR, OR, AND, NOT, XOR,

VI. 32 BIT SHIFTER UNIT

Shifter unit is used to perform logical shift micro-operation. The shifting of bits of a register can be in either direction- left or right. A combinational shifter component can be constructing as Fig. 7. 4 The satisfied of a record that has to be shifted primary placed on top of common bus. This circuit uses no clock pulse. When the uneven unit is activated the register is shifted left or right according to the selection unit. For a shift unit of 32-bit, the output will be of 33-bit with 33th bit to be the outgoing bit

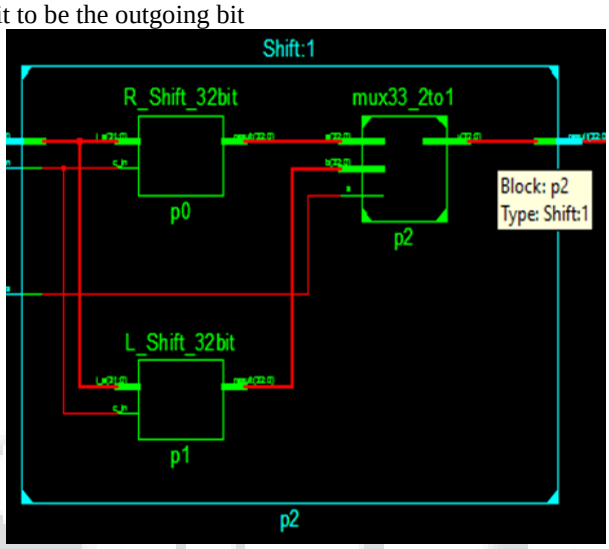

Fig. 4: RTL View of 32 Bit Shifter Unit

A. 32-Bit Arithmetic and Logical Unit

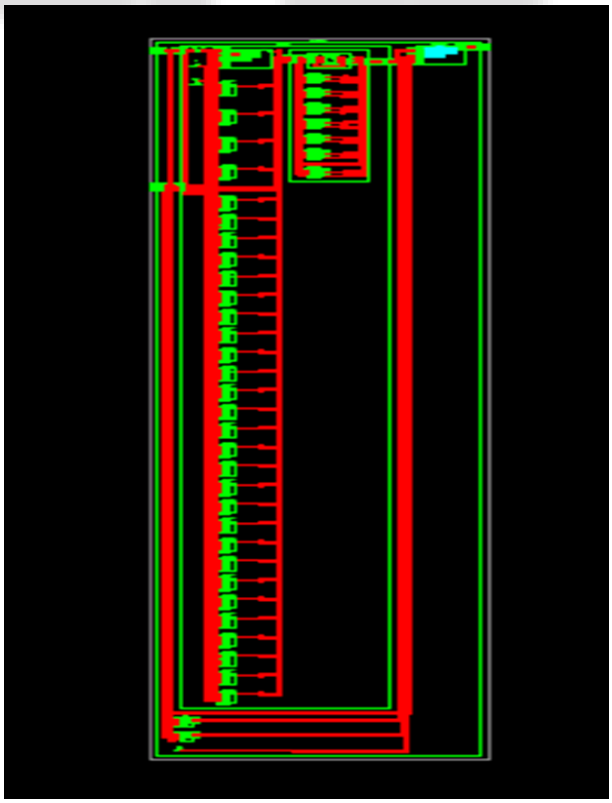

Fig. 5: RTL View of 32 Bit Logic and Arithmetic Unit

The approach used here is to split the ALU into three modules, one Arithmetic, one Logic and one Shift module. The arithmetic, logic and shifter units initiate previous can be mutual addicted to ALU by means of common assortment lines. The shift micro-operations are often performed in a separate unit, but sometimes the shifter unit made part of overall ALU. Since the ALU is composed of three units, namely Arithmetic, Logic and Shifter Units. For 32-bit ALU a 33 bit 4:1 MUX is needed. A particular arithmetic or logic or shift operation is selected according to the selection inputs S0 and S1. The final bit produced of the ALU is resolute with the place of multiplexers through collection lines S2 and S3. The function table for the ALU is shown in figure 5

VII. SIMULATION PROCESS AND RESULTS

In this work, Xilinx and I-sim tools are used for timing analysis and synthesis. The simulation output designed for 32-bit ALU is obtainable. Subsequent to verifying the building block diagram, the performance of 32-bit ALU is checked by simulation process shown in figure 6

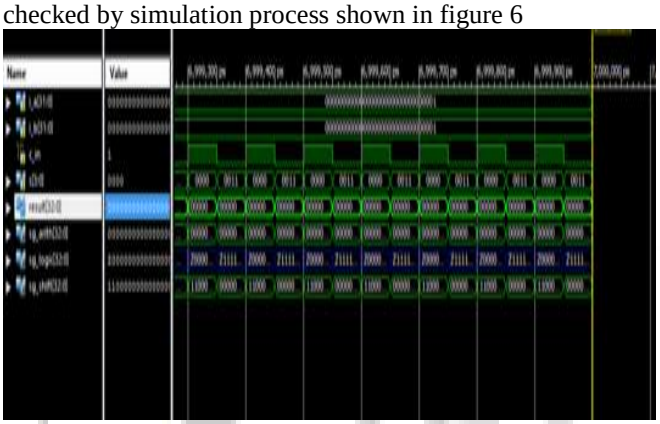

Fig. 6: Simulation View of 32 Bit Logic and Arithmetic Unit

VIII. CONCLUSION

This area efficient adder consume very less area about 1% and only 193 LUTs used out of 10944 .Here the RTL coding is done first using a VHDL and simulation is will be carried out by using ISIM 14.1.These area-efficient applications. By introducing operation of ALU better performance is acquire in terms of area. This work can be extended for the realization of the 128-Bit ALU and there is an extent for VLSI application32 bit ALU consists of an arithmetic unit, a logic unit, a shift unit, clock gating unit and an output multiplexer.

Design	Delay (Ns)	Bit	Power[Nw]
Design [1]	89.62	4 bit	33
Design [2]	45.2	8 bit	2.03
Design[3]	58.42	4 bit	1.09
Proposed Design	33.468ns	32 bit	0.166

Table 1: Comparison Result of different ALU Design

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