# Review Work on XOR Logic Gate Design using MOSFET

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*Abstract*— Full Adder is one of the smallest unit used in the complex data processing to perform fast arithmetic operations. The main aim of this paper is a design of systematic cell design methodology (SCDM) based XOR gate with three input. The XOR gate is an absolutely necessary primitive in the design of full adder cell for sum generation. Intension behind a novel SCDM based design is to improve speed and reduce power dissipation. Traditional dynamic N-channel FET, dynamic P-channel FET and new hybrid type systematic cell design methodology (SCDM) is designed and compare with proposed on the basis of following parameter like propagation delay, average power consumption, energy consumption, and layout area. It is observed that the new design has lower power dissipation, lower energy consumption, less delay and small layout area.

***Key words:*** Power-Delay-Product; Hybrid CMOS Logic; Transmission Gate; Layout Area; XOR/XNOR Gate

## I. INTRODUCTION

A XOR gate is one of the imperative building blocks in the formation of a full adder, full subtractor as well as a comparator [1-6]. With technology scaling, power consumption has turned out to be the most crucial concern of all design constraints in recent years [7-11]. In the past, processor speed, circuit speed, area, performance, cost and reliability were of primary interest while power consumption was attributed a secondary concern. However, with escalating eminence in portable and wireless communications systems, power consumption is being given equal importance in prevailing time. High performance processors consume intense power which consequently increases the cost related with packaging and cooling. Moreover, high power systems frequently run hot increasing the temperature thus having a tendency to aggravate various Silicon failure approaches such as electromigration, thermal runaway, decrement in transconductance, junction diffusion, threshold voltage shift, electrical parameter shift, electrostatic discharge (ESD), package related failure, electrical over-stress (EOS) and silicon interconnect failure [12]. It has been determined every $10^0$ upsurge in temperature nearly doubles the failure rate thereby disturbing the reliability. In this perspective, peak power consumption is a vital design issue because it resolves the thermal as well as electrical confines of designs, influences the system cost, size, weight, and prescribes the battery type, constituent in conjunction with system packaging and heat sinks. Additionally, peak power consumption exacerbates the resistive and inductive voltage drop tribulations. From the biological point of vision, meagre heat will be propelled into rooms provided power dissipation of electronic systems is abridged. Also, fewer electricity will be consumed which as an upshot will have an assenting effect on the global environment.

The XOR gate is one of the most important components of arithmetic and logic unit used in microprocessor. This plays an important role in SoC (silicon on chip) to design ALU in small die area that reduce manufacturing cost. This system inbuilt ALU occupy more area on silicon chip that dissipate more heat and elevate the temperature of chip. This thing degrades the performance of system. In order to save the chip heat sink is needed that release the internal heat to external environment. As the operating frequency of dynamic XOR improves, dynamic power consumption becomes dominant that introduce heating problem as mentioned above. To overcome this problem, dynamic XOR gate proposed with minimum delay and smaller power consumption.

## II. PREVIOUS WORK

LPHS-FA stands for low power and high speed full adder, which is based on hybrid logic. LPHS-FA[13] schematic shown in Fig. 1, demonstrates low-power and high-speed advantages, and merely requires 15 MOSFETs to implement.

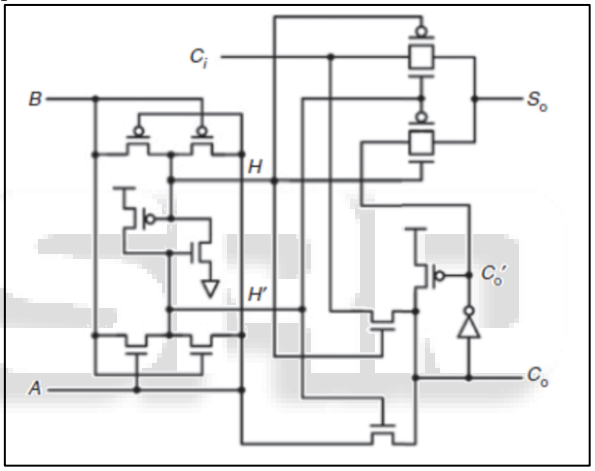


Fig. 1: Circuit schematic of LPHS-FA[13]

The transmission-gates CMOS adder (TG-CMOS)[14], it is based on transmission gates and has 20 transistors. It consumes more power. Next is 18TnewFA[15] is based on 18T and consumes more power.

Work on SCDM based XOR gate can be divided into two categories as they are extracted from the topic: 1) traditional three input XOR gate and 2) its operating methodologies. Cell design methodology has been presented to design some limited functions, such as two-input XOR/XNOR and carry–inverse carry in the hybrid-CMOS style [16-18]. The predominant results persuade us to improve CDM through two stages: 1) generating more complex functions and 2) rectifying some remaining flaws. The flaws in previously published CDM include containing some manual steps in the design flow and generating a large number of designs in which the predominant ones would be determined after the completion of simulations. Therefore, in the first stage, a three-input XOR/XNOR as one of the most complex and all-purpose three-input basic gates in arithmetic circuits have been chosen. If the efficiency of the circuits is confirmed in such a competitive environment, it can show the strength of the methodology. In the second stage, CDM is matured as systematic CDM (SCDM) in

 

designing the three-input XOR/XNORs for the first time. It systematically generates elementary basic cell (EBC) using binary decision diagram (BDD), and wisely chooses circuit components based on a specific target. This takes place when the mentioned features are not considered in the CDM. Therefore, after the systematic generation, the SCDM considers circuit optimization based on our target in three steps: 1) wise selection of the basic cell; 2) wise selection of the amend mechanisms; and 3) transistor sizing. It should be noted that BDD can be utilized for EBC generation of other three-input functions. We consider the power-delay product (PDP) as the design target. It stands as a fair performance metric, precisely involving portable electronic system targets. The motivation to use this methodology is the presence of some unique features and the ability to produce some efficient circuits that enjoy all these advantages.

The SCDM divides a circuit structure into a main structure and optimization-correction mechanisms. In the main structure, it considers features including the least number of transistors in critical path, fairly balanced outputs, being power ground- free, and symmetry. The mechanisms have the duty of completing the functionality of the circuits, avoiding any degradation on the output voltage, and increasing the driving capability.

The dynamic consumption optimization comes from the fact of well-balanced propagation delay. This feature is advantageous for applications in which the skew between arriving signals is critical for proper operation, and for cascaded applications to reduce the chance of making glitches [2]. Power-ground-free main structure leads to power reduction.

The degradation in all output voltage swing can thus be completely removed, which makes the design sustainable in low *V*DD operations and low static power dissipation. The methodology has high flexibility in target and systematically considers it in the three design steps. This can lead to efficient circuits in terms of performance, power, power delay product (PDP), energy delay product(EDP), layout area.

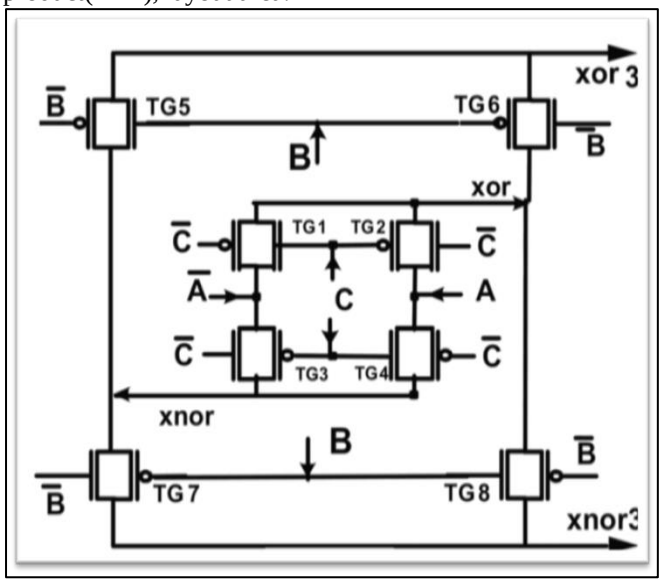


Fig. 2: Three input and 16T XOR/XNOR using transmission gate(XO4)[20]

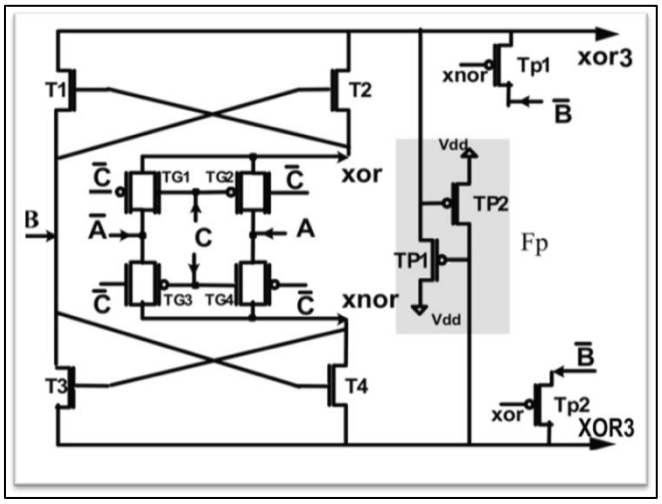


Fig. 3: Three input and 16T XOR/XNOR using transmission gate (XO7)[20]

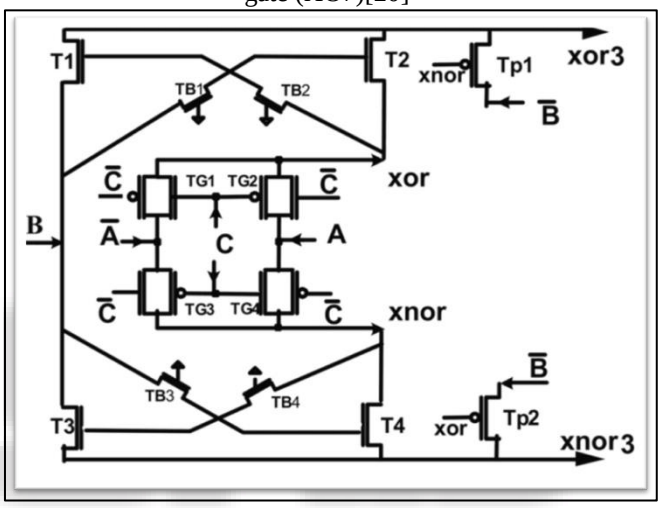


Fig. 4: Three input and 18T XOR/XNOR using transmission gate (XO10)[20]

The fast evolution of microelectronics fabrication processes demands a new cell library generation or a library technology migration. The well-organized systematic methodology leads to automated flow, which can reduce design time and costs, provide consistency in the cell library generation process, increase the range of simulation capabilities at the characteristics step, as well as minimize the risk of errors [17, 19]. Recently published article on hybrid type systematic cell design methodology (SCDM) applied on three circuit as shown in Fig.2, Fig.3 and Fig..4. all three circuit have six inputs (A, B, C, compliment of A, compliment of B and compliment of C) and two outputs (XOR and its outputs).

## III. Implementation Results and Comparisons

To evalute the performance of XOR/XNOR gate, it is necessary to study the timing analysis of proposed design under similar technology and supply voltage with different design. We have performed complete study using Hspice EDA Tool [21]. To investigate and compare the performance of different XOR gate such as LPHSFA, TF, 18TnewFS, XO4, XO7 and XO10, whose excellence have been confirmed in [13] [22] and [4, 23, 24]. Therefore, an approximately fair comparison will take place by selecting

 

them. Table-1 prasents that XO4[20], XO7[20] and XO10[20] technique have least PDP and delay than other existing conventional LPHS-FA, 18TnewFS and TF technique.

| Circuits | Average PDP (fJ) | Average Power (µW) | Average Delay (ns) | Area($\mu m^2$) |
|---|---|---|---|---|
| LPHS-FA | 0.91 | 3.41 | 0.38 | NA |
| TF | 0.52 | 2.79 | 0.23 | 18.34 |
| 18TnewFS | 0.52 | 2.75 | 0.24 | 20.03 |
| XO4 | 0.42 | 3.07 | 0.22 | 13.61 |
| XO7 | 0.47 | 3.17 | 0.19 | 17.37 |
| XO10 | 0.50 | 2.99 | 0.19 | 20.45 |

Table 1: Comparison of base paper results at 130nm technology [25]

## IV. CONCLUSION

The MOSFET based XOR/XNOR gates are extensively employed in portable modern high performance data processing units because of high speed and controllable evaluation by clock node, but they suffer from high power consumption and input signal skew. From the above analysis it can be concluded that SCDM based XOR gate circuit has got better performance in term of layout area, propagation time delay and average power comparatively LPHSFA, TF, XO4, XO7 and XO10. It shows that SCDM approach of full adder design is better for complex data processing application.

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