FPGA Implementation of 16*16 Vedic Multiplier in VHDL Environment

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Abstract— A high speed processor depends greatly on the multiplier in most digital signal processing system as well as in general processor. Currently the speed of the multipliers is limited by the speed of the adders used for partial product addition. It is an ancient methodology of Indian mathematics as it contains 16 SUTRAS (formulae). A high speed complex 16 *16 multiplier design by using urdhvatiryakbhyam sutra is presented in this paper. By using this sutra the partial products and sums are generated in one step which reduces the design of architecture in processors. It can be implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform (FFT) filtering and in microprocessors. By using this method we reduce the propagation delay in comparison with array based architecture and parallel adder based implementation which is most commonly used architecture.

Key words: FPGA, FFT, DSP, RTL, EDA

I. INTRODUCTION

With the latest advancement of VLSI technology the demand for portable and embedded digital signal processing (DSP) systems has increased efficiently. Multipliers are key components of many high performance systems such are FIR filters, Microprocessors, Digital Signal Processors etc. For higher order multiplications, a large number of adders or components are used. Vedic mathematics is the name given to the ancient system of mathematics which was rediscovered from the Vedas. In compare to conventional mathematics Vedic mathematics is simpler and easy to understand. Swami Bharati Krishna Tirthaji Maharaj (1884-1960), re-introduced the concept of ancient system of Vedic mathematics. The word 'Vedic' is resultant from the word 'Veda 'which means the store-house of all knowledge. Vedic mathematics includes sixteen-sutras or formulae and thirteen sub-sutras. Various applications of Vedic mathematics includes theory of numbers, compound multiplication, algebraic operation, calculus, squaring, cubing, cube root, simple quadratic, coordinate geometry and wonderful Vedic Numeric Code . Vedic mathematics is a domain which presents various effective algorithms that can be applied in different branches of engineering such as digital signal processing and computing. All the signal and data processing operations involve multiplication. As speed is always a constraint in the multiplication operation, increase in speed can be achieved by reducing the number of steps in the computation process. The speed of multiplier determines the efficiency of a system.

II. BASYS2 DEVELOPMENT BOARD

A. Features

- 100 K or 250 K -gate Xilinx Spartan 3E FPGA
- Atmel AT90USB2 Full-speed USB2 port providing board power and programming/data transfer interface
- Xilinx Platform Flash ROM to store FPGA configurations
- 8 LEDs, 4-digit 7-segment display, 4 buttons, 8 slide switches
- PS/2 port and 8-bit VGA port
- User-settable clock (25/50/100MHz), plus socket for 2nd clock
- Four 6-pin header expansion connectors
- ESD and short-circuit protection on all I/O signals.

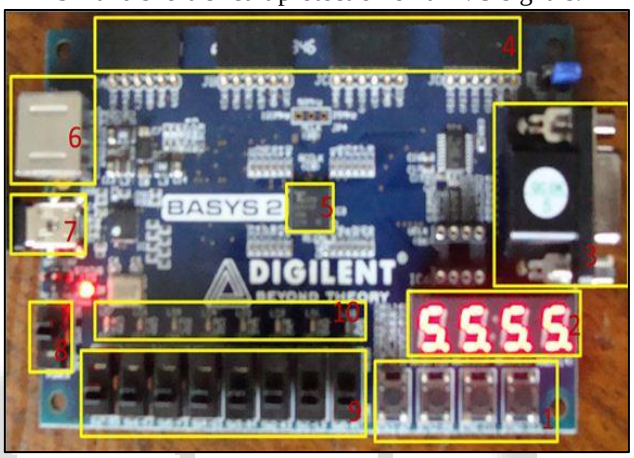

Fig. 1: [BASYS2 development board]

III. FPGA FAMILY (SPARTAN 3E)

Spartan-3E has Low-Cost Features. The Spartan-3E family reduces system cost by offering the lowest cost-per-logic of any FPGA family, supporting the lowest-cost configuration solutions including commodity serial and parallel flash memories, and efficiently integrating the functions of many chips into a single FPGA.

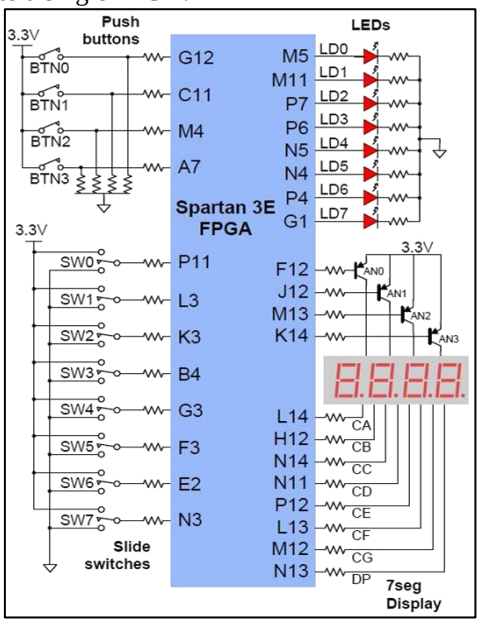

Fig. 2: FPGA family (Spartan 3e)

IV. VEDIC MULTIPLIER (APPROACH USED)

The word "Urdhva-Tiryakbhyam" means vertical and crosswise multiplication. This multiplication formula is applicable to all cases of algorithm for N bit numbers traditionally the sutra is used for the multiplication of two numbers in decimal number system. The same concept can be applicable to binary number system which is being discussed in this paper. Advantage of using this type of multiplier is that as the number of bits increases, delay and area increases very slowly as compared to other multipliers.

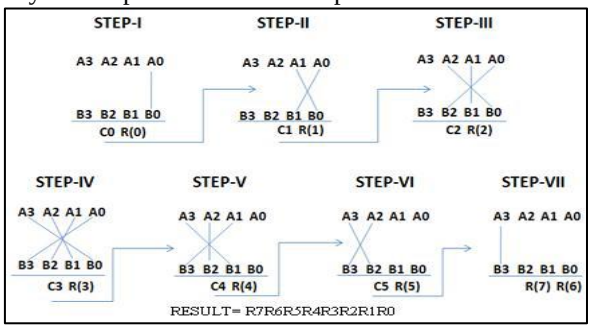

Fig. 3: 4-bit Binary Numbers

In the above figure, 4-bit binary numbers A0A1A2A3 and B0B1B2B3 are considered. The result obtained is stored R0R1R2R3R4R5R6R7.In the first step [A0, B0] is multiplied and the result obtained is stored in R0. Similarly in second step [A0, B1] and [A1, B0] are multiplied using a full adder and the sum is stored in R1 and carry is transferred to next step. Likewise the process continues till we get the result.

V. DESIGN OF 16 BIT VEDIC MULTIPLIER

The design of 16×16 block is a similar arrangement of 8×8 blocks in an optimized manner as in figure below. The first step in the design of 16×16 block will be grouping the 8 bit (byte) of each 16 bit input. These lower and upper bytes pairs of two inputs will form vertical and crosswise product terms. Each input byte is handled by a separate 8×8 Vedic multiplier to produce sixteen partial product rows. These partial products rows are then added in a 16-bit carry look ahead adder optimally to generate final product bits.

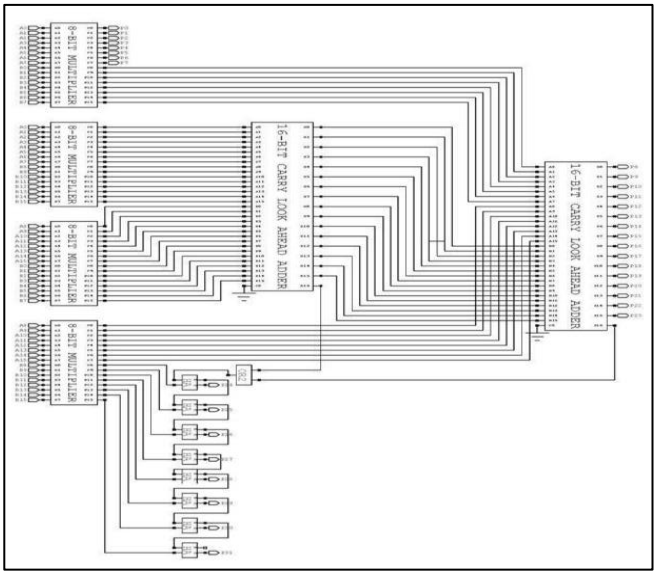

Fig. 4: [Arch. of 16-bit Vedic multiplier]

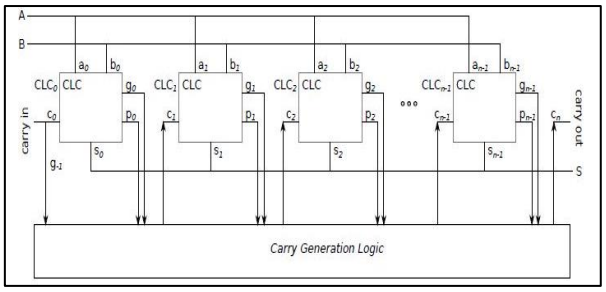

Fig. 5: [Arch. of CLA adder]

$c0 = g{-}1.$

$c1 = g{-}1p0 + g0.$

$c2 = g{-}1p0p1 + g0p1 + g1.$

$c3 = g{-}1p0p1p2 + g0p1p2 + g1p2 + g2.$

VI. EDA TOOL USED (XILINX ISE-14.4)

In this work, 16x16 bit Vedic multiplier is designed in VHDL (Very High Speed Integrated Circuits Hardware Description Language). Logic synthesis and simulation was done in Xilinx ISE14.4 Project Navigator and ISim simulator integrated in the Xilinx package. The performance of circuit is evaluated on the Xilinx device family Spartan3E, package cp132 and speed grade -5.The RTL schematic of 16x16 bit Vedic multiplier. "ved16x16" comprises of four 8x8 bit Vedic multiplier and two 16-bit carry look ahead adder.

VII. SIMULATION RESULTS

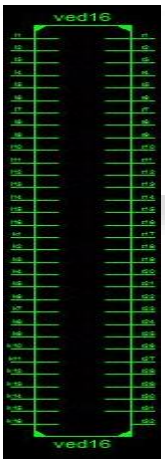

Fig. 6: [Block view of 16-bit Vedic multiplier]

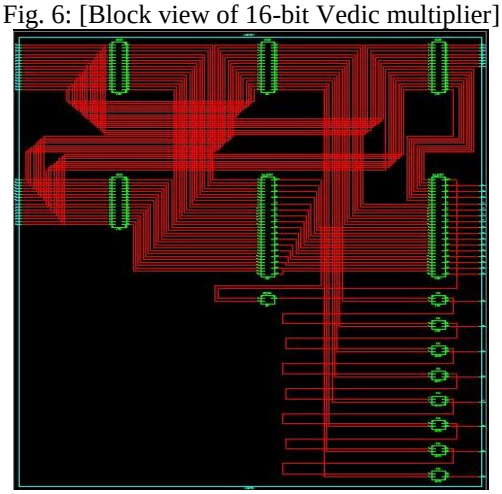

Fig. 7: [RTL view of 16-bit Vedic multiplier]

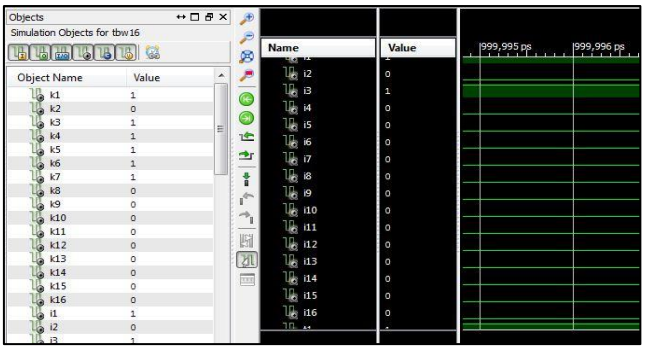

Fig. 8: [Test bench of 16-bit Vedic multiplier] – i/p

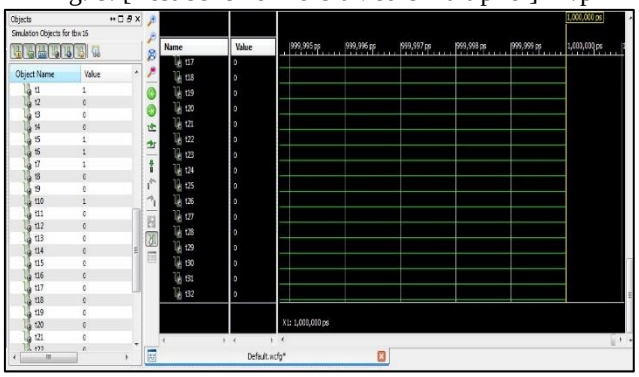

Fig. 9: [Test bench of 16-bit Vedic multiplier] –o/p

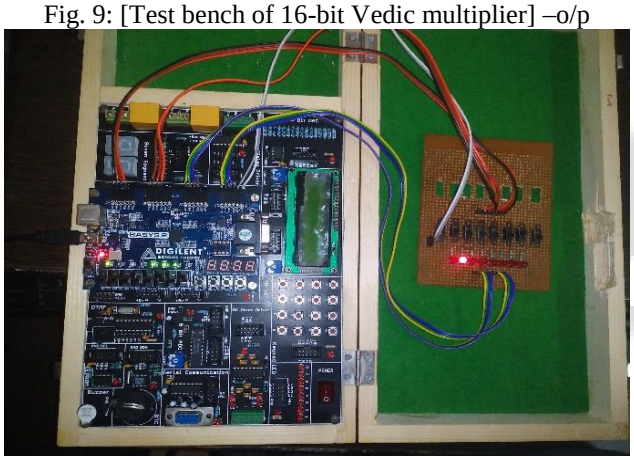

Fig. 10: Implementation on FPGA(Spartan 3E)

VIII. CONCLUSION

This project consists of two major tasks. First, a study of the Vedic multiplier using UT concept and, second test bed development and implementation of Vedic multiplier in FPGA environment.

We have designed 16-bit Vedic multiplier using Xilinx 14.4 successfully. The lower bit Vedic multiplier (for Ex. 2-bit, 4-bit, 8-bit) was verified in the standard verification environment of FPGA and are ready to be used. This design is suitable for the applications that require low power consumption and small occupied Si space. The main advantage is they can be implemented in whichever FPGA which reflects they are not dependent on the implementation platform.

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