Design of Rail-to-Rail CMOS CCII for Low Voltage Low Power Application at 1.5V, 0.25µm CMOS Technology

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Abstract— Low power analog circuits has become very important factor in modern circuit design. At low voltage the threshold voltage changes and show nonlinear variation and transistor operates in moderate inversion region. To overcome this problem constant trans-conductance is required. A second generation current conveyor CCII can reduce this problem. A Rail-to-rail CCII has been shown in this paper. CCII has been designed I two stages first stage is trans-conductance Op-amp and the second stage is current mixer followed by CMOS inverter at the output stage that operates as class AB. It provides Rail-to-Rail output. The CCII has 72 dB of gain and 66^0 of phase margin and UGB of 1.54MHz.

Key words: Rail-to-Rail CMOS CCII, CMOS Technology

I. INTRODUCTION

Power has become a very crucial factor in today's technology. As the battery operated devices such as mobile phones, laptops and hearing aids etc. require low power dissipation. Power is proportional to square of the supply voltage thus it become very important to reduce the power supply. Lowering the supply voltage creates many issues such as Threshold voltage (V_{TH}) change of the transistor as V_{TH} has a nonlinear nature.

There are many technologies used in the low voltage analog circuits such as BJT, CMOS, and Bi-CMOS. CMOS technology is preferred over the other because of its low power dissipation, low fabrication cost and high density area. Current mode circuit (CMC) is most widely used for the low voltage applications [8]. This technique has some advantages, the signals handled by the analog currents in their initial state as the output signals of the sensors are often currents or charges, and the signals are compressed in the entry node that allow the designer to use low voltage power supply. Moreover, this type of circuit shows a high-performance in terms of speed, bandwidth, and accuracy [9].

There are various classification of the current conveyor such as first generation current conveyor (CCI), second generation current conveyor (CCII). CCII has better performance parameter as compare to the Op-amp at low voltage applications, it at high speed and has wide bandwidth. Almost all the application of Op-Amp can be implemented by it such as voltage gain amplifier, voltage follower, and universal filter, oscillator etc. [9].

The paper is organized as fallows; Section 2 describes the Rail-to-rail CMOS differential amplifier. Section 3 describes the conventional CMOS inverter.

II. RAIL-TO-RAIL CMOS DIFFERENTIAL AMPLIFIER

There are various techniques of producing constant trans-conductance (g_m) for the rail to rail input stage, there are large variation in g_m which depends the operating region of the transistor.

A. g_m/I_D Technique

g_m/I_D strongly related to the performance of the circuit, it also indicated the operating region of the device and the size of the transistor. The coefficient g_m/I_D is the slope of the curve I_D versus V_G in a logarithmic scale (1).

$$\frac{g_m}{I_D}=\frac{\frac{\partial I_D}{\partial V_G}}{I_D}=\frac{\partial \log(I_D)}{\partial V_G} \quad (1)$$

The g_m/I_D ratio appears in the weak inversion region, and then it decreases until reaching the strong inversion region. Moderate inversion region are more adequate for low power.

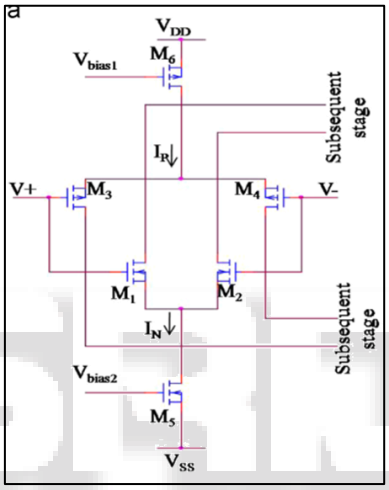

Fig. 1: Complementary input stage

B. Design methodology for the input stage of Op-Amp

The input stage of Op-Amp provides a rail to rail operation which reduces the limitation of the input dynamic range due to threshold voltage. Reduction in the supply voltage reduces the input common mode range (V_{icmr}). Rail to rail will be used as the input stage of CCII.

Rail to rail input stage provide maximum positive to negative voltage swing to input common mode signal [10]. To archive the maximum rail to rail input common mode signal CMOS differential pairs have to be driven in parallel as shown in Fig. 1. The total small signal trans-conductance (g_{mt}) of above mentioned combination depends on the common mode input voltage.

C. DC Level Shifter Technique

DC level shifter circuit is used to proper shift in trans-conductance, which is connected to the input stage of the OTA. It has N and P MOS differential pair which is connected in parallel as shown in figure g_{mt} is the total trans-conductance of the N and P differential pair, M_5 and M_6 provides the I_N and I_P trail currents of N and P differential pair by proper biasing voltage.

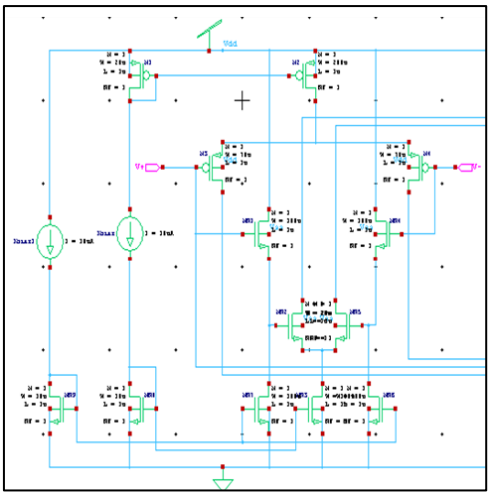

Fig. 2: MOS source follower

M_7 and M_8 (N MOS source follower) along with M_9 and M_{10} (active load) are used for the DC level shifting. The output of the source follower (N MOS) is connected to the N differential pair. The shifting of the transition region of the N MOS transistor can be given by the following equations.

$$V_{in,\min 1} = V_{GSn} + V_{Dsat}$$

$$V_{in,\min 2} = V_{GS,sh} + V_{Gsn} + V_{Dsat}$$

$$V_{Gs,sh} = V_{TH,N} + \sqrt{\frac{2I_{sh}}{\beta_n}}$$

$$g_{mt} = g_{mn} + g_{mp}$$

$$g_{mt} = \beta_n (V_{in} - V_{sn} - V_{TH,N} - \sqrt{\frac{2I_{sh}}{\beta_n}} - V_{TH,N}) + g_{mp}$$

Where V_{GSn} is gate to source voltage of the transistor M_1 and M_2

$V_{D,sat}$ saturated drain to source voltage of transistor M_5

$_{GS,sh}$ is the shift voltage of transistor M_7 and M_8 in V-icm

$V_{TH,N}$ is the threshold voltage of NMOS transistor

I_{sh} is DC current in M_7 and M_8

β_n is the transistor gain factor of NMOS

The next stage combines the currents from N and P differential pair and converts to single ended output. The circuit uses cascade current sink to add the currents and provides high dynamic range of the output voltage.

$$\left(\frac{W}{L}\right)_i = \frac{2I_{D,i}}{K.V_{Dsat,i}}$$

$$V_{B1} = V_{SS} + V_{Dsat,14} + V_{Dsat,16} + V_{TH,16}$$

$$V_{B2} = V_{DD} - V_{Dsat,20} - V_{Dsat,18} - V_{TH,18}$$

Where i represents the transistor number and K is the process factor of the MOS transistor, V_{B1} and V_{B2} are the biasing voltage.

III. CMOS INVERTER

The CMOS inverter at the output stage increases the dynamic range at the output, which can be shown by the following equation

$$V_{in} = \frac{V_{DD} + V_{TH,P} + \sqrt{\frac{\beta_n}{\beta_p}} V_{TH,N}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

$$I_Q = \frac{\beta_n}{2}\left(\frac{V_{DD} + V_{TH,P} + \sqrt{\frac{\beta_n}{\beta_p}} V_{TH,N}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} - V_{TH,N}\right)$$

$$I_{MAX} = I_N = \frac{\beta_n}{2}(V_{DD} - V_{TH,N})^2$$

The CMOS inverter operates in class AB mode with DC voltage V_m.

IV. SIMULATION RESULTS

The DC transfer characteristics of Rail to rail input stage is shown in fig 3. In this mode region it can be operated as a comparator at 0.3 V, 0.78V and 1.2 V. The designed Rail to rail Op-Amp introduces low offset voltage and also wide voltage swing.

The magnitude and phase plot of CCII is show in the fig 4. The CCII has magnitude of 72 dB and phase margin of 66^0 the simulation result is shown in the fig 4.

The DC response of the Rail-to-rail Opam-Amp is shown in fig 3.

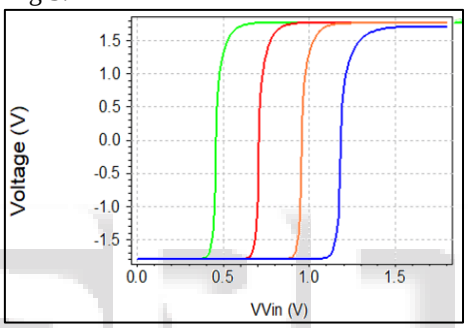

Fig. 2: DC response of Rail-to-rail Opamp

The trans-conductance plot of MOS transistor at 0.25 µm technology is shown in fig 5. Which is tested at 1.8 V V_{dd} and 0-1.8 V DC voltage swing.

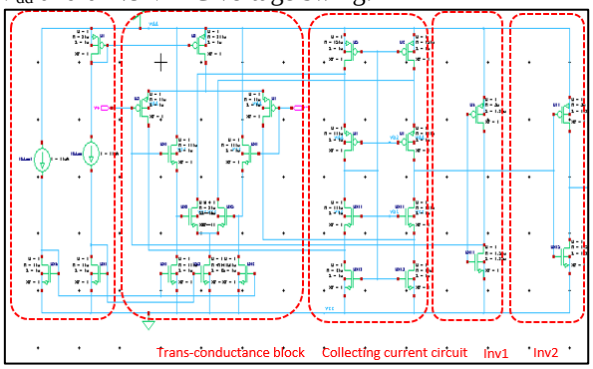

Fig. 3(a): DC voltage swing

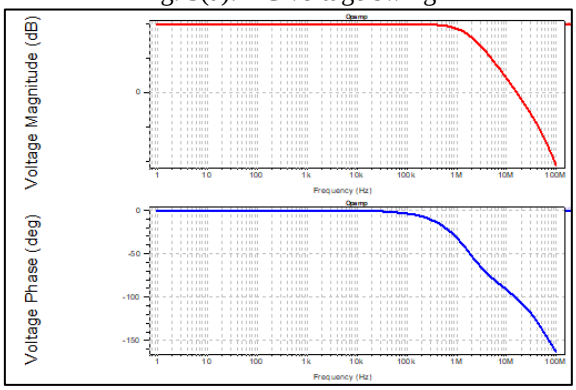

Fig. 4: Gain and phase response of Rail-to-Rail Op-Amp

At the output stage CMOS inverter is used as class AB with DC setting voltage V_m. The value of V_m can be evaluated by connecting the input and output of inverter together which is shown in fig 4.

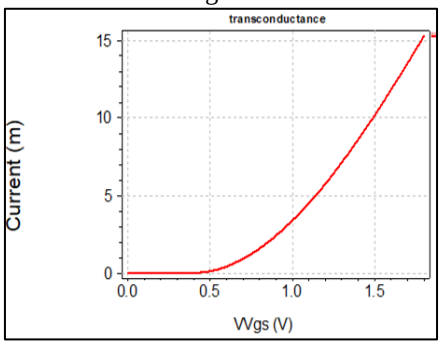

Fig. 3: Trans-conductance plot of MOS transistor at 1.8 V supply voltage

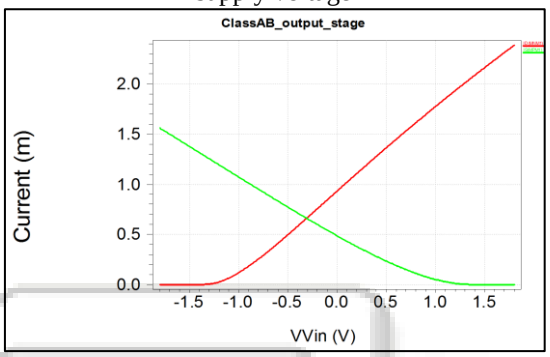

Fig. 4: Input-output transfer characteristic for class AB output stage

The Rail-to-rail CCII has been simulated for the input V_X and V_Y. The rail-to-rail voltage transfer between the input and output terminals as shown in fig. 7.

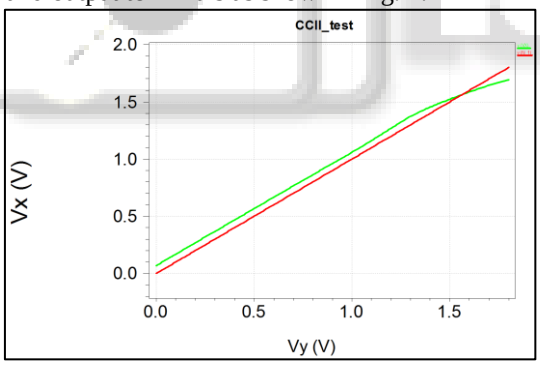

Fig. 5: V_X and V_Y tracking

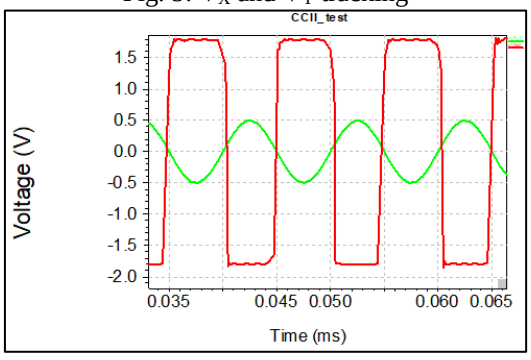

Fig. 6: Open loop transient response of CCII for sinusoidal input

Open loop transient response of CCII in inverting mode is shown in the fig.8 that gives square wave at the output.

The test setup of CCII for close loop non-inverting Op-Amp is shown in the fig.9 and the transient response for sinusoidal input is shown in fig.10.

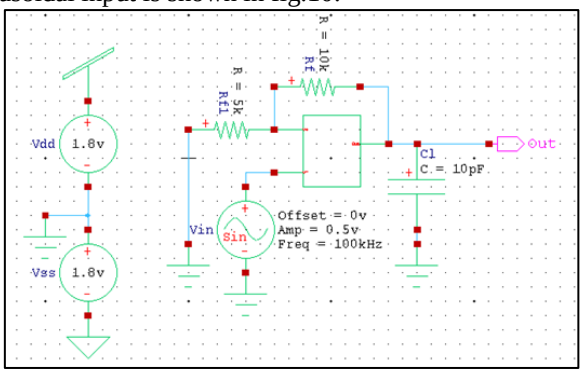

Fig. 9: Test setup of CCII for non-inverting Op-Amp

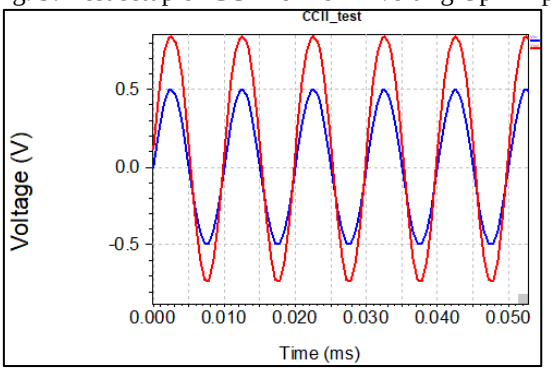

Fig. 10: Transient response of CCII for non-inverting Op-Amp

V. Conclusion

A low voltage low power Rail-to-rail CMOS second generation current conveyor is shown. The CCII is divided into two main part first part is differential rail to rail op-amp followed by the class AB (CMOS inverter). The CCII provides high dynamic range at the input and at the output.

The single stage Rail-to rail Op-Amp has been designed with Operational Trans-conductance Amplifier (OTA) and current summing circuit. The input stage of OTA has two differential pairs (N and P differential pair) connected in parallel.

The Op-Amp stage has been simulated at differential common mode voltages (0V, 0.75V and 1.5V) with load capacitance of 1nF. At this load capacitance Op-Amp gain bandwidth product remains unchanged. The proposed circuit provides maximum input voltage dynamic range equals to 1.5

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