Efficient FFT/IFFT Implementation Technique for OFDM on FPGA

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Abstract— Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier modulation technique which divides the available spectrum into many carriers. OFDM uses the spectrum efficiently compared to FDMA by spacing the channels much closer together and making all carriers orthogonal to one another, to prevent interference between the closely spaced carriers. The main advantage of OFDM is their robustness to channel fading in wireless environment. The principles of OFDM modulation have been around since 1960s. However, recently the attention toward OFDM has grown dramatically in the field of wireless and wired communication systems. In parallel, Field Programmable Gate Array (FPGA) is also emerging as a fundamental paradigm in the implementation of these standards. This is due to their increased capabilities (speed and resources). The objective of this project is to design and implement OFDM transmitter and receiver on FPGA hardware. This project concentrates on developing Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT), in an efficient way. The work also includes design of a mapping module (Modulator), serial to parallel and parallel to serial converter module. The design uses 64-point FFT and IFFT for the processing module, which indicate that the processing block contain 64 inputs data. In this work, a pure VHDL design, integrated with some intellectual property (IP) blocks, is employed to implement an OFDM transmitter and receiver. The proposed design is map and test on Xilinx Spartan 3E FPGA and for simulation, synthesis and implementation XILINX ISE 13.2 software is used.

Key words: OFDM, FPGA, IFFT, FFT, XILINX

I. INTRODUCTION

Orthogonal Frequency Division Multiplexing is a special case of multicarrier transmission, where a single data stream is transmitted over a number of lower-rate subcarriers. OFDM can be seen as either a modulation technique or a multiplexing technique. In OFDM, multiplexing is applied to independent signals but these independent signals are the part of one main signal. In OFDM, the signal itself is first split into independent channels, modulated by data and then re-multiplexed to create the OFDM carrier. OFDM is a technique especially suitable for wireless communication due to its resistance to inter-symbol interference (ISI) and inter-carrier interference (ICI).

FPGA are programmable semiconductor devices that are based around a matrix of logic blocks, connected through programmable interconnect. Basically, an FPGA contains 3 main types of resources: logic blocks, I/O blocks for connecting to the pins of the package, and interconnection wires and switches. The logic blocks are arranged in a two-dimensional array and the interconnection wires are organized as horizontal and vertical routing channels between rows and columns of logic blocks. The routing channels contain wires and programmable switches, which allow the logic blocks to be interconnected in many ways [B].For Xilinx's FPGA, basic logic unit is known as a Configurable Logic Block (CLB). Exact numbers and features vary from device to device, but every CLB consists of a 4 to 6 inputs RAM-based Look-Up Tables (LUTs) to implement logic, some selection circuitry (MUX, etc), and flip-flops.

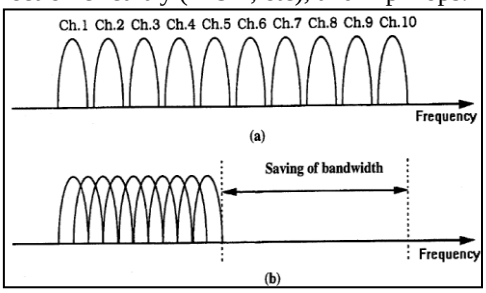

Fig. 1: (a) Spectrum of FDM showing guard bands, (b) Spectrum of OFDM showing overlapping subcarriers.

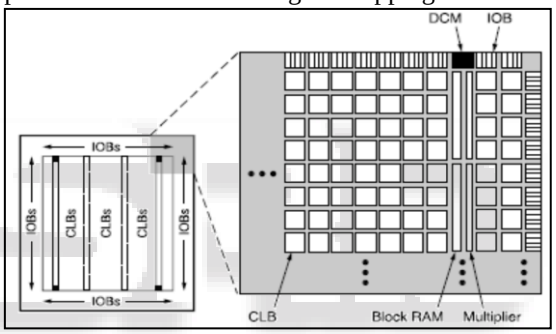

Fig. 2: Block Diagram FPGA

The LUTs are highly flexible and can be configured to handle combinatorial logic, shift registers or RAM. FPGA can be used, to implement logic circuits of more than a few hundred thousand equivalent gates in size. Equivalent gates is a way to quantify a circuit's size, by assuming that the circuit is to be built using only simple logic gate and then estimating, how many of these gates are needed.

II. LITERATURE SURVEY

In [1] Paper they use a high speed 64-point FFT processor based on FPGA using a hybrid-parallel and pipeline architecture. The study has been particular used to decimation-in- frequency (DIF) FFTs of length 64 points and a 8-bit word size has been considered. The whole processor has been implemented using two parallel 8-point FFT and 8 complex multipliers between them. 'Twiddle factor' addresses can be easily generated with counters. The address generation logic is very simple and does not limit the throughput of the system. To improve the system operation speed, a hybrid parallel FFT algorithm is used in this processor. Internal structure of hybrid parallel FFT Firstly, a DEMUX operation is used to de-series the input data into 8 parallel channels.

In [2] In This Paper Describes the Fast Fourier Transform (FFT) is a very important algorithm in signal

processing, software defined radio and the most promising modulation technique i.e. Orthogonal Frequency Division Multiplexing (OFDM). This paper describes the design and implementation of a fully pipelined 64-point FFT engine in programmable logic. The FFT takes 16-bit fixed point complex numbers as input and after a known pipelined latency of 20 clock cycles produces the desired output. The input data samples are fed in parallel to the FFT engine to generate outputs in parallel.

In [3] In this paper OFDM is the most promising modulation technique for most of the wireless and wired communication standards. The basic idea of OFDM is to divide the available spectrum into several sub channels, making all sub channels narrowband which experiences flat fading. OFDM uses the spectrum efficiently due to its orthogonality and prevents interference between the closely spaced carriers. OFDM provides high bandwidth efficiency because the carriers are orthogonal to each other's and multiple carriers share the data among themselves. The main advantage of this transmission technique is their robustness to channel fading in wireless communication environment.

In [4] In this Paper, the design of 32 and 64-point FFT using Radix-2, Radix-8, and Split-Radix algorithms are performed, and the performance analysis with all the three algorithms are done using Minimum Delay(ns) as parameter and their synthesis and simulation results are shown by Xilinx synthesis tool on virtex. The test bench wave forms are displayed by using Xilinx ISE Design Suite 13.2. Further, the performance analysis can also be done by taking various parameters into consideration for different or same number of points.

In [5] this paper describes a FPGA design, validation and implementation of an "Orthogonal Frequency Division Multiplexing" (OFDM) modulator for IEEE 802.11a using a high-level design tool, also reports the resources requirements for the presented system. the design of an OFDM transmitter as a part of an OFDM demonstrator Hiperlan/2based, the features of that transmitter are: 36 Mbit/s, ¾ punctured code rate, 16QAM, 64 IFFT and cyclic prefix of16 samples, meanwhile this work presents all the QAM and PSK alphabets supported by the Std. IEEE 802.11a.

In [6] in this Paper Described the Fast Fourier Transform (FFT) is one of the rudimentary operations in field of digital signal and image processing. Some of the very vital applications of the Fast Fourier transform include Signal analysis, Sound filtering, Data compression, Partial differential equations, Multiplication of large integers, Image filtering etc. Fast Fourier transform (FFT) is an efficient implementation of the discrete Fourier transform (DFT).

III. LIMITATION OF EXISTING SYSTEM

By doing literature survey in FFT/IFFT algorithm are required large number of multiplication and addition. The order of arithmetic operations for FFT is O (NlogN) that is NlogN additions and (N/2) logN multiplications. In arithmetic operation, large number of resource are required. But one limitation in FPGA is the limited number of resources. So, reduce the number of arithmetic operation and more efficient way implement FFT/IFFT algorithm for OFDM system on FPGA.

OFDM systems have the following disadvantages: (i)High synchronism accuracy; (ii) Multipath propagation must be avoided in other orthogonality not be affected, and (iii) Large peak-to-mean power ratio due to the superposition of all subcarrier signals, this can become a distortion problem.

IV. PROPOSED METHODOLOGY

The generation of OFDM signal started from serial to parallel converter. The input data is in serial form and need to convert into parallel format, since QAM (Quadrature Amplitude Modulation) module requires parallel input to process data. These parallel converted data is mapped to appropriate symbol, with the help of amplitude modulation mapping bank. The parallel symbols are transformed from frequency domain into time domain, using IFFT module. Now, the signals are added with a cyclic prefix and converted into serial format, before being transmitted.

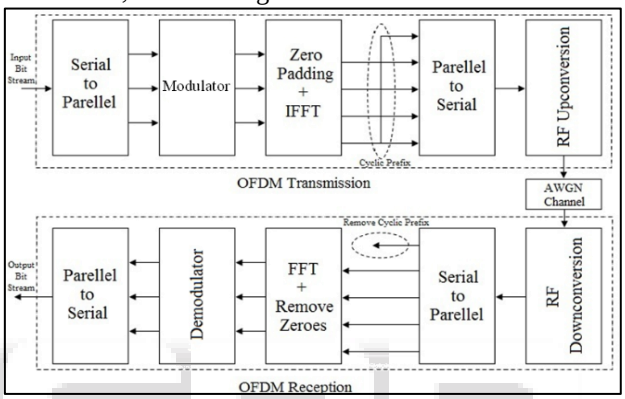

Fig. 3: Basic OFDM system

The received data is in serial format, since FFT input is in parallel, a module which use to converts from serial to parallel is required. Before applying data to the FFT unit, cyclic prefix is removed. Output from FFT is demodulated, using de-mapping module. To demodulate the subcarriers using QAM modulations, reference phase and amplitude of the constellation, on each subcarrier are required. The output of de-modulating module is converted back to serial format, through parallel to serial converter, to get the transmitted data.

V. SIMULATION RESULTS

A. *FFT*

The 8-point complex input ir0+ii0 to ir7+ii7 it is time domain data to converted frequency domain data otr0+oti0 to otr7+oti7 help of DIT FFT algorithm and simulated of 8-point FFT block as shown in Fig.4 and 5.

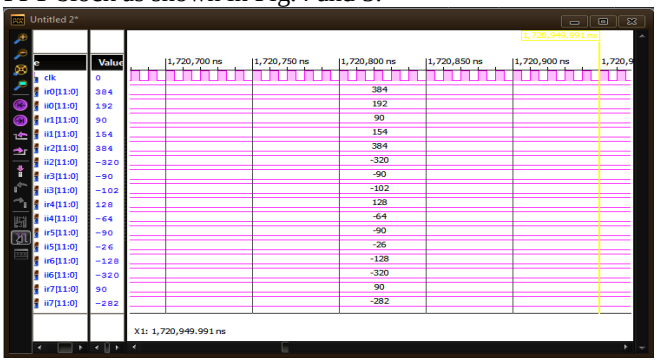

Fig. 4: Input to 8-point FFT

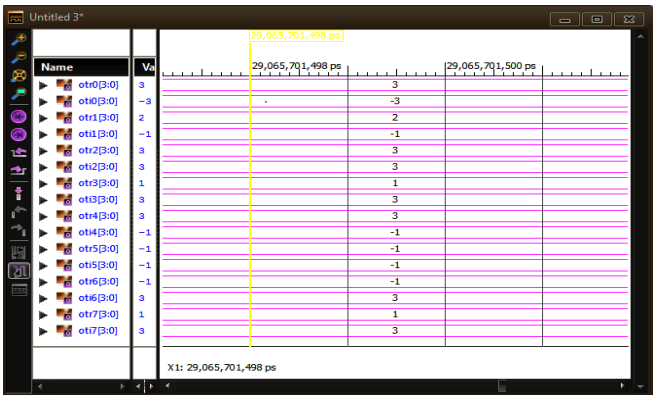

Fig. 5: Output of 8-point FFT

B. IFFT

As shown in Fig. 6 it is frequency domain 8-point complex input data (ir0+ii0 to ir7+ii7) for IFFT block to converted time domain 8-point complex output data (otr0+oti0 to otr7+oti7) as shown in Fig 7. In this way, for implementing FFT using proposed technique, we require only 4 multipliers whereas by normal method, it will require 20 multipliers. Thus, for FFT/IFFT implementation, by proposed technique, we can save multipliers up to 80%. Multiplier requires much resources and more power. Thus, we can save much of the resources.

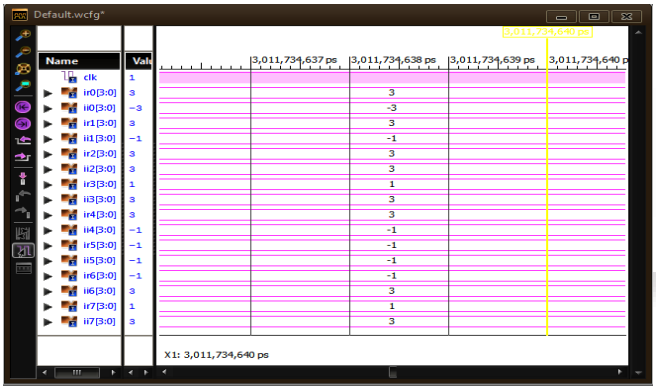

Fig. 6: Input to 8-point IFFT

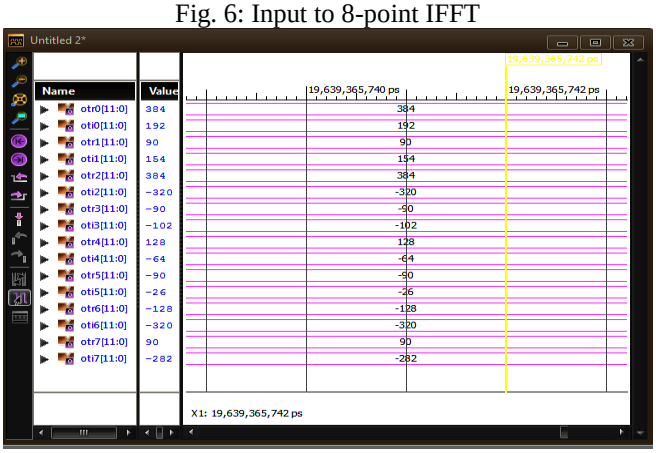

Fig. 7: Output of 8-point IFFT

C. Transmitter model of OFDM System

The generation of OFDM signal started from serial to parallel converter. The input data is in serial form and need to convert into parallel format, since QAM (Quadrature Amplitude Modulation) module requires parallel input to process data. These parallel converted data is mapped to appropriate symbol, with the help of amplitude modulation mapping bank. The parallel symbols are transformed from frequency domain into time domain, using IFFT module. Simulated output of transmitter OFDM block as shown in Fig.8.

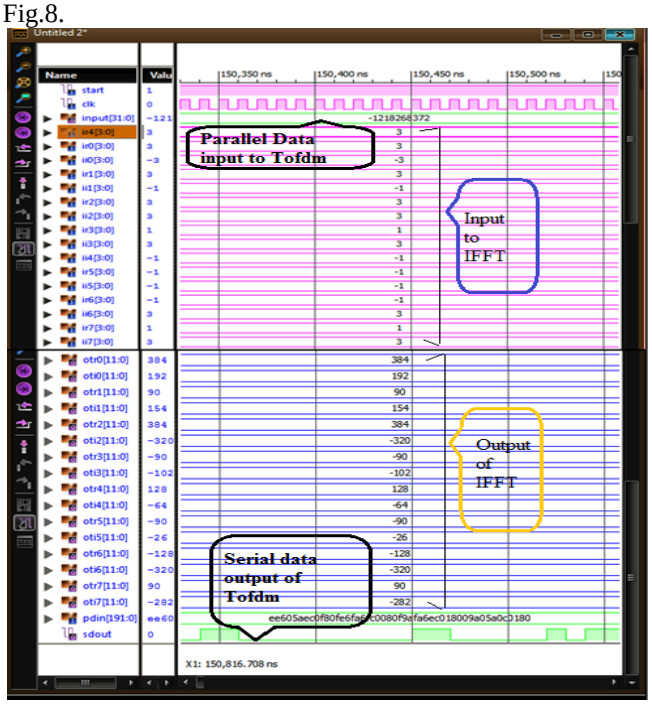

Fig. 8: Transmitter model of OFDM System

D. Receiver model of OFDM System

First, the OFDM data are split from a serial stream (192-bit input data) into parallel sets (input). The Fast Fourier Transform (FFT) converts the time domain samples (ir0+ii0 to ir7 ir7+ii7) back into a frequency domain (otr0+oti0 to otr7+oti7) representation then Demodulated Data using Constellation Diagram. Finally, the parallel to serial block converts this parallel data (pdin) into a serial (sdout) stream to recover the original input data of transmitter module as shown In Fig. 4.21.

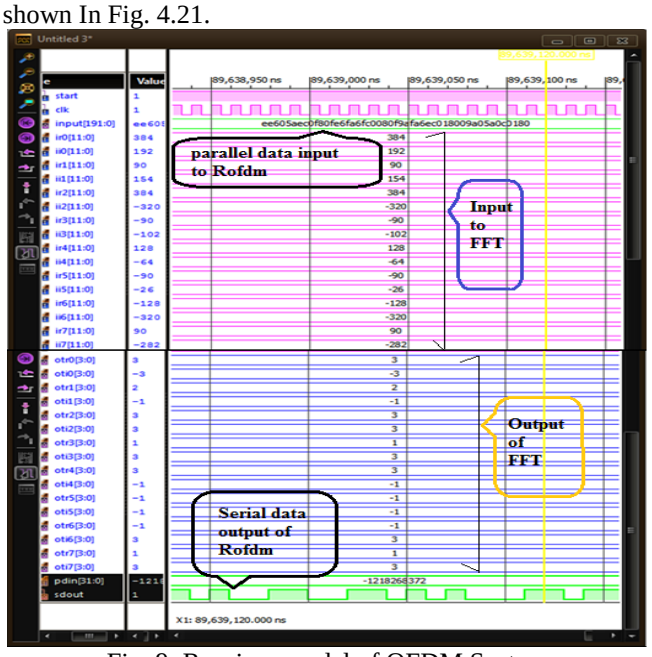

Fig. 9: Receiver model of OFDM System

VI. CONCLUSION & FUTURE SCOPE

The main aim of the project is to implement the core signal processing blocks of OFDM system on FPGA using VHDL

language. The OFDM system is designed on Xilinx project navigator for different number of subcarrier i.e. FFT and IFFT points. FFT and IFFT are important and complex blocks in OFDM system which consumes lots of resources. So, its efficient implementation in terms of available resources is must. In this project, design for efficient implementation of FFT and IFFT modules is proposed and implemented. Also, complete OFDM system in efficient way is implemented. Design is implemented on Spartan 3E Nexsy2 FPGA Board using Xilinx ISE 13.2 synthesis tool, tested for different data patterns and results are compared with theoretical expected results. By manually entering transmitted data at receiver, the recovery of the original required data is done. The results are matching with expected results. The steps involved in implementation of the communications system on hardware and also how to use IP core, Chip Scope Pro are learned during completion of the project. The resources utilization of the Spartan 3E by the design is observed, it shows that the device is sufficient to accommodate the design and there is scope for system expansion in future.

In this project, the OFDM system is implemented using 64 subcarriers i.e. with 64-point IFFT and FFT. This is basic implementation and has advantage of less processing time requirement and complexity but this system has less spectral efficiency. The spectral efficiency can be increased by two ways one by increasing the number of subcarriers and second by change the modulation. In same system, the spectral efficiency (bits/Hz) will be increased by 4 times if 64 QAM is used instead of 16 QAM to modulate subcarrier. It will cause increased resources utilization.

REFERENCES

[1] Joaquin Garcia, Rene Cumplido,"On the design of an FPGA-based OFDM modulator for IEEE 802.16.", IEEE proceedings of 2005 international conference on reconfigurable computing and FPGAs.
[2] Farzad Manavi, Yousef R. Shayan, "Implementation of an OFDM modem for the physical layer of IEEE 802.11a standard based on Xilinx Virtex-II FPGA.",IEEE Vehicular technology conference,2004, vol.3 pp-1768-1772.
[3] Wen Fan, Chui-sing Choy, senior IEEE member "Robust, low complexity and energy efficient downlink baseband receiver design for MB-OFDM UWB system.", IEEE transactions on circuits and system Vol.59 No.2 February 2012 IEEE pp.399-408.
[4] R.W. Chang, "Synthesis of band limited Orthogonal Signals for Multichannel data transmission," Bell system Technical Journal, Vol. 45, Issue 10 pp. 1775-1776, December.1996.
[5] Salzberg, B. R., "Performance of an efficient parallel data transmission system," IEEE transaction comm., Vol. COM-15, pp. 805-813, December. 1967.
[6] Weinstein, S. B., and P. M. Ebert, "Data transmission by Frequency Division Multiplexing using the DFT," IEEE Trans. Comm., Vol. COM – 19, pp. 628-634, October.1971
[7] Horosaki B., "An orthogonally multiplexed QAM system using the DFT," IEEE Trans. Comm. Vol. COM-29, pp. 982-989, July 1981.
[8] KitaekBae, Student Member, IEEE, Jeffrey G. Andrews, Senior Member, IEEE, and Edward J. Powers, Life Fellow, IEEE, "Quantifying an Iterative Clipping and Filtering Technique for reducing PAPR in OFDM",IEEE Transactions on wireless communications, vol. 9, no. 5, may 2010
[9] Michael Bernhard, Joachim Speidel on "Implementation of an IFFT for an Optical OFDM Transmitter with 12.1 Gbit/s" IEEE Photonic Networks, 2010 ITG Symposium on Leipzig, Germany May 2010 pp.1-6
[10] Chandrashekhar Kukade, R. M. Patrikar, R. B. Deshmukh, "Design & Implementation of OFDM base band for The IEEE 802.11a WLAN", at (VNIT Nagpur)
[11] IlgazAz and SuhapSahin, "Implementation of FFT and IFFT algorithms in FPGA" Third International Conference on Emerging Trends in Engineering and Technology 2010 IEEE pp.614-619
[12] Koushik Maharatna, Eckhard Grass, and Ulrich Jagdhold, "A 64-Point Fourier Transform Chip for High-Speed Wireless LAN Application Using OFDM"IEEE Journal Of Solid-State Circuit,vol.39,NO.3,March-2012.
[13] Nick LaSorte, W. Justin Barnes, Hazem H. Refai, "The History of Orthogonal Frequency Division Multiplexing" publication in the IEEE "GLOBECOM" 2008 proceedings. pp-1-6.
[14] Karim JABER, Ahmed FAKHFAKH and Nouri MASMOUDI, "VHDL-AMS Behavioral Modeling and Simulation of M-QAM transceiver system", 4th International Conference: Sciences Of Electronic, Technologies Of Information And Telecommunications
[15] J. W. Cooley and J. W. Tukey, "An Algorithm for the Machine Calculation of Complex Fourier Series," published by American Mathematics Society, Mathematics of Computation, vol. 19, no. 90, pp. 297–301, 1965.
[16] Wang Xudong, Liu Yu, "Special-purpose computer for 64-point FFT based on FPGA" IEEE Wireless Communications & Signal International Conference on Nanjing China,Nov-2010 pp.1-3.
[17] J. M. Rudagi et.al., "An Efficient 64-point pipelined FFT Engine"IEEE 2012 international Conference on Advance in Recent Technologies in Communication and Computing.pp.204-208.
[18] K. Sowjanya ,Leela Kumari balivada, "Design & Performance Analysis of 32 and 64 point FFT using multiple Radix Algorithms" internatonal journal of computer applications.Vol.78-No.1,sept.2013 pp.25-29.
[19] R.Durga Bhavani, D. Sudhakar "Design and Implementation of Inverse Fast Fourier transform for OFDM" International Journal of Science and Engineering Applications Vol.2, Issue -7, 2013. pp. 155-158.
[20] Asmita Haveliya "Design and Simulation of 32-Point FFT using Radix-2 Algorithm for FPGA implementation" 2012 second International Conference on Advanced Computing & Communication Technologics.pp.167-171.
[21] N.Kavita, M.Madhu babu,"implementation of OFDM transmitter & receiver For FPGA based Applications" Methods Enriching Power & Energy Developments April 12th, 2013

