Design of SRAM with Negative Capacitance Circuit

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Abstract— Modern day portable devices and ICs demand memory with large size for storage and data manipulation. SRAM having high performance and large size with low power and area makes the design complicated. Due to scaling of CMOS the effect of process variation increases which spread the delay in circuit. The overall effect of process variation in designing SRAM of large size with low area in nanometer technology causes the SRAM cell to functionally fail. Functional failure includes read access failure, write failure. In this paper SRAM of size 512 is design which uses negative capacitance circuit to improve the readability of SRAM. Use of negative capacitance circuit reduces the bit line capacitance which results in improvement of SRAM readability. 512 SRAM cells is design in 180nm technology using 0Tanner EDA tool 13.0.

Key words: SRAM, Process Variation, Read Access Failure, Negative Capacitance Circuit

I. INTRODUCTION

Battery operated and portable system has great demand in market. This portable SOC requires SRAM as memory having high performance and large size with low area and low power. SRAM occupy more than 50% of die area in ICs. Design of SRAM in nanometer technology is great challenge as CMOS shows large process variation due to scaling. While designing any digital system in nanometer technology process variation effects come into the picture. The effect of process variation on CMOS is variation in parameter such as threshold voltage, channel length and mobility [1]-[4]. SRAM cell have smallest device size on chip so it shows largest sensitivity towards the process variation. The overall effect of the process variation and scaling is to delay spread in digital circuit which cause reduction in parametric yield. Due to inter die process variation there is mismatch between the transistor in the cell which result to functionally fail the memory[5].Functionality failure of memory includes static read access and write failure. Read failure is nothing but some SRAM cell are fail to produce sufficient threshold voltage that requires for sense amplifier to read the memory.

Read operation in SRAM is perform by recharging bit line and bit line bar to VDD and word line is enable this will connect internal node of cell to bit line. One of the bit line will start discharging through the node storing zero while other will remain at VDD. Sense amplifier is enabled by using sense control signal when sufficient differential voltage is developed between bit lines. For correct read operation cell must produce differential voltage which is greater than the threshold value of sense amplifier. This differential voltage is function of read current and bit line capacitance.

While designing SRAM with large size number of cell connected between the bit lines are large due to which bit line capacitance is high. The effect of increase in bit line capacitance is to reduce the readability of SRAM. In order to reduce the bit line capacitance SRAM is design with various architecture such as sub array architecture, hierarchical bit line architecture with local sense amplifier [6], [7]. Negative capacitance is one of the techniques to reduce the capacitive load of bit line so as to increases the input differential voltage of sense amplifier [8].

A. *Negative capacitance concept*

Negative capacitance concept is based on the miller effect. It can be implemented by connecting a capacitance say Cf in between the input and output of non-inverting amplifier having gain A as in fig 1.a. By miller effect this Cf is divided into input and output capacitance given by equivalent circuit\ as in f

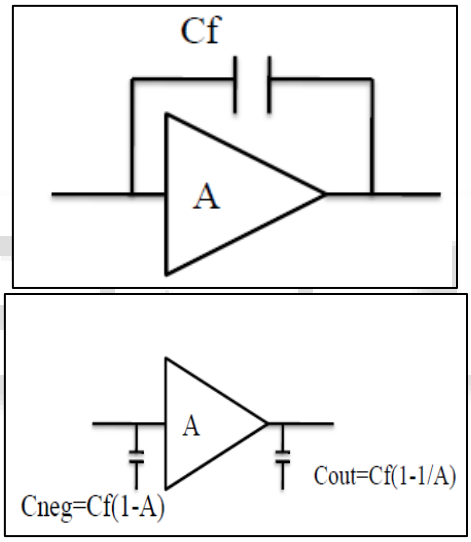

Fig. 1. (a) Negative capacitance implementation using non-inverting amplifier with feedback capacitance. (b) The Miller equivalent circuit of (a). [10]

Where Cneg is input capacitance. When amplifier gain is greater than one the resultant input capacitance is negative and negative capacitance is realized. For example the required value of Cneg is -1fF and A is 2 required value of Cf is 1fF. Also by miller compensation connecting capacitance in between the input and output of non-inverting amplifier add zeros to the left half of plane so it will not affect the SRAM stability.

II. DESIGN OF 512 SRAM CELL

A. *6T SRAM with read and write operation*

6T SRAM cell is use as base cell to design array of 512.6T SRAM cell has minimum area with better noise immunity and speed than other SRAM cell. Architecture of 6T SRAM cell is as shown in fig. 2. It consists of two crossed coupled inverter with two NMOS as access transistor. Two crossed coupled inverter are used to store the data i.e. 0 or 1. Read

and write operation of cell can be control by access transistor, word line (WL) and two bit lines (BL and BLB).

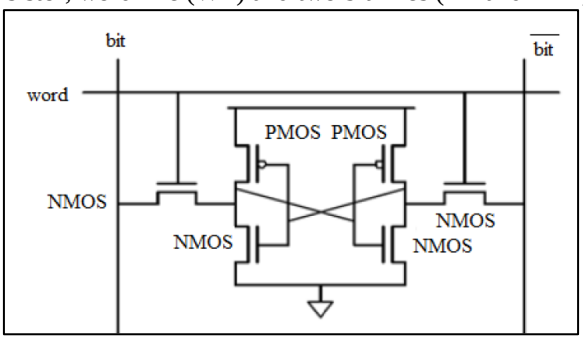

Fig. 2: Architecture of 6T SRAM

1) Read operation:

In read operation both bit lines are floating high and word line is raised. Inserting the word line connects the bit line to the inverters through the access transistor. One of bit line will start discharging through the node storing zero while other remains constant. The difference between bit lines voltage is amplified by the sense amplifier to read the data stored in cell.

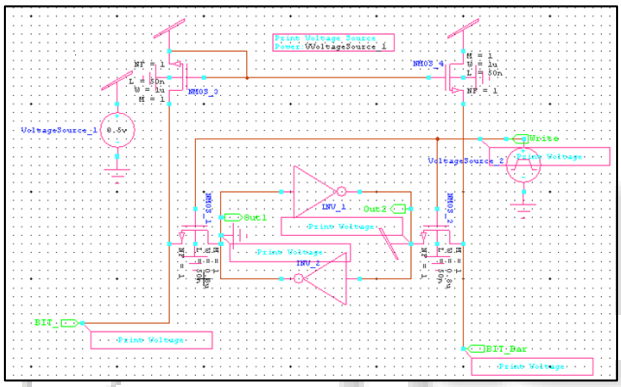

Fig. 3: 6T SRAM read operation

2) Write operation:

Write operation is starts by charging the respective bit line where we wish to write value '1' and left it to floating and other bit line is pulled low by a write driver.

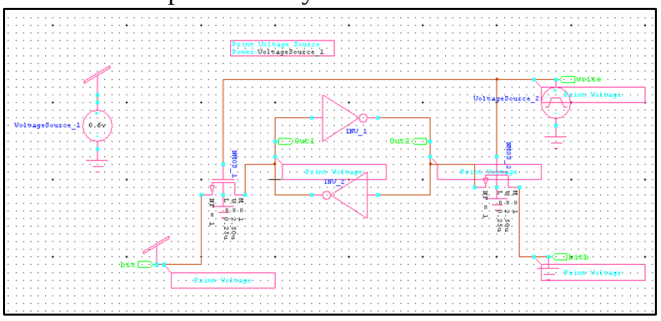

Fig. 4: 6T SRAM write operation

B. Row and column decoder

Row and column decoder are design to select the particular SRAM cell according to the input address. Row decoder is design with help of static NAND gate. Fig. 5 shows the design of Row decoder and Fig. 6 shows the design of Column decoder.

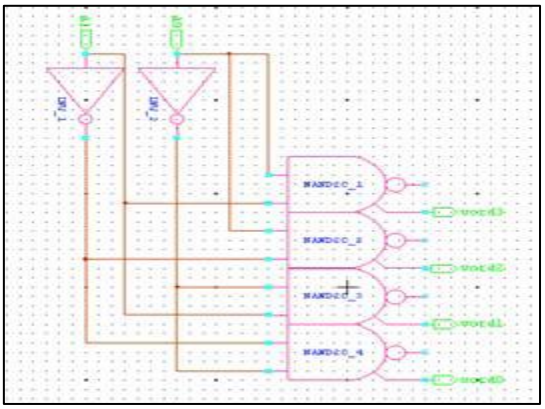

Fig. 5: Row decod

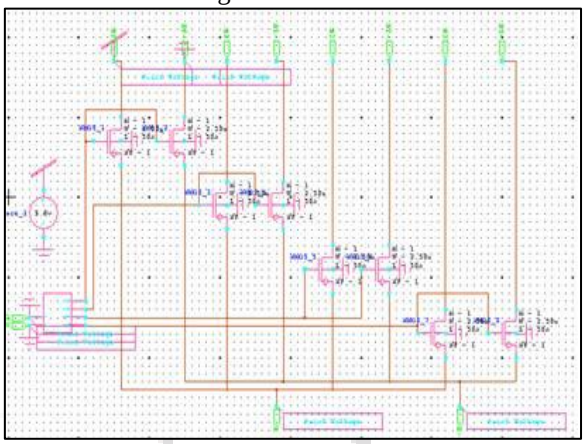

Fig. 6: Column decoder

C. Sense amplifier design

Sense amplifier is design with the help of non-inverting differential pair. A feedback capacitance of value 1fF is connected between input and output of sense amplifier to implement Miller effect based negative capacitance.

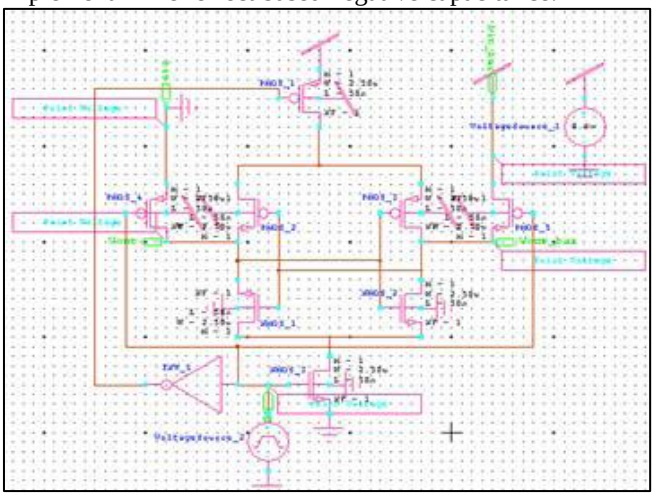

Fig. 7: Differential pair based sense amplifier

D. 512 SRAM with bit line architecture

SRAM array of size 512 is design by using 6T SRAM cell as base cell as in fig. 8. The array consists of 32 rows and 16 columns. The design consists of one sense amplifier instead of using separate sense amplifier in each column. Row and column decoder are used to select the specific SRAM cell.

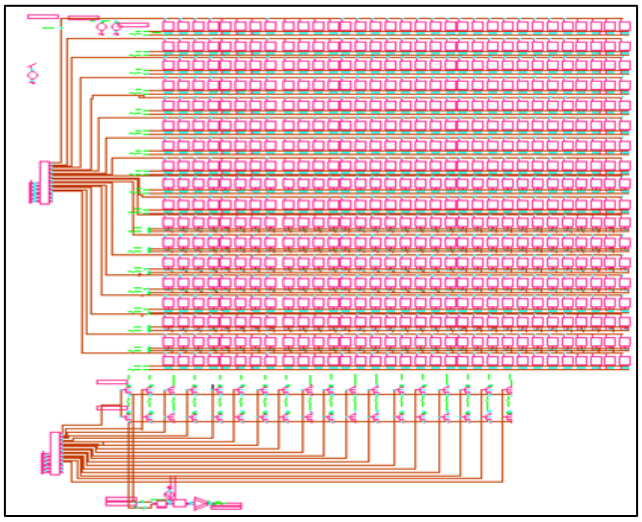

Fig. 8: Complete 512 SRAM cells

III. SIMULATION RESULT AND ANALYSIS

All the circuits have been simulated using 180nm technology on Tanner EDA 13.0.

A. 6T SRAM read operation

In read operation both bit lines i.e. bit and bit bar are floating high and word line is inserted. So both the bit lines are connected to the inverter through access transistor. As node named out1 is storing '0' bit line starts discharging through it while bit line bar remains floating high.

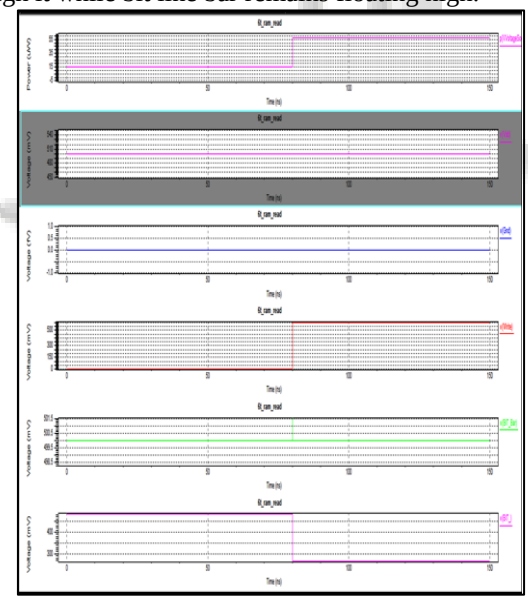

Fig. 9: Output waveform of 6T SRAM read operation

B. 6T SRAM write operation

Here, initially value of node named out1 is '0' and we wish to write their '1'. So bit line is charge high and left it floating while bit line bar is pulled low by inserting write signal. The output shows that value of node named out1 gets '1' and out2 gets '0'. Though the write signal is lowered the values are retained by the nodes.

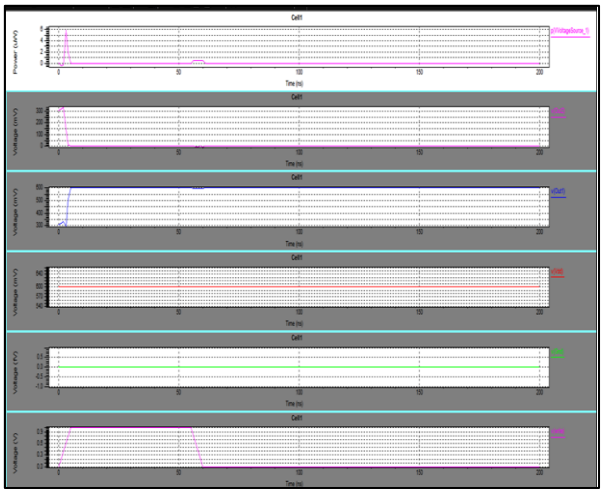

Fig. 10: Output waveform of 6T SRAM write operation

C. Power supply variation analysis

The design is tested for various power supplies. It shows the best results with minimum power supply of 0.8volts.

D. Temperature variation analysis for different Vdd

The power analysis of 512 SRAM cells for different temperature and voltages is tabulated below.

Vdd / Temp.	0.8 V		0.9 V		1.0 V	
	Current (mA)	Power (mW)	Current (mA)	Power (mW)	Current (mA)	Power (mW)
0^0C	11.07	8.85	20.99	18.89	34.95	34.95
10^0C	12.42	9.94	22.46	20.21	36.45	36.45
25^0C	14.51	11.61	24.68	22.21	38.72	38.72
40^0C	16.62	13.30	26.94	24.24	41.01	41.01

Table 1: Power analysis of 512 SRAM cells

E. Monte Carlo analysis

Monte Carlo analysis is done to measure the read time delay in SRAM with and without negative capacitance circuit. Read operation for SRAM without negative capacitance circuit has rise time of 0.383nsec. While read operation of SRAM with negative capacitance circuit has rise and fall time of 0.227nsec and 0.288nsec respectively. Thus there is improvement in the read operation of SRAM.

IV. CONCLUSION

In this paper, SRAM of size 512 is design using 32×16 array. This structure of SRAM uses only one sense amplifier instead of separate sense amplifier in each column. As number of cell connected to bit line is more its capacitance is high. A negative capacitance circuit is used in sense amplifier which reduces the bit line capacitance and hence improves the read operation of SRAM.

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