Design of Double Gate Heterojunction TFET for Low power applications

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Abstract— Due to various problems which are exist with the scaling of MOSFET (Metal Oxide Semiconductor FET) devices such as short channel effects, drain induced barrier lowering (DIBL) and saturation of velocity are limits to the performance of MOSFET. To overcome the existing problems a new device Tunnel FET is alternative to the MOSFET. This paper, propose a design for a double gate Hetero-junction tunnel field effect transistor (DG Tunnel FET). In this work, using the calibrated 2-D TCAD simulation, we demonstrate that the ON current (ION) and OFF state current (IOFF) for the double gate Hetero-Junction Tunnel FET shows the improvement with a silicon channel and SIO_2 as a gate dielectric. DG Tunnel FET is explored by using the practical design parameters which shows ON-state current 13.12μA/μm and the OFF current achieved is 1.68pA/μm for a gate voltage of 1V which specify that better power switch performance.

Key words: Gate Dielectric, BTBT, MOSFET, Double Gate (DG), Tunnel Field Effect Transistor, CMOS

I. INTRODUCTION

Performance of MOSFET (Metal Oxide Semiconductor FET) devices are limited by such as short channel effects, drain induced barrier lowering (DIBL) and saturation of velocity. When the scaling of MOSFET is done without change in the electric field, channel length and thickness of oxide are scaled by 1/k while doping of substrate is scaled by k (where k is scalar constant). The above mention scaling will enable the supply of voltage to be scaled by 1/k and this type of scaling is known as R. Dennard Scaling but it is does not work for the modern devices and the reason is that when we reduce the channel length the dependency between the supply voltage (V_{DD}) and Threshold Voltage (V_T) is not much longer linear [1]. For the modern technology the most important feature for scaling is to maintain gate overdrive voltage (V_{GS}-V_T or V_{DD}-V_T) constant. When gate overdrive voltage is decrease, ON current is decrease which negatively affect the ratio of ON and OFF current and dynamic speed. Two possible solutions for high ON current is to (a) Increase in V_{DD}: With increase in V_{DD}, dynamic and static power consumption is increase as, dynamic and static, (b) Reduce in V_T: With reduction in V_T, OFF current is increase by 10 times which results in high leakage power. As the technology is shrinking today, the number of transistor per unit chip area increase which increase the leakage power and this leads to the standby power consumption in electronic devices. So, these are not the proper solution to problems mention above [2].

Some of the most important challenges to the continued scaling of transistor are such as continuous demand for more silicon device to provide the economic pull to Moore's law, increase in power consumption and increase in complexity of density with keeping the manufacturing cost low specially for the small dimension devices. In order to overcome above challenges to the continued scaling of transistor, literature has proposed the new device known as TFET (Tunnel FET). TFET that has been evolved in 1992 by T.Baba, as one of promising alternative to the conventional MOSFET based on the various parameters and the advantage of TFET is low sub threshold current which leads to low leakage per device with high ON and OFF current ratio which is suitable for digital circuits and memory. TFET based circuits are highly energy efficient and regarded as a green transistor. Tunnel FETs are interesting as low-power devices because of their quantum tunneling barrier [3].

II. TFET STRUCTURE

The basic Structure of TFET is very similar to the MOSFET except that source and drain terminal are doped with opposite type and the most distinguish characteristics of TFET is the doping used for drain and source. A common TFET device structure consists of a P-I-N (p-type, intrinsic, n-type) junction, in which the electrostatic potential of the intrinsic region is controlled by a gate terminal and it is working under the condition of reverse bias. Thermal injection is a mechanism for the source of carrier injection used in MOSFET but TFET utilize the BTBT as mechanism of source carrier. TFET basic structure shown in Figure 1 consist Three parts (Source, Gate and Drain) [4]. Source terminal is used as a source of majority carrier, Drain terminal is used to carry out the majority carrier and Gate terminal is used to controls the majority carrier moving from source to drain indirectly controls the drain current (Drain current depends on number of majority carrier reaching to drain). Channel is formed between the p-type and n-type region. Gate Oxide is used insulate the gate and to enable gate to control the electrostatic in the channel and oxide is insulator, gate oxide prevents the current leakage from channel to gate [5]. TFET belong from the family of abrupt slope device that are currently under the investigation for application that can be used for very low power. TFET belong from the family of abrupt slope device that are currently under the investigation for application that can be used for very low power. The quality of TFET is Sub-threshold Slope (SS) lower the edge of 60mv/decade for Field Effect Transistor (FET) [6].

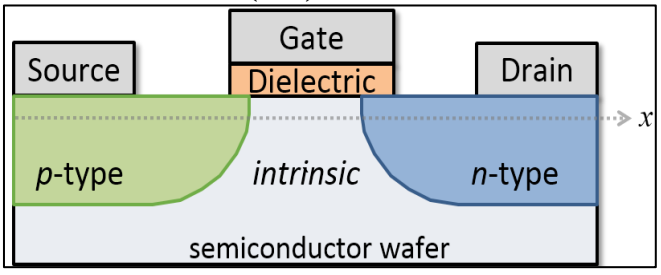

Fig. 1: Basic TFET Structure [6]

The critical quality of TFET is Sub-threshold Slope (SS) lower the edge of 60mv/decade for Field Effect Transistor (FET) which is crucial for low power application. The structure of TFET consist a p-i-n diode, working under condition of reverse bias. The Thermal injection is a source of carrier injection mechanism in MOSFET but mechanism used by a Tunnel FET is band-to-band tunneling (BTBT) for injection of source carrier [7]. Fig. 2 shows the band diagrams of the OFF and ON states in n-channel TFET.

In the OFF state, a large barrier potential is present between the channel and source, consequently tunneling in this not exists but the small leakage current exists. When a voltage of gate (V_G) exceeds the voltage of threshold (V_T), barrier potential exists between the channel and source become contracted so that tunneling current can flow, it is known as the ON state for Tunnel FET. Due to use of different mechanism for injection of source carrier, Tunnel FET is present as comparable device to MOSFET, which is useful in achieving sub threshold slope below 60-mV/decade [8]. In energy band diagram, during the off state condition the width of barrier is very much wide, so no tunnel current is flowing at that time only leakage current is flowing exist. But in the ON state, as the gate voltage is increased with drain voltage ,width become narrower and tunnel current is start flowing in which electrons and holes start flowing between the conduction and valence band [9].

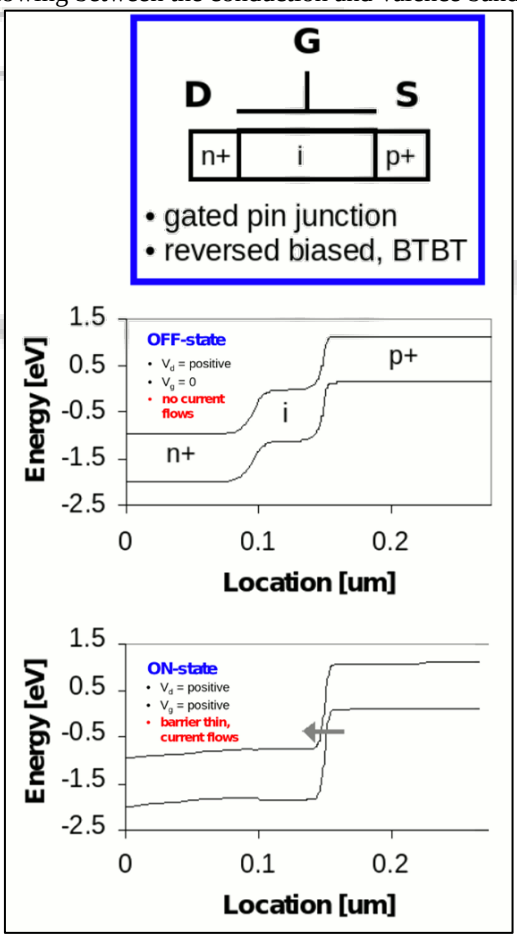

Fig. 2: Schematic & EBG of TFET [9]

Most important challenge of TFETs to obtain ON current with a high value as this critically depends on probability of transmission represented by T_{WKB}, of inter band tunnel barrier and barrier can be approximates by triangular potential [10]. TFET transmission probability is calculated using the Wentzel Kramers Brillouin (WKB) approximation given in equation 1.

$$T_{wkb} \approx \left[\frac{4\lambda\sqrt{2mE_g^3}}{3qh\left[E_q + \Delta\emptyset\right]}\right] \quad (1)$$

Such TFET Device having more than one gate is called Multi gate device or multiple gates FET. A TFET having two gates is known as DOUBLE GATE TFET as shown in figure. So, gate can reduce leakage current more effectively than conventional TFET [11].

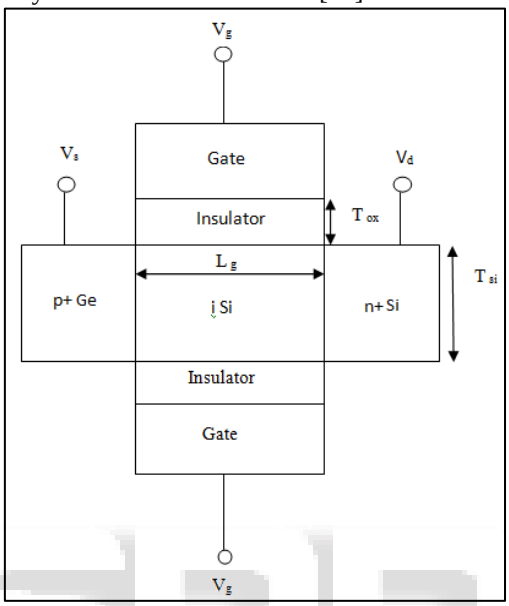

Fig. 3: Double Gate TFET

III. SIMULATION PARAMETER

The structure consists of two heavily doped n-type drain and p-type source of length 20 nm. It contains a n-type doped silicon intrinsic channel is lightly doped of width 10nm. The metal gates are separated from silicon channel by equivalent oxide layer with a power supply voltage VDD of 1V. In this work, proposed model with a channel length of 20nm is compared. The schematic view of double gate Germanium Source p-i-n Tunnel FET shown in Figure. The parameters used in simulation: Silicon Film Thickness(T_{Si})= 10nm; Effective oxide thickness (Tox) = 2nm; Source/DrainDoping =1×10^{20}atoms/cm^3, Channel = 1×10^{17}atoms/cm^3; Gate work function = 4.1ev.

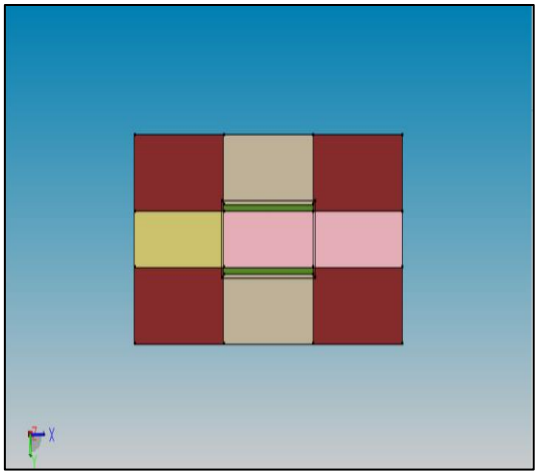

Fig. 4: DG TFET Schematic

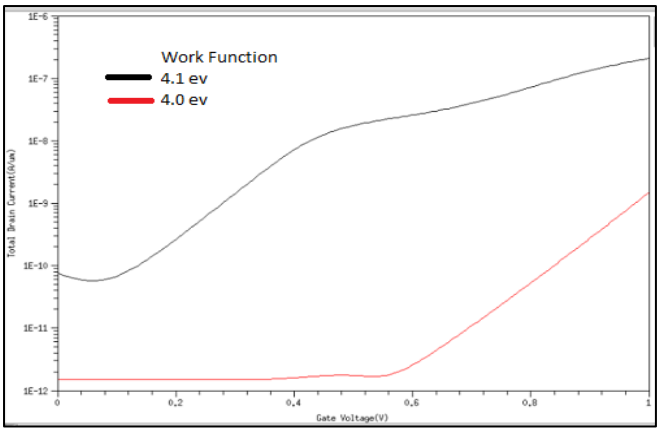

Fig. 5: Transfer Characteristics with different work function

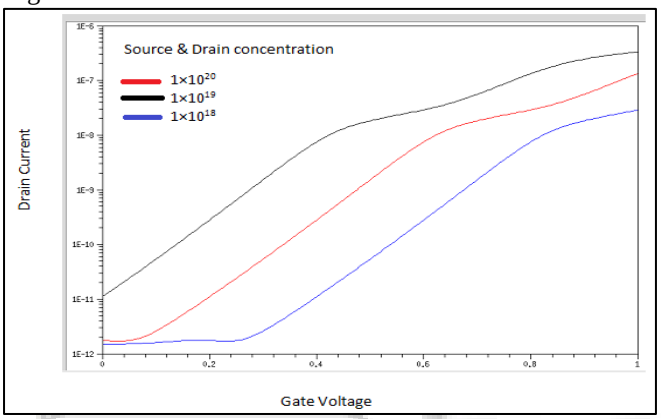

Fig. 6: Transfer Characteristics with different doping concentration

Figure 5 and 6 shows the transfer characteristics with different doping concentration of source/drain and different value work function. From the characteristics it is observed that the best characteristics obtain with 1×10^{20} atoms/cm^3 and the metal gate work function 4.1ev. The orientation used in simulation is x=(1,0,0); y=(0,1,0); z=(0,0,1).

Parameter	DG TFET
Channel Doping	10^{17} cm^3
Source /Drain Doping	1×10^{20} cm^3
Channel Length	20nm
Oxide thickness	2nm
Channel width	0.01µm
Work function of gate	4.1ev
Spacer length	20nm

Table 1: Various Parameters used for Simulation

The value of dielectric constant used in this work are 3.9 for SiO2 and One of the main parameter between the dielectric material and Silicon substrate is the conduction band offset. The value used for of conduction band offset used in this work 3.1 for Sio2. The various parameter used for device in our simulation are summarized in table. Using this proposed model, the homojunction and hetrojunction tranfer characterstics shown in figure and difference between the MOSFET nad TFET are shown with a gate dilectric Sio2 for Effective Oxide Thickness = 2nm at VDS=VDD= 1V are plotted in figures at gate length of 20nm.These figures shows the variation of Drain Current with respect to gate voltage for DG TFET.

IV. Result & Disscussion

In DG TFET process, TFETs will benefits from the added gate because the area of tunneling is increases which enhances the ON current while the value of OFF current also increase by a same factor but it remains extremely low. The difference between Germanium Source TFET and conventional TFET are use of Germanium in the source region of device. Germanium source device enhances the ON state current of TFET as compared to Silicon device. Germanium has the approximately half the band gap as compared to Silicon (0.66ev v/s 1.2ev) and the smaller effective mass ($0.06m_0$ v/s $0.2m_0$) which provides the small value of 'B' factor and enhance exponentially large ON current. It also allows more energy band overlap and small tunneling distance. In addition, I_{ON} is increase from Germanium source, I_{OFF} can be effectively reduced due to presence of Germanium-Silicon Hetero-junction which improves the overall ratio. Spacers are used in proposed structure of SiO2 material with a width of 20nm over the source and drain. Spacer with a low dielectric value (k=3.9) for SiO2 causes the improvement in ON state current. An increase in width increases the coupling between gate metal and source through spacer, thereby causing the degradation in device performance.

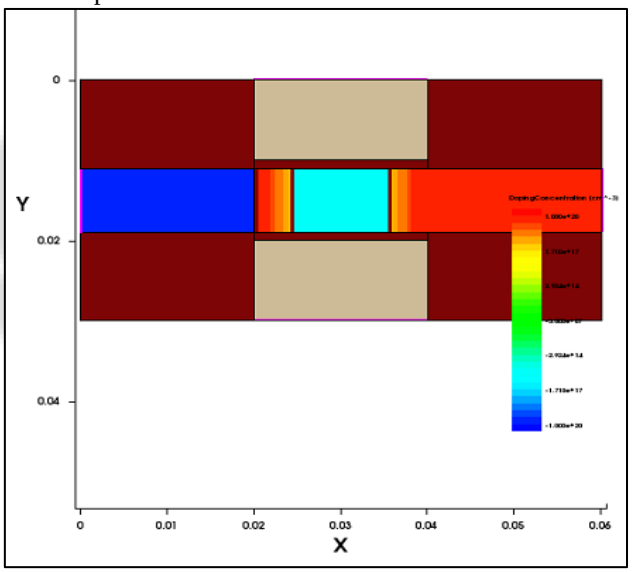

Fig. 7: DG TFET Structure

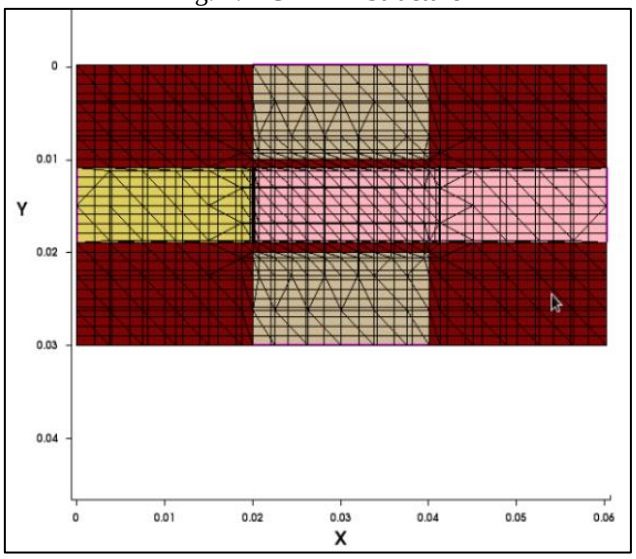

Fig. 8: DG TFET Meshing Structure

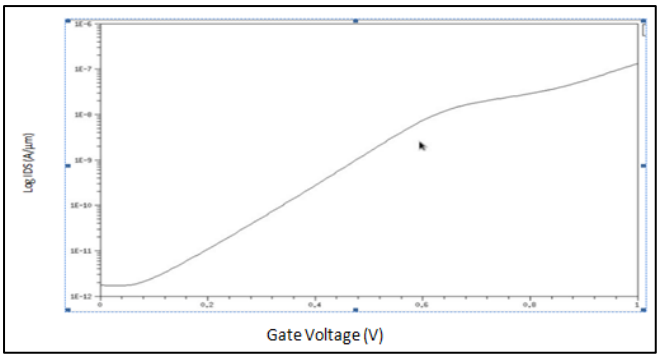

Fig. 9: Transfer Characterstics

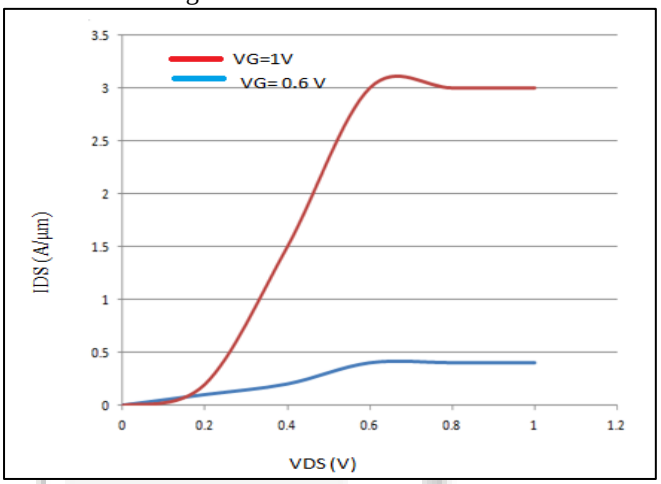

Fig. 10: Output Characterstics

Parameters	Ref[14]	ThisWork
Structure	Si TFET	Ge TFET
T_{ox}(nm)	2(SiO_2)	2(SiO_2)
L_G(nm)	70	20
V_D(V)	1	1
Tunnel Current	12.1µA	13.12µA
Leakage Current	5.4nA	1.68pA
Power	5.4nW	1.7pW

In this work, using the calibrated 2-D TCAD simulation, we demonstrate that the ON current (I_{ON}) and OFF state current (I_{OFF}) for the double gate p-i-n Tunnel FET with a silicon channel and SIO_2 as a gate dielectric are appreciably high. DG Tunnel FET is explored by using the practical design parameters which shows ON-state current 13.12µA/µm for a gate voltage of 1V and the OFF current achieved is l.68pA/µm calculated from the transfer characteristics. This improves the I_{ON}/I_{OFF} ratio for device which is simulated with 20nm gate length (present over the intrinsic region), which specify that to achieve better power switch performance, TFET is a promising device.

V. Conclusion

Scaling of TFET device is needed to increase the speed and density, but it degrades the device performance with respect to short channel effects. With increase in scaling of gate length of the TFET for the performance improvement and density, it is very difficult to maintain proper body-doping level of concentration, gate-oxide thickness and source/drain doping profile to prevent short channel effects when conventional TFETs are used. However, the large amount of doping used to suppress SCEs results in decrease in mobility and increase in junction leakage. So, to overcome all these drawbacks, several innovation methods have been employed and one of them is using the low energy band gap material and high work function is used to reducing the leakage current and achieve the high ratio of ON to OFF current so as increase the performance of device in power application.

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