Applications of Reversible Logic Gates in BCD Adder-Subtractor

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Abstract— In present time, reversible gates are being used extremely due to its capability to design more multifaceted circuits with a reduction of power dissipation. Power expenditure is the main reason in low-power VLSI design. The applications of reversible gates with Binary Coding Decimal (BCD) system reduce the power consumption during the loss of 1-bit of data in simple operations along with usual logic gates. The main focus of this paper is to provide the basics of reversible gates along with the Binary Coding System (BCD) and also compare operations of the gates in the BCD adders and subtractors. Reversible gates is a standard computing paradigm in the applications of optical, quantum computing, nanotechnology, VLSI along with low power CMOS.

Key words: Reversible logic gates; BCD adders; BCD subtractors, garbage value

I. INTRODUCTION

Now-a-days the importance of decimal arithmetic growing in commercial business framework, financial and internet cannot tolerate the inaccuracies in the system generated by binary and decimal configurations. The major significances is implement the Binary Coded System (BCD) arithmetic is to increase the speed of operations as much as possible. Using the BCD along with reversible logic gates do not loss the information or data and its computations can be complete only when system compromises of the reversible logic gates. These reversible compromise circuits generate a unique output from each input data and vice-versa, i.e. require one to one mapping between input and output data. The major objective in reversible logic design is to reduce the number of reversible gates used and garbage output produced. This paper introduces the reversible logic implementation of the conventional and new reversible logic gates along with BCD adders and subtractors. For achieving this objective, novel reversible logic gates are projected and innovative technologies are preferred for BCD adders and subtractors. Binary system is the mathematical element of digital systems so the use of the binary computation is common at present.

The binary number system has many advantages over a conventional decimal system for a high performance of the computer system. In the digital system design, there are many reversible logic gates being used in large numbers. But in current time power utilization is the main aspect, which is taken considerably. All the available logic gates are reversible. According to Launderer's there is loss of 1-bit of data that will dissipate kT*ln2 joules in form of energy, where k is k (1.38x10 -23 J/k) is Boltzmann's constant and T is the absolute temperature in Kelvin. It is observed that if data is lost in operations that can be recovered from output by applying reversible logic gates in the design. In this paper, BCD adders and subtractors unit using reversible logic gates are implemented. BCD also requires errors correction units which provide correct BCD output. There are many reversible gates are available such as Toffoli gate, Feynman gate, TNORG gate and URG gate, SBV gate, COG gate are used in the design of reversible BCD addition and subtraction unit. This will be effective by reducing the delay, error and garbage values.

II. REVERSIBLE LOGIC GATE

The main concept behind the reversible logic is the reversible function i.e. multiple output (x1; x2; :::; xn) of n Boolean variables is called reversible; when the number of outputs is equal to the number of inputs and any output pattern has a unique pre-image, in other words functions have sets of permutations are the reversible function.

From this concept reversible logic gates are designed to meet the demands of high speed without any loss of data in form of heat energy. It is have wide applications in the field of low power optical computing, quantum computing and nanotechnology. Reversible gates are used by one to one mapping of input and output vectors prevent the gate from loss of information in the form of energy. The basic input vectors of the reversible gates are 0 and 1; and the output vectors comprise of output and garbage values. Reversible logic gates are more effective in executing the Boolean expressions with high accuracy. Garbage value is the number of outputs added to make an input and output function reversible. The simple relation between the number of garbage outputs and constant inputs i.e. input + constant input = output + garbage

There are various conventional and simple reversible logic gates are available i.e NOT gate is a 1*1 gate and Feynman gate, CNOT gate and Toffoli gate, in which Feynman and Controlled NOT (CNOT) are 2*2 reversible gates. There are different types of 3*3 reversible gates such as FG, TG, PG and Fredkin Gate. The Quantum cost of 1*1 reversible gate is zero and 2*2 Reversible gates is one. Fredkin gate, Feynman gate, CNOT gate, and Toffoli gate are shown in Figures.

1) Feynman gate:

In Feynman gate, every linear function can be construct by composting only when A = 0 then Q = B, when A = 1 then Q = B'. In other case when B=0, than Feynman gate is used as a Fan-out gate.

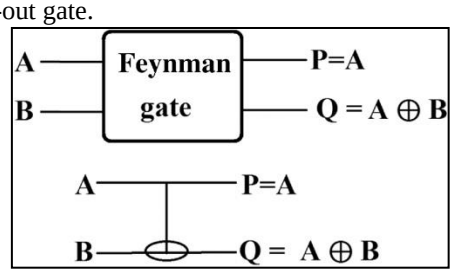

Fig. 1: Feynman Gate

2) CNOT Gate:

It is type of quantum gate that is used in the construction of a quantum computer. Circuit can be simulated to an arbitrary degree of accuracy using a combination of CNOT

gates and qubit rotations. It is a quantization of a classical gate.

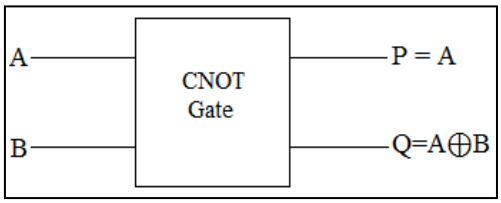

Fig. 2: CNOT Gate

3) Fredkin Gate:

It is Reversible 3*3 gate that used to maps inputs (A, B, C) to outputs P,Q and R, that having Quantum cost of 5. It also requires 2*2 Feynman gate with Quantum cost of all dotted rectangles, i.e. is corresponding to a 2*2 Feynman gate with Quantum cost of all dotted rectangle is 1, 1 V and 2 CNOT gates. Fredkin gate and its Quantum implementations are shown in Figure.

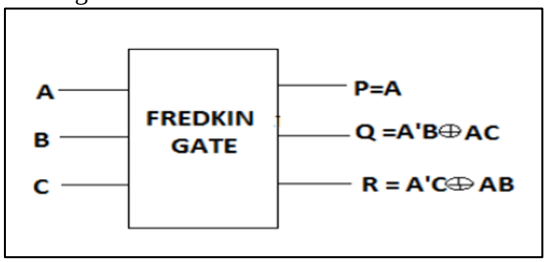

Fig. 3: Fredkin Gate

4) Toffoli gate:

It is also Reversible 3*3 logic gate with three inputs and three outputs where the inputs (A, B, C) are mapped to the outputs P, Q and R has Quantum Cost of 5 and requires 2V, 1 V+ and 2 CNOT gates.

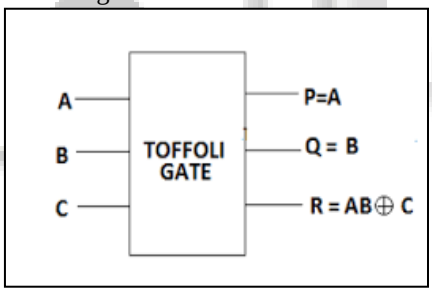

Fig. 4: Toffoli Gate

A. New Reversible Logic Gates

There are many new reversible gates are introduced with minimum quantum cost because of its reversibility characteristics. These are FG. TG, F2G, BVF, PG, R , TG with 2 more QC and TR. This new reversible gates will be also able to synthesize more complex circuits that had not been possible previously. Figures shows FG with new outputs, TG with 3 more QC, F2G with new outputs , BVF Gates with new outputs, PG with new outputs, R Gate with new outputs , TG with 2more QC and TR Gates with new outputs.

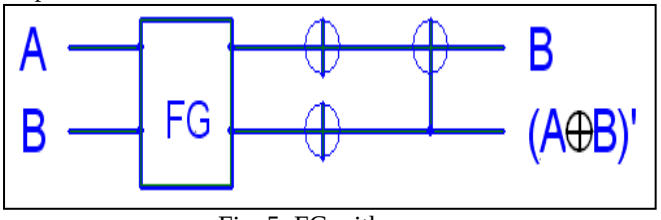

Fig. 5: FG with new

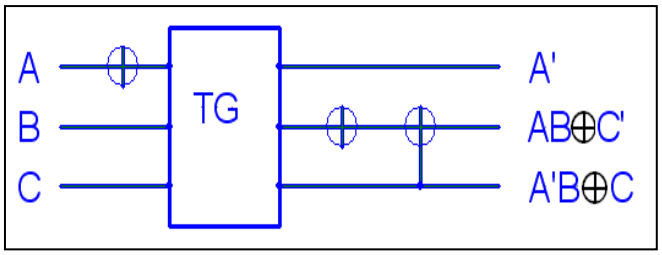

Fig. 6: TG with 3 more QC

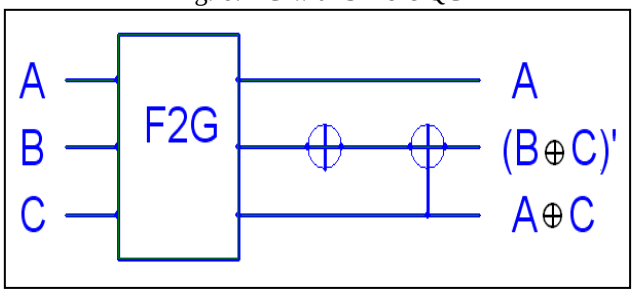

Fig. 7: F2G with new outputs

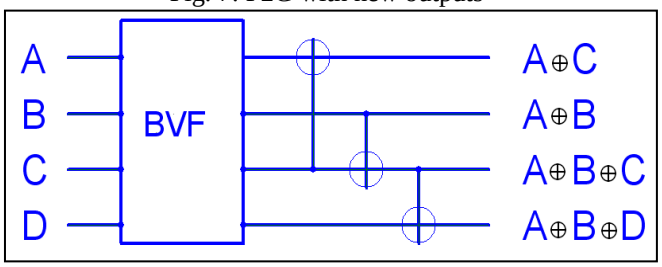

Fig. 8: BVF gate with new outputs

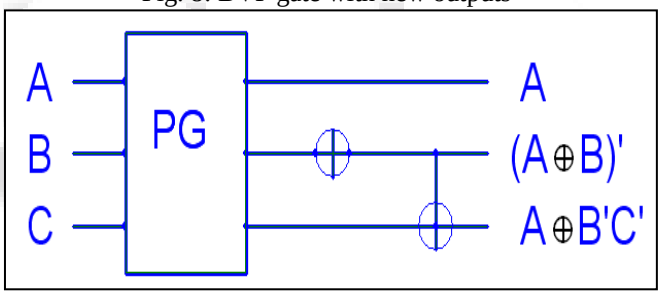

Fig. 9: PG with new outputs

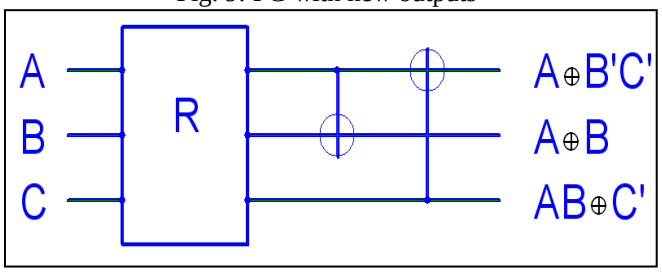

Fig. 10: R gate with new outputs

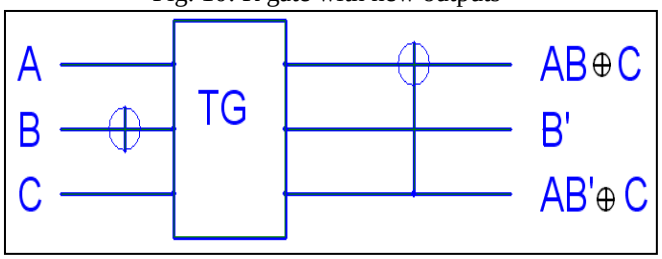

Fig. 11: TG with 2 more QC

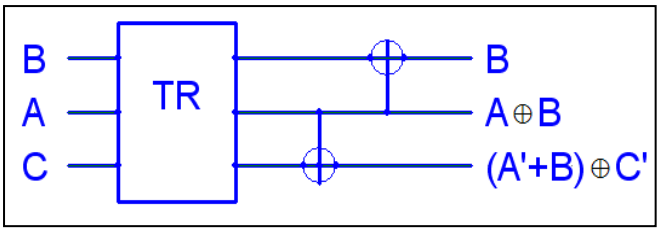

Fig. 12: TR gate with new outputs

B. APPLICATION OF REVERSIBLE LOGIC GATES

The application of reversible logic gates is given following.

1) Computer security.
2) Transaction processing.
3) Field Programmable Gate Arrays (FPGAs) in CMOS technology.
4) Computer graphics.
5) The design of low power arithmetic and data path for digital signal processing (DSP).
6) Low power CMOS.
7) Quantum computer.
8) Nanotechnology.
9) Optical computing.
10) DNA computing.
11) Computer graphics.
12) Communication

III. BINARY CODING SYSTEM (BCD)

A number digit by digit coded in binary which is a representation of decimal system is defined as Binary Coding System (BCD). For example, a number 3541 is represented as 110111010101 BCD. It can be shown that each digit of the decimal number is coded in binary and then linked together to form BCD representation of the decimal number. For this binary representation all the logical and arithmetic operations need to be described. When the decimal system contains 10 digits, then BCD digit represent by at least 4bits. If A is decimal number it represent as A4A3A2A1. One of the important notable point in BCD system is that the maximum value represent by it is "9" only. The representation of two digit decimal system i.e. AB is two digit number and it represent in BCD A digit as A4A3A2A1A and B digit as B4B3B2B1. In usual approach of binary coding, two digits are added using BCD adder during that the resultant seems to be exceeding 9 in an overflow, which can be in BCD by adding the binary equivalent of 6.

A. Binary Adders

These binary adders are not only vital in addition functions, but also in performing many others basic arithmetic operations such as subtraction, multiplication, increment and decrement. This all operations needed an efficient adder for better performance of a processor in Algorithmic logical unit (ALU).

Binary addition consists of following possible elementary operations, this includes;

0+0=0
0+1=1
1+0=1

1+1= 0, and carry 1 to the next more significant bit, (1+1=10)

Starting three addition functions generate a sum whose length is one digit, but when both augent and addend bits are equal to 1, the binary digit consist of two digit. The high bit obtained in this operation is called carry. The circuit operation that performs addition with 2 bits is called half adder while the addition of 3 bits is known as Full adder.

1) Ripple Carry Adder

When a simple execution of higher operations of adders take place for two operands A and B by carrying out by dropping n of these basic adder units, this is known as a ripple carry adder. The design of this type of adder is very simple and easy but sometimes it suffers from delay causes. Therefore the next stage needs to wait for carry bit from previous stage.

2) Carry Select Adder

In previous adder, there is delay issues of input carry in next stage from previous stage when sum and carry out take place. In order to overcome problem of delay, in ripple adder, Carry select adder is introduced which pre-computes the sum and carry out operations when input carry either 0 or 1. This pre-computation of sum minimize the delay of rippling of carry. It requires more hardware but due to advantages of pre-computation or less delay, uses more.

3) Carry Look ahead Adder

Another one technique is evaluated to derive the Sum and Carry outputs by using the terms Generate and Propagate. Generate term introduce the carry-out independent of the carry-in, value of carry-in not affect the carry-out i.e. always 1, incase when input A and B both are 1. Thus Generate=A.B. Propagate terms allocate the input carry as output carry when one of any inputs is high and Propagate (P) defined as P = A⊕B. In Propagate operation, the Carry-out depends on the Carry-in.

4) Prefix Based Adders

The prefix based adder consists of 3 steps i.e. Pre-computation stage, prefix network stage and post-computation stage. Firstly, pre-computation computes the carry Propagate and carry Generate bits for each input data pair. Next prefix network stage calculates the final carries from the carry Propagate and carry Generate bits. Carry computation associate with this operator '○' which correlate the pairs of Generate and Propagate. And in last stage post-computation stage computes the final sum for carry generated in prefix network stage. These designs are very much efficient in terms of delay as compared to carry-select and carry look-ahead adders.

B. Binary Subtractors

Similar to adders, subtractors circuits take two binary numbers as input and subtract one binary from other binary; it gives two outputs, difference and borrows.

Binary subtractors consists of following possible elementary operations, this includes;

0 - 0 = 0
1 - 0 = 1
1 - 1 = 0

0 - 1 = 1, and borrow 1 from the next more significant bit

Binary subtraction can be understood from the following analysis.

1) Minuend X
2) Subtrahend Y
3) Difference D

4) Borrow B

In this BCD subtraction, the nine's complement of the subtrahend is added to the minuend. In the subtractors arithmetic, the nine's complement is computed by nine minus the number whose nine's complement is to be computed. Using nine's complement in BCD subtractors, there can be two prospective;

The sum after the addition of minuend and the nine's complement of subtrahend is an invalid BCD Code. The final result will be the positive number represented by the sum.

The sum of the minuend and the nine's complement of the subtrahend is a valid BCD code which means that the result is negative and is in the nine's complement form.

1) Half Sub-tractors

It is used for subtracting one single binary digit from another single binary digit. In this half-subtractor, circuit is designed to perform subtraction of two bits which has two inputs minuend and subtrahend and two outputs difference and borrow. The expressions for sum and difference outputs are same in case of half-subtractor and half adder. In case of half subtraction the expression for borrow is more or less same with carry of the half adder. The Boolean expression for half-subtractor defined as;

$$Difference=A'B+AB'=A\oplus B$$

$$Borrow=A'B$$

C. Full Sub-tractors

It is combination circuit that performs subtraction of three bits, that is minuend, subtrahend, and borrow, so there is possibility of multi-bit subtraction due to cascading. There are basically two outputs difference D and borrow B. The borrow output shows that the minuend bit requires borrow 1 from the next minuend bit. In comparison of full subtractor and full adder, the difference output D is same as sum output and borrow output similar to carry-out.

The Boolean expression for half-subtractor defined as;

$$Difference=A'B'C+A'BB'+AB'C'+ABC$$

Reduce it like adder

Then We got

$$Difference=A\oplus B\oplus C$$

$$Borrow=A'B'C+A'BC'+A'BC+ABC=A'B'C+A'BC'+A'BC+A'BC+A'BC+ABC \text{ ----------} > A'BC=A'BC+A'BC+A'BC$$

IV. Results & Conclusions

This paper focused on optimizing arithmetic logical units (ALU) which when used together lead to efficient realization of reversible logic gates and binary adders and subtractors. The applications of reversible gates can be used for designing large reversible system which can be used in ultra low power digital circuits and quantum computers. It is also observed that due to optimization the power dissipation, speed and hardware complexity is reduced. The contribution of the paper is found the applications of reversible gates and BCD system in development of efficient circuits that address the problems of fan-out, delay and power consumption. Another output of this paper which has been shown to be efficient in terms of speed of operation without resulting in extra power consumption. Since such a reversible gates and BCD plays a major role in an ALU circuits. The comparison of BCD adders and subtractors are efficient in terms of delay while consuming less energy. Finally all the individual arithmetic logic units if combined with the fundamentals of reversible logic gate and BCD system to resulting in an efficient design to those existing in literature.

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