Design and Implementation of I²C Interface for Multiple Access

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Abstract— This paper focuses on the design of I²C interface in which an single master is controlling the two slaves, which consists of a bidirectional data line i.e. serial data line (SDA) and serial clock line (SCL). This protocol can support multiple masters as well as multiple slaves. I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices and is used for faster devices to communicate with slower devices and each other without any data loss. It requires only two lines for communication with two or more chips and can control a network of device chips with just two general purpose I/O pins whereas, other bus protocols require more pins and signals to connect devices. The complete module is designed in Verilog and simulated in ModelSIM.

Key words: I²C Interface, Multiple Access

I. INTRODUCTION

The I²C bus which is a bi-directional, two-wire and serial communication standard is also known for its user friendly protocol. It is designed in such a way to have a simple interconnection but also for efficient integrated circuit (IC) control. Here the system is using two bus lines, namely SCL (Serial Clock) and SDA (Serial Data) that carry information between the ICs connected to them. By the use of this bus based protocol a number of applications can be designed; however, this application discusses only the Master-Slave system implementation. I²C bus refers to the protocol which governs its action based on some rules, here the I²C bus is known for serial data communication between master to slave and also between slaves which can act as a master and master as a slave depending upon the read or write statement.

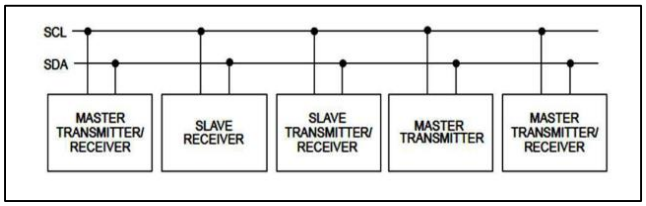

Fig. 1: I²C bus configuration using masters and slaves.

I²C-bus also helps to supports any IC fabrication process i.e. it may be NMOS or CMOS or bipolar. Each device is recognized by a unique address fed by master within the clock pulse (whether it's a microcontroller, LCD driver, EEPROM, ADC or RTC) and can operate as either a transmitter or receiver, depending on the type of function user wants to perform on the device. Obviously an LCD driver is only a receiver, whereas a memory can act as both receiver and transmitter for data.

II. I²C PROTOCOL

To depict the logic behind the serial communication is that the I²C master will respond for the connected slaves for operation to be done on them. The operation is done in Verilog platform, it consist of the parallel interface which helps the user for the desired operation to be done. A new design which cooperates the I²C master so as to create the serial peripheral interface to I²C. Here the I²C is considered to be half duplex transmission based system which consists of two lines i.e. serial data line and serial clock pulse. Devices on the bus are arranged in such a way that as to make 0 it has to pull the line to ground and to make 1 it has to release a line.

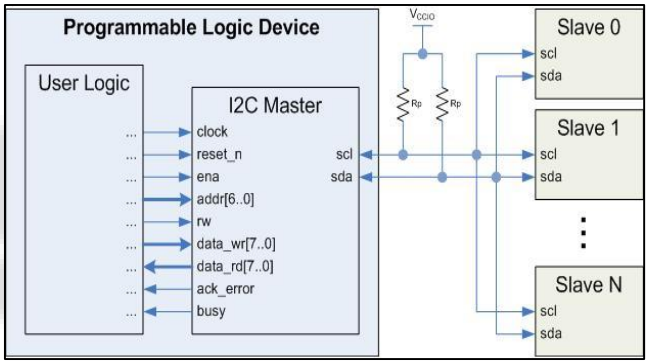

Fig. 2: I²C Bus Connected with Master and number of Slaves

Here according to the below figure, here the master is arranged in such a way that there will be a connection of slaves which helps to run the operation of transferring the data on the serial Peripheral interface of I²C interface. Here refers to the interconnection of multiple slaves connected in such a way that once the master send the signal to trace the required slave then all slaves will see the upcoming signal but the respond will be done by the addressed slave only. After that all the other one except one slave are considered to be in idle state or in sleep mode which helps the user to interface properly.

III. STATE MACHINE:

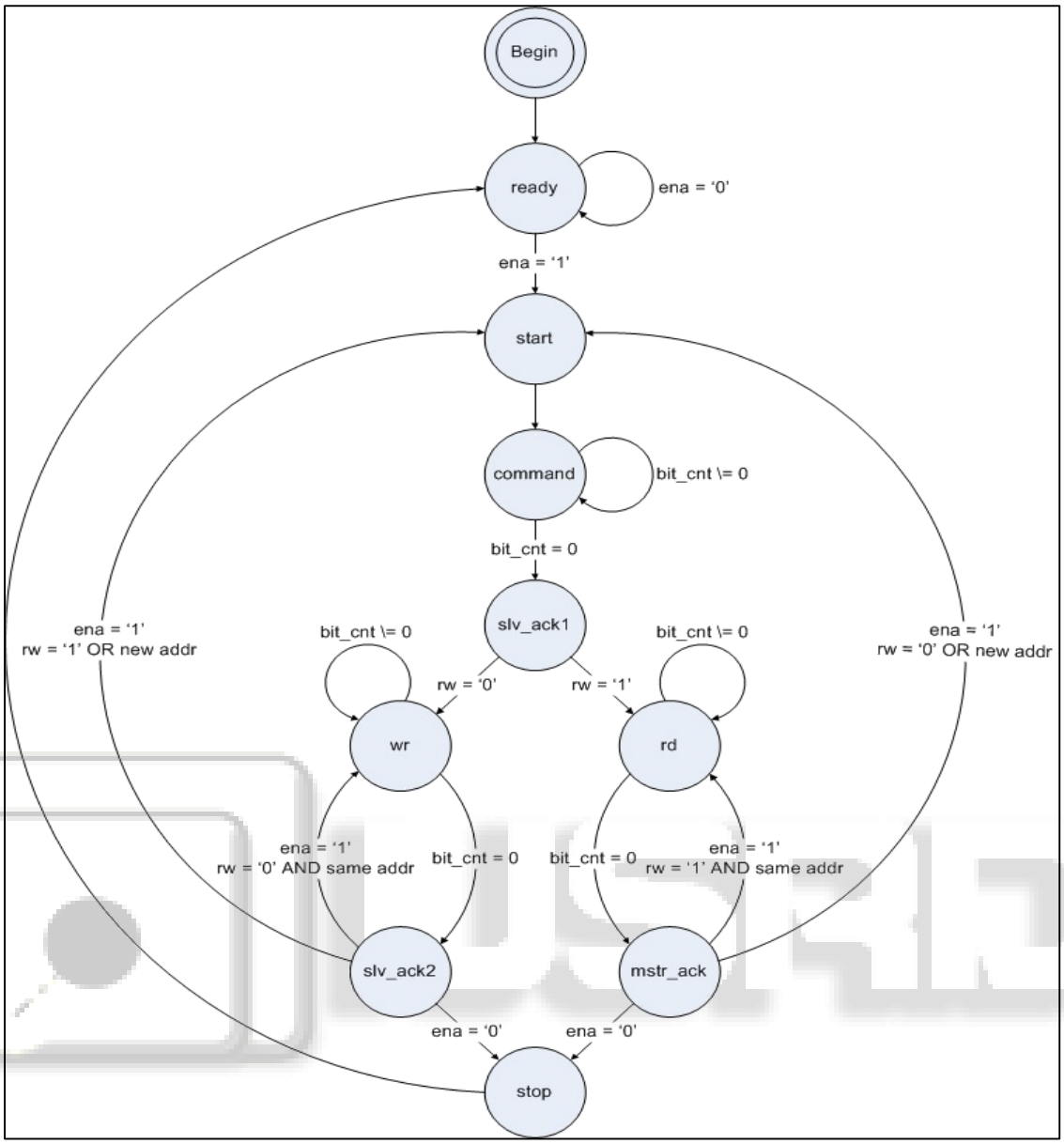

Fig. 3: I²C based State Machine

The state machine tells the overall functioning of the I²C bus protocol by means of considering the overall analysis of the different states. To start the operation here comes the start signal which depicts the starting bit transferred by the system, i.e. whether the signal given is master or slave, now once it is received, then the further transfer of the slave address is fed. Now the addressed slave will respond by the acknowledgement signal. Once the RW bit is 1 then the application of write will be done on the slaves and if RW bit is 0 then the read operation will be performed. Once this acknowledgement is received by the master from slave then the further RW is fed, after that the data governed by the 8 bit is depicted as the data to be written on the slave.

However vice versa is done for the read operation by means that the RW is said to be 0, after this the slave will be respond over the depicted data bit of 8 bits for the read operation. After all such operation on the master and slave the acknowledgement signal will be transferred to slave and master. This shows that the communication can be done on the bus using the I2C bus protocol. But for further operation new address of the slaves can be traced to send the data on the same bus.

IV. FUNCTIONAL DESCRIPTION

The functional description of I2C master is described in the Verilog HDL. That is called design module. The test bench program is developed to test the design module. The test bench gives the input to the design module & verifies the output. The test bench is written in such a way that the design module can be checked in all possible conditions. The signals given from the test bench to test the working of the prototype design of the I²C master are:

ena
ack
en
in_data
sda_r

V. SIMULATION RESULTS

The I2C single master for two slaves has been designed in Verilog and simulated in simulator tool Modelsim which is

used to verify the design functioning. Here for the designing and verifying the results the data and the slaves address are changed accordingly, so as to perform the operation. This design works for both read and write cycle.

1) Figure 4, shows that the single master is controlling the single slave, here slave address is called and the data has to be written on it with acknowledgement. Data is-1110000 and the address so called is-11111010
2) Figure 5, shows the single master is arranged for single slave when the data and the slave address is changed. Here the data here used is 1010000 and the address so called is 11011010.
3) Figure 6, here in this simulation result the master is going to control two slaves to accomplish the objective of this research work. The data is used here is 1010000 and the address of the slave so called is 11011011

The results of Master and Slave RTL Structure is also assigned in this paper.

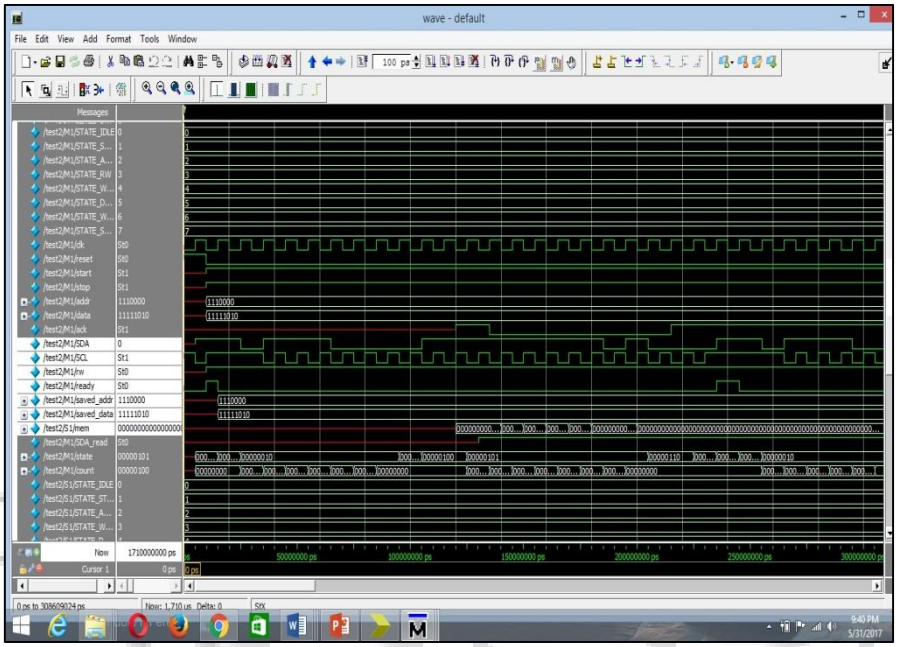

Fig. 4: Master to Slave Transmission.

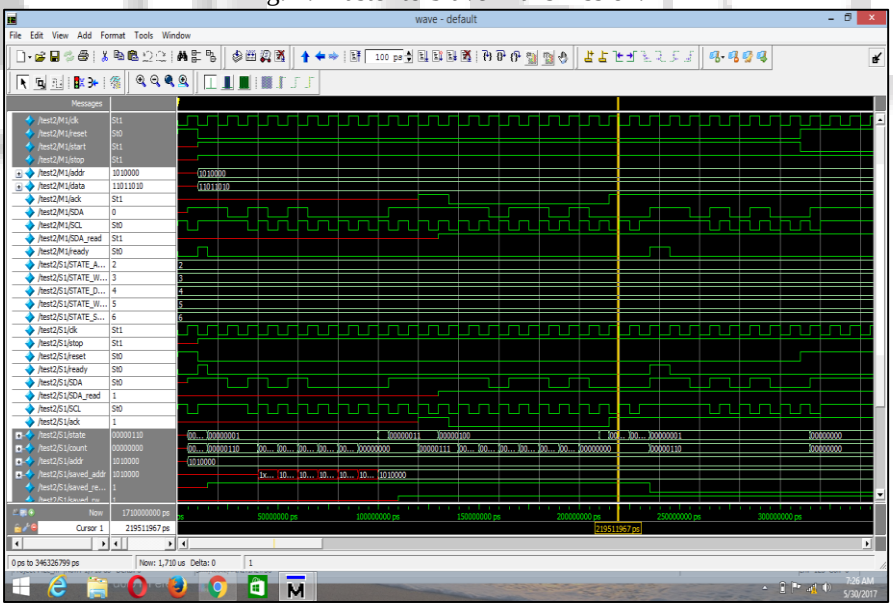

Fig. 5: Master to Slave Transition for different Address and Data

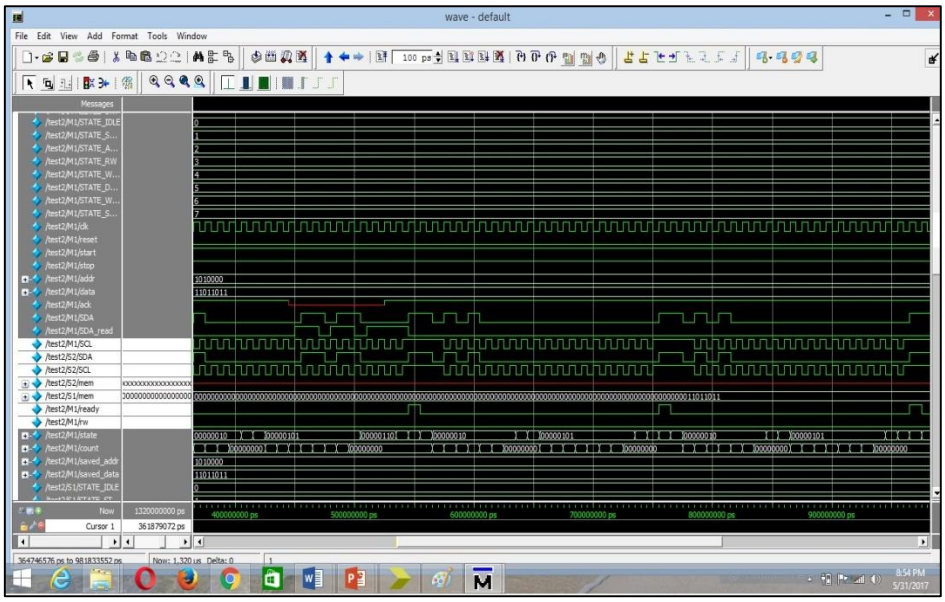

Fig. 6: Master controlling two Slaves

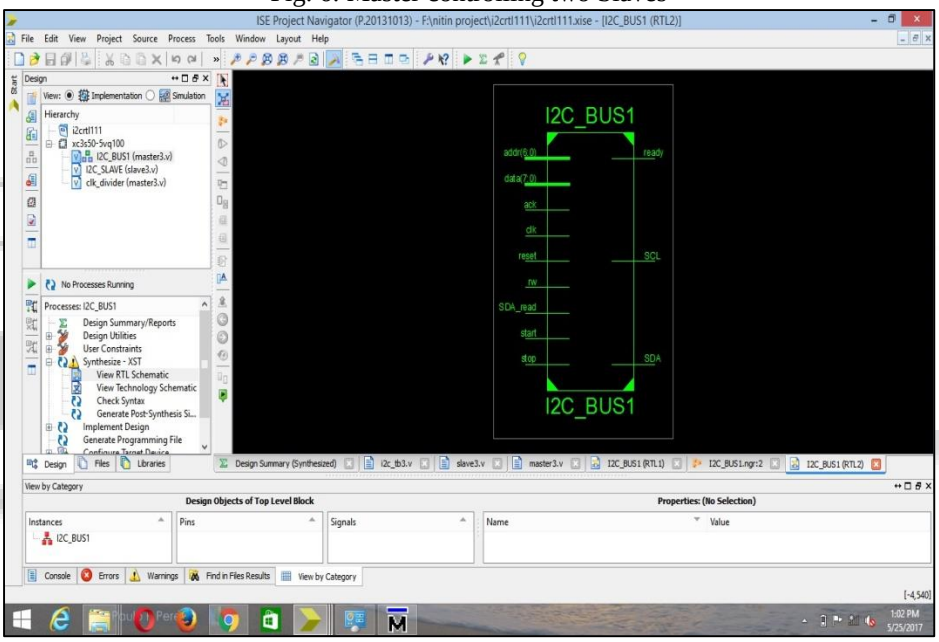

Fig. 7: RTl structure of Master

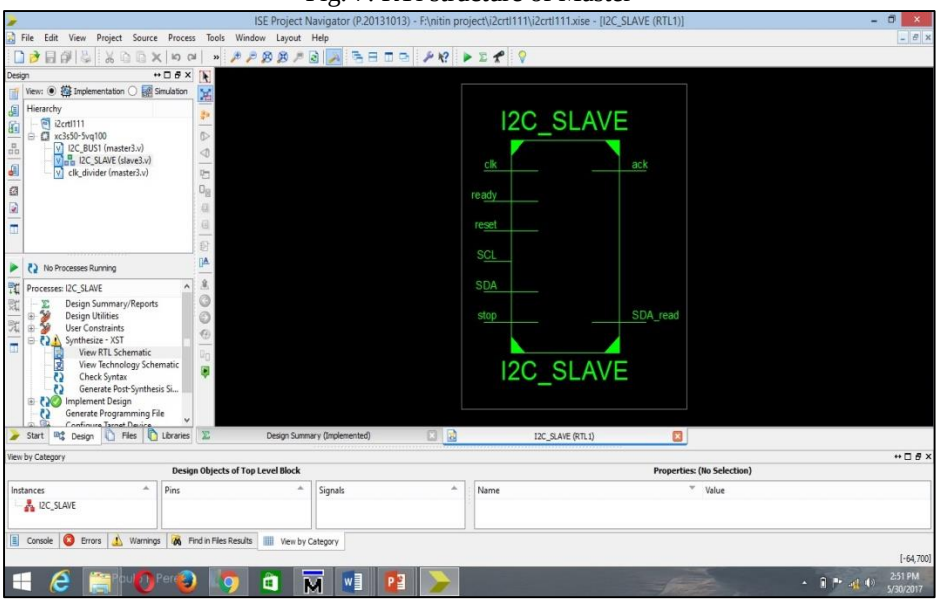

Fig. 8: RTl structure of Slave.

VI. RESULTS

The data transmitted by master is successfully stored and read by it.

VII. CONCLUSION & FUTURE SCOPE

The results of simulation and the data fed agrees the desired behavior of the i2c bus controller. The interfacing of the 2 slaves with a single master governs that the platform is also suitable for the more number of slaves. The design of I2C controller is done by means of Verilog HDL and the simulation is governed by the Model-sim as a simulator. In future aspects the multi-masters and multi-slaves can be done and the smart slaves and smart masters as a can also be designed.

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