Design & Analysis of on Chip Charge Pump Circuits for Low Power VLSI Circuits

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Abstract— Due to advancement of Digital India a lot of peoples move to digital era. Today Life cannot be think without electronic gadgets. Regarding portability power dissipation is main constraint. Consumer demands more features in small size and extended battery life at a lower cost Charge pump circuit is widely used in integrated circuits (ICs) due to the continuous power supply reduction which is dedicated to several kind of applications of low voltage phase locked loop (PLL), flash Memories & DRAM's smart power, switched capacitor circuits, non-volatile memories, operational amplifiers, voltage regulators, SRAMs, LCD drivers, piezoelectric actuators, Radio frequency antenna switch controllers, etc. Charge pump are used in these application, basically it is DC to DC converter which have capacitor instead of an inductor or transformer for energy storage. In this paper Dickson, static & dynamic charge pump has been analyzed in terms of delay, power and conversion ratio.

Key words: PLL, LCD, DRAM Conversion Ratio

I. INTRODUCTION

Electronic devices have become inseparable parts of people's lives in modern times for portable consumer. The basic requirements of the people's are portable, thin, lightweight and multifunctional consumer electronic devices such that mobile phone, laptops is increasing day-to-day. These portable devices are charged from single battery and they should be capable to operate for an extended phase of time. In electronics industry, there are lot of devices usually have a large number of circuit sub-systems which require different voltage domains to conduct the device. Consequently, the requirement for multiple voltage creation from a single voltage battery operated power supply imposes design challenges to achieve high voltage conversion efficiency, low power dissipation low output ripple voltage and low reverse current.[1,2]

Basically there are such a two way by which devices can be charged using charge pump with inductor and without inductor DC to DC power convertors. Generally Charge pumps with inductor less DC-DC power converters are used which step up or step down the voltage level of the input power supply to generate higher output voltages.[3] Charges pump use charge transfer switches and capacitors to transfer the charge packets to the output loading circuit. Charge pump utilize switches and pumping capacitors only so they can be without difficulty implemented with conventional integrated circuit CMOS technology.[4]

In Microsystems, charge pump are frequently fully built on-chip, instead off-chip, to simplify chip and board design and decrease costs. Integrated implementations of charge pump develop integrated capacitors as storage elements and transistors as transfer switches, where the 2-switch terminals are source and drain, and the gate terminal is used to manage the switch state. Many MOS-based systems have need of multiple supply voltage levels for their functional blocks and therefore are capable of with charge pump. Charge pump are helpful in many different types of circuits, together with switched-capacitor circuits, low-voltage circuits, DRAM circuits, EEPROM's and transceivers.[5]

II. CONCEPT OF ON CHIP CHARGE PUMP

The basic principle of charge pump is doubling the input voltage as shown in fig.1&2. Here consider all the switches and capacitors are ideal, that means there is no leakage current in the capacitors and electric charge transferring is instantaneous. In this process there are two phase, phase I & phase II.

A. *Phase I:*

phase I is charging mode. In this phase switches S_2& S_3 are shorted (closed) and switches S_1& S_4 are opened. And capacitor C_F is charged up to power supply V_{DD}.

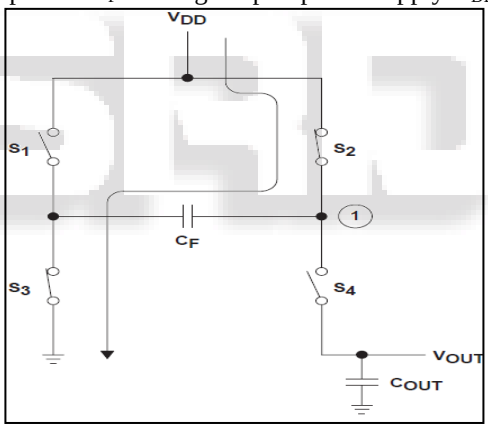

Fig. 1: Charging Phase of charge Pump

B. *Phase II:*

phase II is transfer phase. In this phase switches S_1& S_4 are shorted (closed) and switches S_2& S_3 are opened. After that Capacitor C_F is discharged and output capacitor (C_{OUT}) is charged .therefore voltage at node1 is ideally:

$$V_1 = V_{DD} + V_{CF} = 2.V_{DD}$$

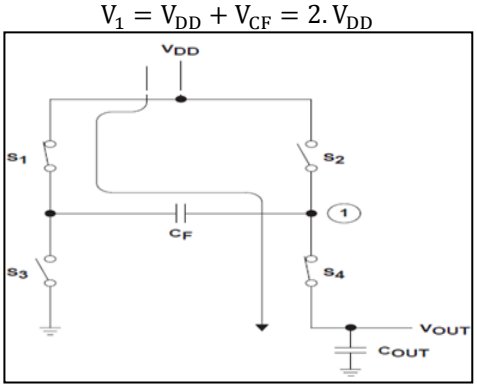

Fig. 2: Transfer phase of charge pump

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In other words, we can also write

$$(V_{OUT} - V_{DD}) \times C = V_{DD} \times C_F$$

Or

$$V_{OUT} = 2 \times V_{DD}$$

Therefore, the C_{OUT} will ideally be charged up to twice times of supply voltage after reaching the steady state. The actual voltage at output capacitor will be a little less than twice times of supply voltage.[6]

III. IMPLEMENTATION OF CHARGE PUMPS

A. Dickson charge pump:

The Dickson charge pump consist of diode connected five MOS transistor, five capacitor and two pumping clocks as shown in fig: 3.1. The charges in the Dickson charge pump can be flow only in one direction due to MOS transistor. This charge pump has 2-phase non overlapping clock pulse namely clock and clock1. The amplitude of the clocks is equivalent to amplitude of power supply voltage V_{DD}. The diode connected NMOS are used to transfer charges from input to output in each stage

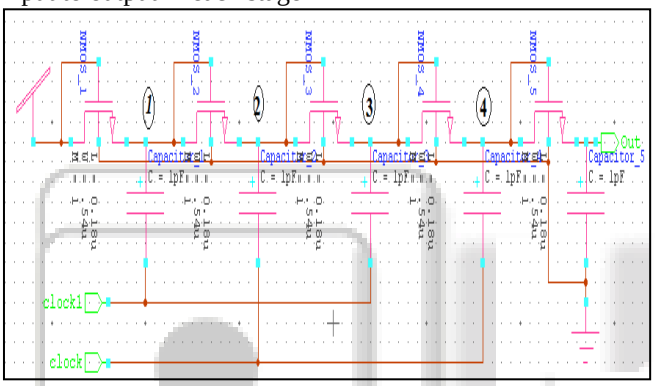

Fig. 3.1: schematic of Dickson charge pump

1) Case I: When the Clock is low and clock1 is high

Then NMOS_1, NMOS_3, and NMOS_5 are turned on and NMOS_2 & NMOS_4 are switched off, after that the charge is transferred to node1 from VDD, the charge in node 2 is transferred to node 3, and the charge in node 4 is transferred to V_{out}.

2) Case II: When the Clock is high and clock1 is low

Then NMOS_2 and NMOS_4 are turned on and MNOS_1 & MNOS_3 switched off, After that the charge is transferred to node 2 from node 1, and charge in node 3 is transferred to node 4. Therefore, the output voltage of Dickson charge pump circuit is:

$$V_{out} = \sum_{i=1}^{N+1} (V_{DD} - V_{tn})$$

Where

V_{tn} = threshold voltage of the diode-connected NMOS in the i-th stage and

N = stage number of stage

B. Static charge pump:

The diode voltage drop i.e. Threshold voltage is removed by using charge transfer switch (CTS) in parallel with the diode connected device (MOS transistor) in order to improve the performance in low voltage applications. Therefore Static and dynamic CTS techniques have been found. CTS are used rather than the diodes to transfer the charge between nodes. Though the diodes are used only for setting up the initial voltage at each pumping node. The schematic of Static charge pump is shown in fig 3.2.

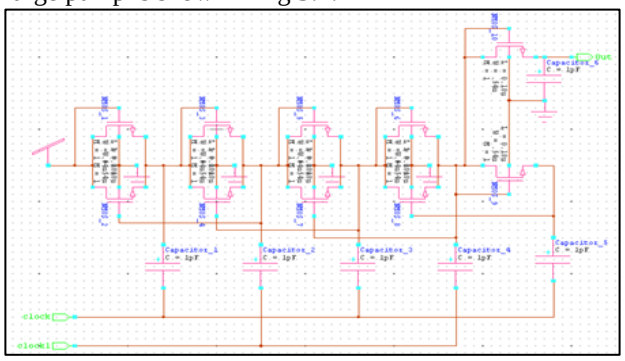

Fig. 3.2: Schematic of Static Charge Pump

The voltage pumping gain per stage can be now expressed as

$$Gv = \Delta V$$

Static CTS technique uses higher voltage from the next stage for controlling the operation of the CTS's.

The functional workings of static charge pump as follows:

1) Case I: When the Clock is high and clock1 is low:

Then NMOS_2 transistor is switched ON. Thereby initial voltage is setup at node2. The gate to source voltage of NMOS_4 is $2\Delta V$. If this gate to source voltage is greater than the threshold voltage of the NMOS_4. If this condition is satisfied, NMOS_4 is turned ON.

2) Case II: When the Clock is low and clock1 is high:

Then NMOS_3 will be switched off. Therefore gate to source voltage of NMOS_4 is $2\Delta V$. There is such a condition which occurs i.e. $2\Delta V < V_{tn}$, where V_{tn} is the threshold voltage of MOS transistor. Therefore NMOS_4 will be switched off, which is not valid. Thus performance of this charge pump is decreased.

C. Dynamic charge pump:

In this charge pump CTS is accompanied by auxiliary circuit that contains NMOS &PMOS transistors so that the charge transfer switch can be completely turned off in required period and can be turned on by the high voltage of the next stage as in static CTS technique Dynamic CTS format is used to remove the body effect and the voltage loss problem occurs in the previous charge pump.

All diode-connected MOS transistors are NMOS_1, NMOS_3, NMOS_7, and NMOS_10 used to set up the initial voltage. However, these MOS transistor are not involved in the CTS operation. NMOS CTSs are NMOS_2, NMOS_5, NMOS_8 and NMOS_11 used to control the switches. In addition, the backward control scheme is employed to obtain voltage from the previous stage to boost the gain, Clock and Clock1 pulses are out-of-phase but with the amplitudes of power supply voltage [45]. The schematic of Dynamic charge pump is shown in fig 3.3

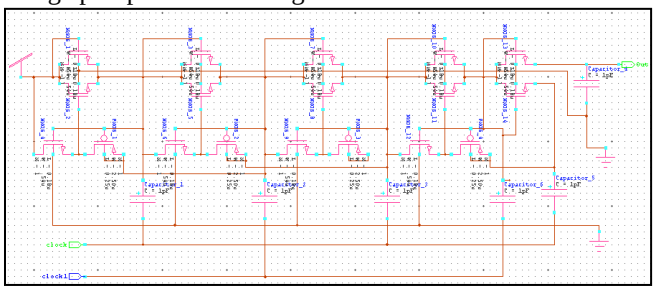

Fig. 3.3: Schematic of Dynamic charge pump

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The functional workings of Dynamic charge pump as follows:

1) Case I: When the Clock is high and clock1 is low:

Then , the source-to-gate voltage of PMOS_2 is 2ΔV , the gate-to-source voltage of NMOS_6 is zero, and NMOS_5 will be switched ON if and only if: $2\Delta V > |V_{tp}|$ & $\Delta V > V_{tn}$

Where

V_{tp} = threshold voltage of PMOS

V_{tn} = threshold voltage of NMOS.

2) CaseII: When the Clock is low and clock1 is high:

Then, PMOS_2 will be switched OFF and NMOS_6 will be switched ON if and only if MP2 will be turned OFF and MN2 will turn ON If:

$$2\Delta V > Vtn$$

NMOS_5 will be fully turned OFF. CTS's are hard to turn ON in low voltage environment. So that dynamic CTS method is not helpful at low voltage applications.

IV. RESULT & DISCUSSION

A. Dickson Charge Pump:

The diode-connected NMOS transistors are used in the Dickson charge pump rather than the diodes for implementing the circuit in standard CMOS process. The diode connected NMOS transistor permit the charge flow only in the direction of the output stage in ideal situation. The charges are pushed to the next from one stage, resulting in higher DC voltage at the output.

The simulation of Dickson charge pump is done at 180nm technology and W/L ratio = 540/180 of NMOS transistor and output waveform is shown in fig: 4.1

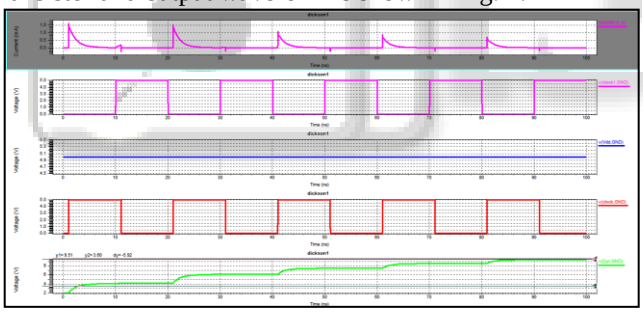

Fig. 4.1: Output Wave Form of Dickson Charge Pump

Voltage analysis of the Dickson charge pump is obtained at different V_{DD}, constant V_{DD}, same Vdd, same clock pulse, different clock pulse and constant clock pulse. At same condition power consumption and delay, also obtained. On varying the input voltage change in output voltage is observed. Its different parameters such as output voltage, power consumption, delay.

S. N.	Vdd (v)	Clk (V)	Clk (v) 1	o/p (v)	Power Consumption (uW)	Delay nS	Conversion Ratio
1	5	5	5	9.5	334	1.77	1.9
2	1.8	1.8	1.8	2.5	267	3.25	1.38
3	1.6	1.8	1.8	2.5	232	3.8	1.56
4	1.4	1.8	1.8	2.42	225	4.26	1.72
5	1.2	1.8	1.8	2.34	217	4.7	1.95
6	1	1.8	1.8	2.27	209	5.8	2.27

Table 4.1: Output Voltage, Power consumption, delay and conversion ratio at different Vdd and same clock pulse of Dickson

B. Static charge pump:

Static charge pump uses CTS in addition to Dickson charge pump to remove the problem of voltage threshold drop. Static CTS charge pump employing dynamic switches to increase the voltage pumping gain. The vital idea behind these multipliers is to use MOS switches with accurate on/off characteristics to direct charge flow.

The simulation of static charge pump is done at 180nm technology and W/L ratio = 540/180 of NMOS transistor and output waveform is shown in fig:4.2

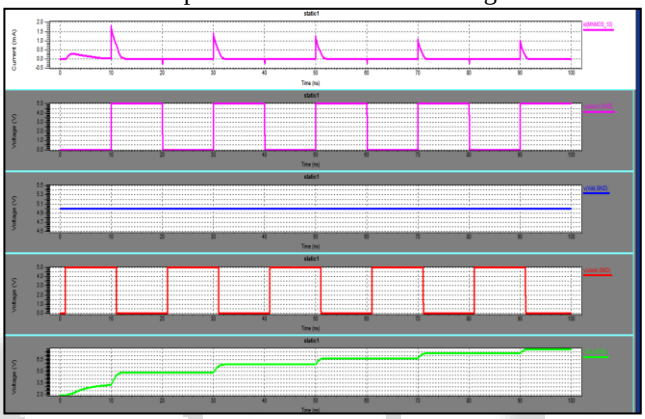

Fig. 4.2: Output Waveform of Static Charge Pump

S. N.	Vdd (v)	Clk (V)	Clk (v) 1	o/p (v)	Power Consumption (uW)	Delay nS	Conversion Ratio
1	5	5	5	7.88	402	.94	1.57
2	1.8	1.8	1.8	2.6	397	1.4	1.44
3	1.6	1.8	1.8	2.5	381	1.5	1.56
4	1.4	1.8	1.8	2.4	370	1.52	1.71
5	1.2	1.8	1.8	2.23	362	1.74	1.85
6	1	1.8	1.8	2.1	350	1.89	2.2

Table 4.2: Output Voltage, Power consumption, delay and conversion ratio at different Vdd and same clock pulse of Static Charge Pump.

C. Dynamic charge pump:

This is a another charge pump which eliminates the reverse charge sharing problem is solved by using dynamic control of the CTS's .In this charge pump, each CTS is accompanied by an auxiliary circuit that contains NMOS and PMOS transistors. Therefore CTS's can be turned off completely in the required stage and can be turned on by high voltage of the next stage as in static CTS technique. The simulation of Dynamic charge pump is done at 180nm technology and W/L

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ratio = 540/180 of MOS transistor and output waveform is shown in fig: 4.3

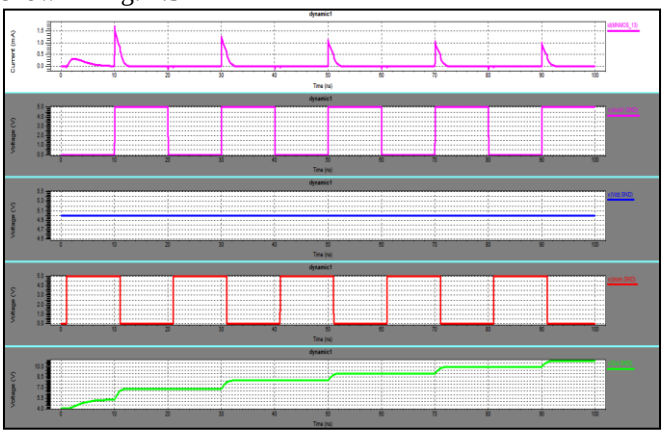

Fig. 4.3: Output Waveform of Dynamic Charge Pump

S. N.	Vdd (v)	Clk (V)	Clk (v) 1	o/p (v)	Power Consumption (uW)	Delay nS	Conversion Ratio
1	5	5	5	9.4	3790	.98	1.88
2	1.8	1.8	1.8	2.80	436	1.7	1.55
3	1.6	1.8	1.8	2.70	421	1.55	1.68
4	1.4	1.8	1.8	2.60	406	1.21	1.89
5	1.2	1.8	1.8	2.57	397	1.68	2.14
6	1	1.8	1.8	2.50	383	1.43	2.5

Table 4.3: Output Voltage, Power consumption, delay and conversion ratio at different Vdd and same clock pulse of Dynamic Charge Pump.

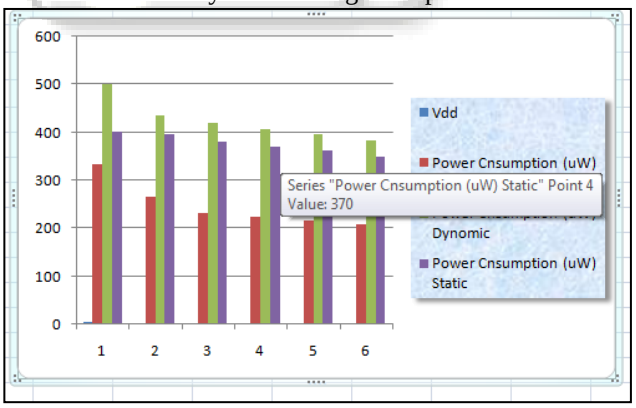

Fig. : Graphical View of power consumptions

V. CONCLUSION

On the analysis of 3 types of charge pumps concluded that output and Power conversion ratio of Dickson charge pump is high at same input power supply and same clock pulse. Delay of static charge pump is less. We can use in VLSI circuits as per requirement. There is always need to trade of between area power & delay. Dickson charge pump not applicable for low voltage.

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