Study and Analysis of CMOS Inverter and Layout Implementation

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Abstract— In this paper, Complementary Metal Oxide Semiconductor (CMOS) is analyzed for application to low power, mixed signal environments. A small CMOS cell library is developed and optimized for several different performance requirements. The cells are then applied to the generation of ripple adders and pipelined CORDIC structures and compared with equivalent MCML circuits. CMOS CORDICs are designed which can operate from 130MHz to 330MHz with power consumption varying between 4.5mW and 18.8mW. These power results are up to 1.5 times less than MCML CORDICs, with equivalent propagation delays. Design was done in a 0.25μm standard MCML process from ST Microelectronics.

Key words: Power, CMOS Inverter, Layout Implementations

I. INTRODUCTION

The basic functions is the NOT operation in digital logic. A CMOS inverter circuit provides the NOT operation in a straightforward manner. The inverter is fairly simple and is built using an nFET-pFET pair that shares a common gate. The circuit gives a large output voltage hang and only dissipates significant power when the input is switched; these are two important properties of static CMOS inverter. In This paper provides a detailed examination of a CMOS inverter and sets the foundations for most high-level CMOS design styles in the rest of the book. The recent advances in CMOS technology have allowed rapid growth in the area of portable electronic devices. Cellular phones, Laptop computers, and personal desktop assistants have all become ordinary items in people's lives. One of the primary customer complaints of these devices is the short battery life and/or the extra weight of the batteries due to the high power consumption in the circuitry. As CMOS technology scales and demand for great processing power increases, it can be shown that the power consumption of future of IC's will increase over time if important architectural changes are not made [1]. It is consequently critical in future circuits that power be minimized away from the traditional constraints of packaging cost and heat dissipation.

II. CMOS GATE DESIGN

In order to give a fair comparison of CMOS gates to standard implementations, a set of static MCML gates was also created. The MCML versions of each block were optimized for low power. Conventional sizing rules were used in which the pmos devices were made twice as wide as the nmos devices and all series transistors were made wider to realize the same first order delays. While logic styles such as dynamic logic or pass-transistor logic were generally not used, numerous of the blocks such as XOR, MUX, and adders were designed with transmission gates for enhanced performance and power efficiency. Since this paper does not deal with effects of long intersect, small load capacitances were used and hence all gates were minimum sized for low power [4].

Three dynamic latches and three flip-flops were analyzed for MCML sequential circuits: C^2MOS, TSPC, and Doubled C^2MOS. A more detailed report of these latches can be found in [3]. All of these dynamic blocks were compared to static MCML implementations and were found to be significantly superior in power and delay.

III. DESIGN PARAMETERS

We can view our test environment explain above as a computation engine which takes the user defined input parameters and the gate topology to be tested and create a number of performance metrics. The next step in the optimization process is to define and organize all of these input parameters to be optimized. The input parameters are show in Table 1:

Parameter Name	Description
V_{DD}	Supply Voltage
ΔV	Input and Output Voltage Swing
I	Current desired in current source
WA, LA	Width and Length of first level pull down network nmos devices
WB, LB	Width and Length of second level pull down network nmos devices (if needed)
WC, LC	Width and Length of third level pull down network nmos devices (if needed)
WRFP, LRFP	Width and Length of pmos load devices
WRFN, LRFN	Width and Length of nmos current source
LOADCAP	The output loading capacitance

Table 1: Input Parameter Description

Satisfy note that the WB, LB, WC, and LC parameters are only needed for two or three level gates. Too note that the total load capacitance (LOADCAP) is the sum of the input gate capacitance of the gate beneath test and some fixed interconnect capacitance. The basis for this type of loading is to avoid the optimization from unfairly using large strategy and creating a large loading on the preceding gate.

The subsequent sections are an attempt to show some of the property on the performance criteria by varying each of the design parameters. As avowed earlier, these effects are not independent of each other. This analysis is offered in order to give an intuitive feel for the design optimizations.

A. CMOS Optimization Procedure

Parameter Name	Limit
V_{DD}	$V_{DD} \leq 2.5V$

ΔV	200mV ≤ ΔV ≤ 2.4V
I	0.5uA ≤ I ≤ 100uA
LA, LB, LC	LA, LB, LC = 0.25um
WA, WB, WC	0.5um ≤ WA, WB, WC ≤ 1.5um
WRFP	WRFP = 0.5um
LRFP	0.25um ≤ LRFP ≤ 1.5um
WRFN	WRFN = 2.0um
LRFN	LRFN = 0.5um

Table 2: CMOS Optimization Procedure

for 0.5uA ≤ I ≤ 100uA
{
for 200mV ≤ ΔV ≤ 2.4V
{
Initialize V_{DD}= 2.5V
for 0.25um ≤ LRFP ≤ 2.5um
{
Find smallest WA,WB,WC which satisfy: 0.5um ≤ WA, WB, WC ≤ 1.5um Gain > 1.45,
Current Matching Ratio > 90%, Voltage Swing Ratio > 98%, Signal Slope Ratio < 5,
$|V_{DD}$ - RFP| voltage < 2.2V
If above is possible, find smallest V_{DD} which satisfies: Gain > 1.4,
Current Matching Ratio > 90%, Voltage Swing Ratio > 98%, Signal Slope Ratio < 5
If above is possible, store parameters and ED product.
}
Find LRFP which gives minimum ED for given I, ΔV
}
Find ΔV which gives minimum ED for given I Store values of I, ΔV, V_{DD}, WA, WB, WC, LRFP
}

IV. CMOS OPTIMIZATION RESULTS

It is useful to have a set of idealize data points as an upper bound on performance. This section will show the theoretical performance limits of individual CMOS gates and compare them with equivalent MCML gates.

The power-delay and energy-delay metrics for CMOS gates are directly comparative to the logic depth of the circuitry being used. It is therefore exceptionally unfair to compare CMOS and MCML gates at their absolute maximum clock frequency ($1/t_p$). as an alternative, we assume an optimistic yet possible logic depth of 4 for all gates in these section. The actual performance of the CMOS gates can be scaled accordingly from that depth in order to see the actual performance underneath real circuit conditions.

The final qualification before displaying the results is that this optimization does not take any layout effects into account. The load capacitance value uses an estimation of 1fF of wiring capacitance per fanout and a fanout factor of 4 (5for MCML) identical gates. The effects of actual circuit layout will be discussed in the next chapter. The first MCML gate optimized through the above procedure was a simple inverter/buffer. The result parameters are given in Table 3 for numerous different current levels, each optimized for energy-delay product. The plots of delay, energy, and energy-delay vs. current are shown in figure below 4. Note that each value of the current is fully optimized in all of the other parameters.

I (uA)	ΔV (mV)	V_{DD} (V)	$(W/L)_A$	$(W/L)_P$	$(W/L)_{RFN}$	tp (ps)	ED (pJ*ps)
0.5	300	0.80	0.5/.25	.5/1.5	2.0/.5	2134	7.22
1	300	0.75	0.5/.25	.5/1.0	2.0/.5	1075	3.40
3	300	0.80	0.5/.25	.5/.6	2.0/.5	391	1.43
6	350	0.85	0.5/.25	.5/.6	2.0/.5	247	1.21
10	400	0.90	0.5/.25	.5/.6	2.0/.5	182	1.15
30	400	1.10	0.75/.25	.5/.25	2.0/.5	98	1.21
60	500	1.25	0.95/.25	.6/.25	2.0/.5	68	1.30
100	600	1.35	1.20/.25	.8/.25	2.0/.4	57	1.57

Table 3: CMOS Inverter Optimization Results

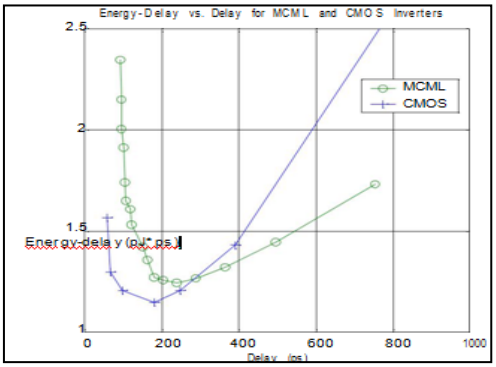

Fig. 1: MCML and CMOS Inverter Comparison

With these results, we can generate some comparisons with MCML inverters. The MCML inverter simulated has moms width = 0.5um and pmos width = 1.0um with a fanout of 5 indistinguishable inverters (plus interconnect capacitance). In order to compare the energy efficiency of CMOS and MCML gates, we plot the energy delay (ED) product against the delay of the gate. In CMOS gates, we vary the delay by changing the current level. MCML In gates, we vary the delay by changing V_{DD}. Once again, we assume a logic depth of 5 in order to allow a more fair comparison. The results are shown in below figure 1.

All of the gates show the same general trends as the inverter comparison and perform better in comparison for high performance, low depth circuits. We will not give the sizing results for all of the gates but it is illustrative to show the results for one of the larger gates, XOR3. These results for a limited set of current points are shown in table 4.

I (uA)	ΔV (mV)	V_{DD} (V)	$(W/L)_A$	$(W/L)_B$	$(W/L)_p$	$(W/L)_{RFP}$	$(W/L)_{RFN}$	tp (ps)	ED (pJ*ps)
1	250	0.75	.5/.25	.5/.25	.5/.25	.5/1.0	2.0/.5	2414	17.0
10	500	1.00	.5/.25	.5/.25	.5/.25	.5/.6	2.0/.5	532	10.5
100	800	1.70	1.40/.25	1.45/.25	1.50/.25	.6/.25	2.0/.4	201	25.6

Table 4: CMOS XOR3 Optimization Result

V. CMOS GATE LAYOUT

The second most important topic of layout methodology concerns the general cell design framework. There are two primary ways of doing layout for cell based of design: standard cell format and data path formation [3]. In standard cell designs, all cells usually have the same height but vary in width based upon the difficulty of the gate. The inputs and outputs are left balanced in a standard cell so that routing tools can send the signals in any direction. In data path designs, the width is typically fixed for all cells in order to make sure pitch matching but the height can vary. The inputs and outputs are united to opposite sides of the cell and bring to the edges to facilitate tiling. Both of these come near are shown in table 4.

One of the type differences between standard CMOS layout and MCML layout is the subject of transistor matching. It is known in MCML processing that many parameters of the transistor can vary both within a chip and between chips. These differences between transistors can degrade performance of differential of the circuits. There are three major places where transistor mismatch can unfavorably affect CMOS gate performance: input differential pair mismatch, pomes load mismatch, and VSC-gate mismatch. if first two forms of mismatch, input diff. pair and pmos load, are very similar in their range and effects. It can be shown [6] that these mismatch effects can be representation by an input offset voltage of the differential pair. For example, combination of the threshold voltage, gate oxide thickness, and transistor W/L mismatch may create a 60mV offset voltage for the input of a single gate. Therefore, if 300mV is applied to the input, the actual effective input voltage will be either 200mV or 350mV depending on the polarity. If 200mV is not enough for the gate to operate correctly, then the mismatch has successfully destroyed the circuit.

VI. LAYOUT RESULTS

The first comparison to be made is the difference in area and performance of the two styles of CMOS layout for basic cells. The two gates inspect were the inverter and XOR3. Both gates were layed out for three different current. The layout for the I = 10uA versions are shown in table 4. If we compare the implementations of the parallel and anti-parallel CMOS blocks, we observe that the parallel implementations are larger, as predictable. Figure 2 gives a synopsis of the type simulated results

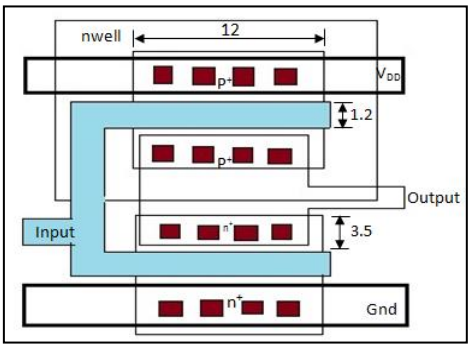

Fig. 2: CMOS inverter layout

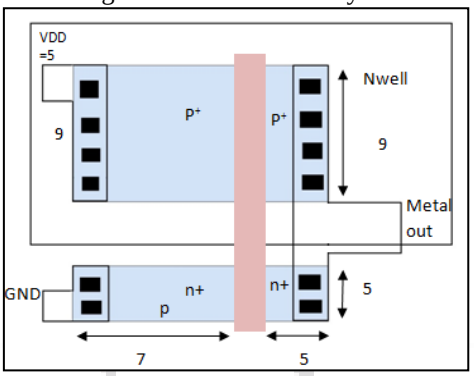

Fig. 3: Alternate layout approach

VII. CMOS LAYOUT VS. SCHEMATIC

Now that we have seen the tradeoffs associated with CMOS gate layout topologies, we would like to assess the performance degradation between simulations of schematics to simulations of layout. It is known that the layout simulations will create slower gates but the important measurement is to find out the relative slowdown in comparison with the slowdown of MCML circuits. With this knowledge, we can more accurately predict the benefits of CMOS over MCML when using schematic level simulation numbers.

Gate	V_{DD} (V)	Area (um^2)	Schematic Delay (ps)	Layout Delay (ps)	% change	Schematic ED (pJ*ps)	Layout ED (pJ*ps)	% change
INV	1.0	9.6	365	386	5.8	1.32	1.46	10.6
INV	1.5	9.6	162	169	5.0	1.34	1.46	9.0
INV	2.0	9.6	113	119	5.4	1.68	1.86	10.7
INV	2.5	9.6	93	98	5.4	2.25	2.45	8.9
XOR3	1.0	117	1995	2383	19.4	36.9	53.5	45.0
XOR3	1.5	117	827	975	17.9	36.8	52.0	41.3
XOR3	2.0	117	569	648	13.7	49.7	66.6	38.2
XOR3	2.5	117	455	528	16.5	66.9	92.5	38.3

Table 5: CMOS Schematic vs. Layout Performance

VIII. CMOS FULL DESIGN

In full design to see the overall effects of the optimizations and guidelines of the previous, we would like to design some more complex blocks of logic in CMOS. The first such example will be a case study of ripple adder of design. Please refer to [3] for a more comprehensive analysis of ripple adder architecture.

The building blocks of the ripple adder are the full adder block. The logic equation for a full adder is well known to be an XOR3 for the sum and a 4 input majority vote for the carry [3]. In nearly all MCML ripple adders, an optimization is made which pre-computes the propagate and generate

signals in order to speed up the carry path [3]. There is a similar possibility for CMOS adders and 2 implementations can be imagined. The two possibilities are shown in Figs. 8.1a and 8.2b below. The MCML adder used for comparison in this section uses transmission gates and is generally minimum sized and optimized for low power. Now that we have defined the two alternative adder structures in MCML, we would like to compare the two architectures against each other and against the equivalent MCML adder. For this experiment, we designed several different size ripple adders ranging from 4 bits to 64 bits and measured the delay and power consumption for both the CMOS and MCML implementations. The same experiment could be done at any presentation level but we limited the scope to a single current point near the optimal for CMOS at I = 10uA for all of the "gates" inside of the full adders. We use the same generalization techniques state to fix the voltage swing and V_{DD} across gates and we allow for the use of two VSC's for better swing control. The first comparison to be made is the relation performance of the two different full adder architectures for changeable ripple adder bit length. The key graphs of delay, power-delay, and energy-delay vs. bit length are shown in the figure 4.

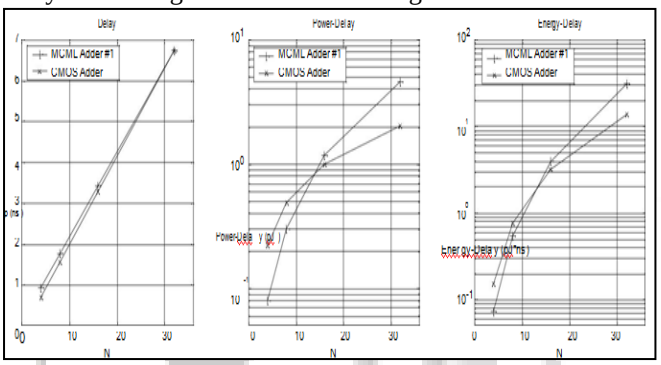

Fig. 4: (a,b,c) Comparison of MCML and CMOS Ripple Adders

IX. Optimization Results

Now that the algorithm, architecture, and circuits of the CORDIC system are defined, we will look at the simulation results. In order to verify the effects of wiring capacitance and other layout effects, the critical path pipeline stage was layed out for both the MCML and one of the CMOS CORDIC data points. We simulated the critical path delay for both the diagram and extracted versions from this single channel stage and extrapolate some of the results to the entire CORDIC. All of the predictable values are denoted with an asterisk but are believed to be very close to actual values. A subject for future work would be to absolute the layout of the entire CORDIC block for both the CMOS and 3 different MCML implementations. The simulated and predicted results are summarized in table 6.

Nominal V_{DD} (V)	2.5	2.0	1.5	1.0
Schematic W.C. Clock Freq. (MHz)	235	180	110	35
Extracted W.C. Clock Freq. (MHz)	140	106	66	20
Schematic Power (mW)	21.31	9.90	3.18	0.44
Extracted Power (mW)	21.5*	9.94*	3.33*	0.45*
Schematic ED (pJ*ns)	**312**	**248**	**213**	**249**
Extracted ED (pJ*ns)	**905**	**725**	**648**	**788**

Table 6: CMOS Results

In addition from delay and power, we would also like to consider the area and current switching properties of the two logic styles. Because only a single channel stage was layer out for both styles of the CORDIC. We cannot compare total areas but we can compare the area of this stages. We can also see at the simulated results of the power supply current and report the change due to switching activity. As the areas are all very similar between design points and the supply switching properties are more main for the high performance designs, we only report those results here. These results are summarized in table 9.2:

	CMOS	MCML
Area (um^2)	11,300	9,000
Nominal Supply Current (mA)	1.66	0
Maximum Supply Current (mA)	1.69	23
Minimum Supply Current (mA)	1.62	-5

Table 7: Area and Supply Current for CORDIC Pipeline Stage

X. Conclusions

This paper has been an in depth analysis of the benefits and pitfalls of using MOS Current Mode Logic. We have analyzed the transistor level behavior of CMOS circuits and compared their properties to those of standard MCML circuits., a design algorithm was proposed for CMOS gates and many of the design constraints were analyzed and explained. The algorithm was used to design better pieces of logic and several global design optimizations such as adaptive pipelining and current ratio adjustment were projected. We have seen that under ideal circuit conditions, CMOS can be much more energy efficient than equivalent MCML circuits and also present significantly less noise on the supply network.

XI. Future Work

While this paper attempted to analyze many different facets of the CMOS operation, there were several areas which still necessitate more research. The first goal of any future work would be to automate the design process for the CMOS gates using the algorithm. This automation would greatly reduce the time of implementing larger logic functions. Along the same lines, use of the CMOS gates should be incorporated into a standard digital logic design flow counting synthesis, placement, and routing. The main challenges in this arena would be the characterization of the CMOS gates for the synthesis tool and the implementation of differential routing.

The second major area of future work would be in the implementation of the control logic. While many of the effects of adaptive pipelining are predictable in this paper, it would be nice to actually implement the adaptive pipeline circuitry and measure its area, power consumption, and track properties. Also included in this future work would be the design of the VSCs and closer measurements of opamp requirements.

Finally, the design of different large circuit blocks would give a better representation as to the true effects of global routing and system issues. Further work is desirable to optimize the differential routing problem noticed in the CORDIC design. Other issues such as clock distribution and MCML interfacing need to also be addressed.

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