High Speed Vedic Multiplier used Vedic Mathematics

Dravik Kishorbhai Kahar[1] Harsh Mehta[2]
[1,2]Department of Electronics & Communication Engineering
[1,2]Parul University, Vadodara, Gujarat, India

Abstract— Multiplier is one of the most important part in any processor speed, which improves the speed of the operation like in special application processors like Digital Signal Processor (DSPs). Now I propose a method, which is faster multiplication technique by using Vedic mathematics formula Urdhava Tiryakbhyam method means vertically, and cross wise. Vedic mathematics is mainly based on sixteen Sutras and was rediscovered in early twentieth century. In ancient India, this Sutra was traditionally used for decimal number multiplications within less time. The same basic concept is applied for multiplication of binary numbers to make it useful in the digital hardware. The speed of the computation process is increased and the computing time is reduced due to decrease of path delay compared to the existing multipliers.

Key words: Vedic Mathematics, FPGA, MAC, Multiplier

I. INTRODUCTION

The general MAC architecture consists of multiplier, adder and an accumulator. The Multiply-Accumulate (MAC) unit is extensively used in microprocessors and digital signal processors for data-intensive applications, such as filtering, convolution, FFT transform and inner products. Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition determines the execution speed and performance of the entire computation. As the multiplier exhibits inherently long delay among the basic operational blocks in digital system, the multiplier determines the critical path. In order to improve the speed of the MAC unit, there are two major bottlenecks. The first is the partial products reduction network that is used in the multiplication block and the second is the accumulator. Both of these stages require addition of large operands that involve long paths for carry propagation. The main key to the proposed architecture is using the Vedic multiplier to design the MAC unit and compare the performance with the conventional MAC units Using Booth Multiplier, Wallace Multiplier in terms of area, speed and number of resources. The Vedic multiplier uses "Urdhva Tiryagbhyam" algorithm. The authors in use Vedic multiplier based on the ancient algorithms (sutras) for multiplication.

II. VEDIC MATHEMATICS PRINCIPLE

Vedic mathematics is the name given to the ancient system of mathematics, which was discovered between 1911 and 1918 by Sri Bharati Krishna Tirthaji. The word "Vedic" is derived from the word "Veda" which means the store house of all knowledge. The Vedic mathematics is based on 16 sutras which deal with various branches of mathematics. These sutras have been traditionally used for the multiplication of two numbers in the decimal number system. The possible multiplier architecture of Vedic mathematics to be implemented on DSP applications is Urdhva Tiryagbhyam. Traditional Indian mathematicians used this sutra to do multiplication of two decimal numbers in less time. It multiplies the number in the vertical and crosswise fashion. It is applicable to all cases of multiplication.

A. *Urdhva tiryagbhyam Sutra*

The main purpose of Vedic Mathematics is to be able to solve complex calculations by simple techniques. The formula being very short makes them practically simple in implementation. Urdhva-tiryagbhyam (Vertically and crosswise) sutra is general formula applicable to multiplication operation.

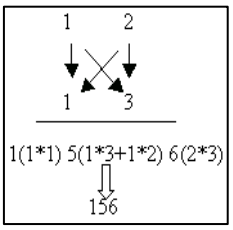

Fig. 1: Urdhya Triyagbhyam Methode

III. HARDWARE REALIZATION

A. *Hardware Realization*

The hardware realization of the two-bit number using the concept of the Urdhva-Tiryagbhyam sutra of the ancient Indian Vedic mathematics is shown in Fig 1.

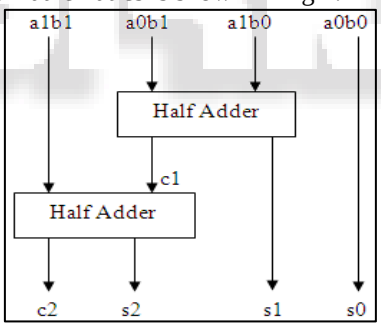

Fig. 2: Block Diagram of 2x2 bits Vedic multiplier [1]

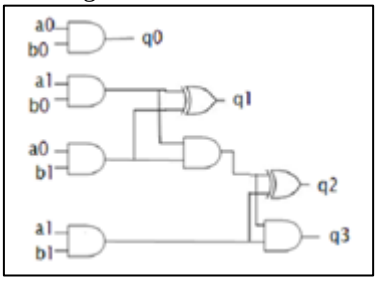

Fig. 3: Hardware Realization of 2*2 Hardware [2]

B. *8x8 Multiplier*

The 8x8 multiplier is made by using 4, 4x4 multiplier blocks. Here the multiplicands are of bit size (n=8) and the output is of bit size 16. The input is broken into small units of size n/2= 4. The newly formed units of 4 bits are given as the input of 4x4 multiplier block, where again these units are divided into even smaller units of size n/4=2 and fed to 2x2 multiply

block. The output obtained from output of 4x4 bit multiply block which is of 8 bits are sent for addition to an addition tree. The block diagram is shown in Fig 7. [2]

Let the two numbers

Let the two numbers A and B

A= a7 a6 a5 a4 a3 a2 a1 a0

B= b7 b6 b5 b4 b3 b2 b1 b0

The input is divided into small bits of four bits.

A1= a7 a6 a5 a4 A0=a3 a2 a1 a0 &

B1= b7 b6 b5 b4 B0= b3 b2 b1 b0

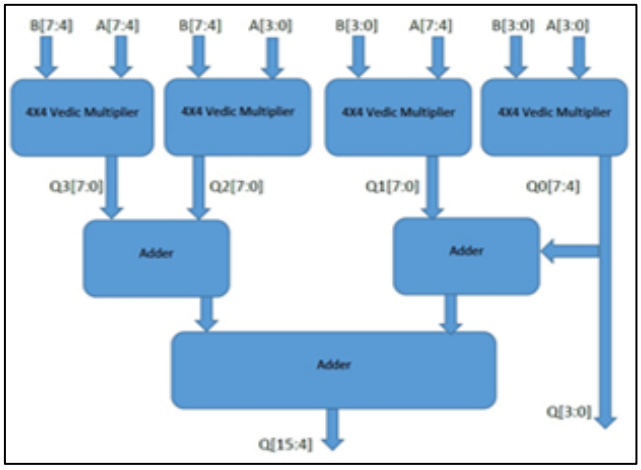

Fig. 4: 8*8 Multiply Block

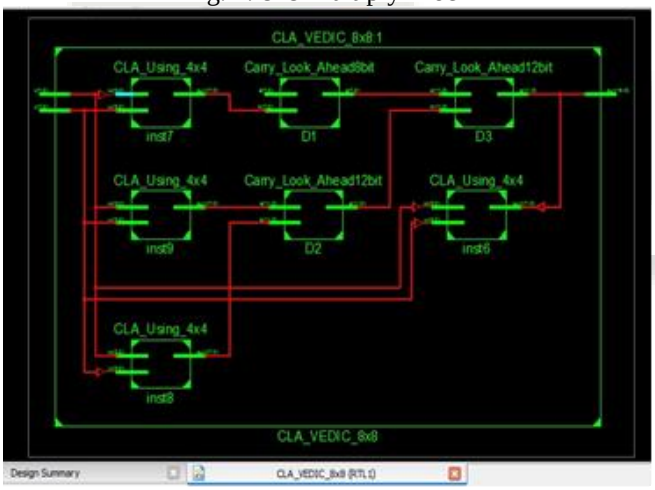

Fig. 5: RTL Veiw of 8x8 Vedic Multiplier

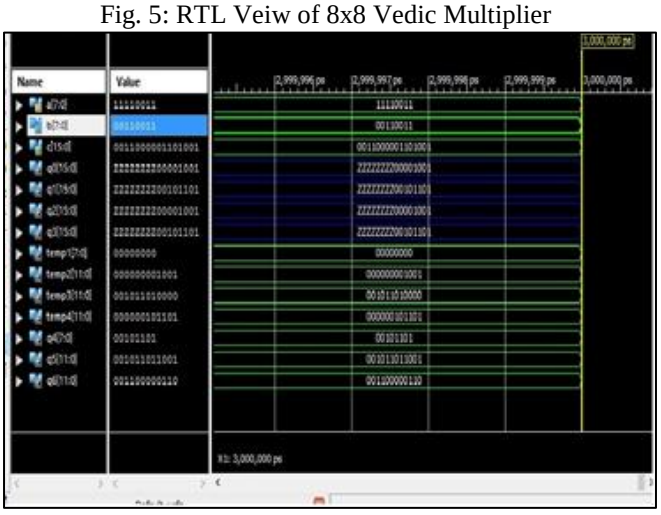

Fig. 6: Stimulation of 8x8 Vedic Multiplie

C. 32x32 Multiplier

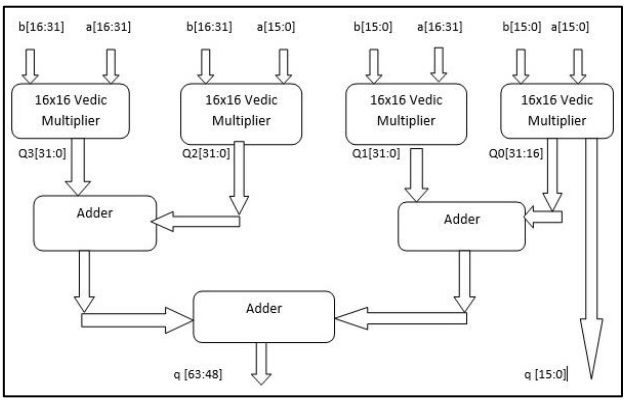

Fig. 7: 32*32 Multiply Block

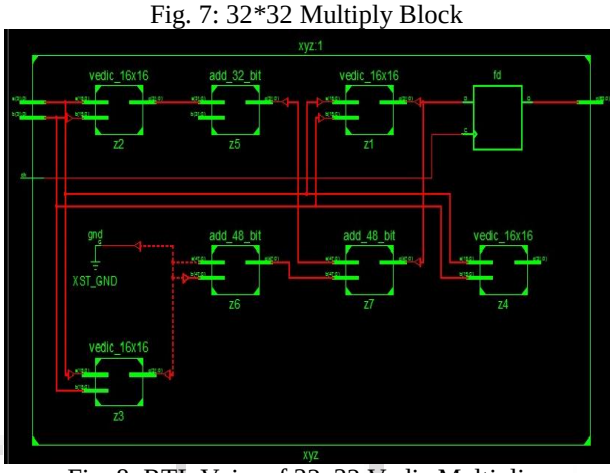

Fig. 8: RTL Veiw of 32x32 Vedic Multiplier

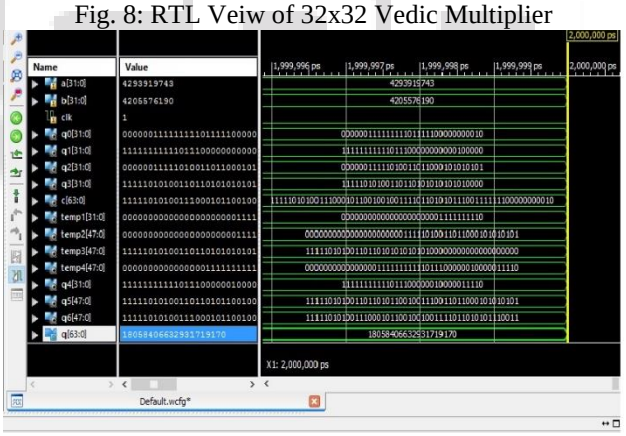

Fig. 9: Stimulation of 32x32 Vedic Multiplie

D. 64x64 Multiplier

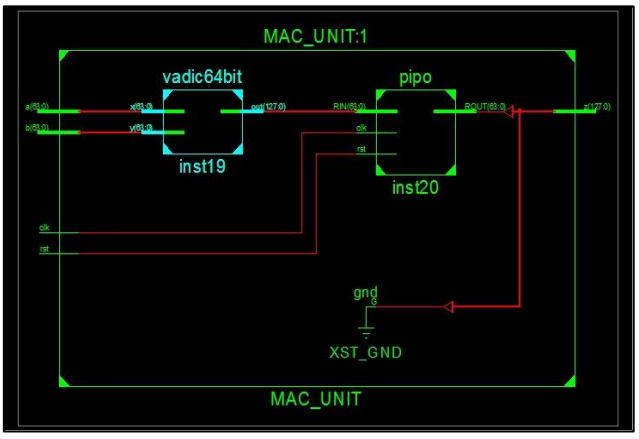

Fig. 10: RTL Veiw of 64x64 Vedic Multiplier

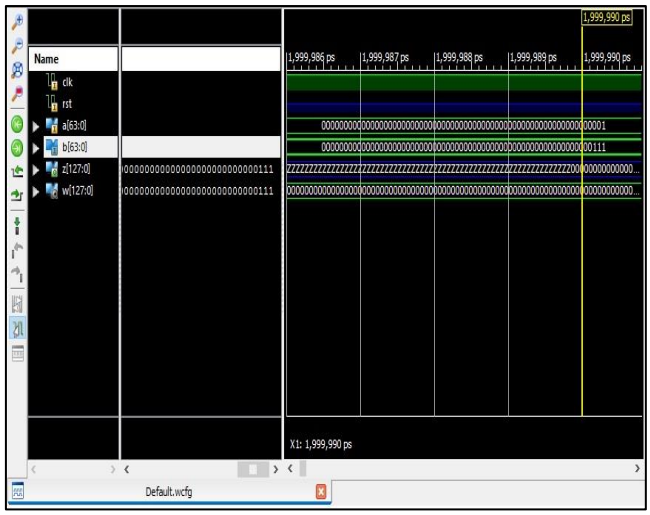

Fig. 11: Stimulation of 64x64 Vedic Multiplie

E. Advantages

- Vedic multiplier is faster than the other multipliers.
- The area needed for vedic multiplier is very small as compared to other multiplier architecture.
- MAC is used in modern digital signal processing.
- MAC always lie in the critical path that determines the speed of the overall hardware systems.
- It is use in binary and decimal number multiplication and also use unsigned and signed number multiplication.

F. Disadvantages

- For Complex Multiplications, Even the System Becomes Complex.

IV. COMPARISON & TABLE

Multiplier	Booth Wallace Multiplier	DevikaJaina, Kabiraj Sethi, Rutuparna Panda [1]	My Multiplier
4X4	13.77ns	17.45ns & 12ns[6]	11.477ns
8X8	25.756ns[1]	25.06ns	21.550ns
16X16	59.38ns[1]	36.09ns	28.086ns
32X32	-	-	30.956ns
64X64	-	-	44.377ns

Table 1: Comparison of Timing Delay

Multiplier	Number of Slice Utilized [4]	My Multiplier Number of Slice Utilized	Number of LUT [4]	My Multiplier Number of LUT
4X4	18	18	32	31
8X8	92	91	162	159
16X16	412	403	716	710
32X32	-	1639	-	2900
64X64	-	826	-	1440

Table 2: Comparison of Area

V. FUTURE WORK EXPANSION AND CONCLUSION

The design is based on Urdhva Tiryagbhyam Sutra is highly efficient algorithm for multiplication. Therefore, the design complexity is reduced for inputs of large number of bits and multiplication Speed is increased. The computation delay obtained for 64x64 Vedic multiplier is 44.377ns. The future enhancement of the Vedic multiplication is more reducing computation delay and increasing speed of Vedic multiplier.

REFERENCES

[1] Devika Jaina, Kabiraj Sethi & Rutuparna Panda "Vedic Mathematics Based Multiply Accumulate Unit" IEEE 2011
[2] Sreelekshmi M. S., Farsana F. J., Jithin Krishnan, Rajaram S, Aneesh R"Implementation of MAC by using Modified Vedic Multiplier"ISSN-2013
[3] P. Jagadeesh, Mr. S .Ravi and Dr. Kittur Harish. "Design of High Performance 64-bit MAC Unit" IEEE-2013
[4] Shamim Akhter "VHDL Implementation of Fast NxN Multiplier Based on Vedic Mathematic" IEEE-2007
[5] Vaijyanath Kunchigi, Linganagouda Kulkarni, Subhash Kulkarni, "32-bit MAC unit design using vedic multiplier" ISSN-2013.
[6] Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim, Yong Beom Cho "Multiplier design based on ancient Indian Vedic Mathematics" IEEE-2008

Books

[7] Vedic Ganit by Ashish Sipai.

