PPM adder design using XNOR-XOR Function

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Abstract— In this research work proposed a new 12 transistor PPM adder design using XNOR-XOR functions. A proposed PPM adder is reduced the transistor and while the better performance of the existing PPM adder. This better performance analysis of PPM adder is presented and significant reduction in power consumption, peak power and propagation delay. The entire PPM adder simulation result is obtained at TSMC 90nm CMOS technology.
Key words: PPM Adder, Power, Delay, PDP

I. INTRODUCTION

Recently, the conventional operations like addition, subtraction and multiplication, can produce the carry-propagation chains a building low- power VLSI system has emerged as highly in demand because of the fast growing technologies in digital communication and computation [1]. The battery technology does not advance in the microelectronics technology. There is a limited amount of power available for the mobile systems. So the designers are faced with some constraints: high speed, high throughput, small silicon area, low-power consumption and high-performance adder cells are of great interest.

The Redundant Binary number represents by three values {1, 0, -1}.The use of signed digit format allows each bit of the result to be obtained in parallel without carry propagation in arithmetic operations. Basically the PPM adder is depending on the Redundant Binary (RB) system. The PPM adder circuit is used as the building block in the RB system to handle the signed bit operations and improving its performance is critical for increasing the overall performance of Redundant Binary based digital signal processing system. There is a different design variety of PPM (Plus Plus Minus) adders in the literature, both at the transistor level and gate level [1] [2] [4]. The signed redundant binary digit number system is taken care of by the PPM adder and consequently, there is no need for an explicit mechanism to handle signed digit number.

The redundant binary number system is converted to binary number. This operation can perform easily from the following equation:

$$P(\sum_{i=0}^{n-1} p_i 2^i) = q^+(\sum_{xi=1} p_i 2^i) - r^-(\sum_{xi=-1} p_i 2^i) \quad (1)$$

Where $p_i \in (-1, 0, 1)$,

Each digit of p^+ and $p^- \in (0,1)$. This conversion can be used to carry look ahead adder circuit with a time propagation to *log n*.

II. PPM ADDER BASIC

PPM adder performs the operation $p^+ + q - p = 2t^+ - u^-$, whereas the redundant number $p = p^+ - p^-$, unsigned binary number q, resulting in another redundant number expressed by an interim sum and a transfer digit t^+. All the inputs are defined as $u^+, p^+, p^-, q \in \{0,1\}$ and the output bits are $t^+, u^- \in \{0,1\}$. In signed redundant binary system, there are three possible digits {1,0, -1} can be encoded using two bits shown in table 1.Hence, each signed digit is represented as $p = p^+ - p^-$, where $p^+, p^- \in \{0,1\}$ and $p \in \{-1, 0, 1\}$.

The addition operation performed by a PPM adder is: $p + q = 2t^+ - u^-$, where x is a redundant number expressed as $p = p^+ - p^-$ therefore $p^+ + q - p = 2t^+ - u^-$. Encoding of the digit p, where $p = p^+ - p^-$, using radix-2 redundant number system.

p	p^+	p^-	$P= p^+ p^-$
0	0	0	00
-1	0	1	01
1	1	0	10
0	1	1	11

Table 1:

Using the truth table, the interim sum u^- and the transfer digit t^+ can be expressed by the following expression:

$$u^- = \overline{p^+}\,p^-\,\overline{q} + \overline{p^+}\,\overline{p^-}\,q + p^+\,\overline{p^-}\,\overline{q} + p^+\,p^-\,q \quad (2)$$

$$t^+ = \overline{p^+}\,p^-\,q + p^+\,\overline{p^-}\,\overline{q} + p^+\,\overline{p^-}\,q + p^+\,p^-\,q \quad (3)$$

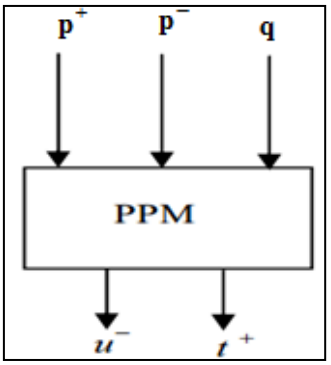

Fig. 1:

A.Guyot et al [7], 24 transistor PPM adder designed as shown in figure 2. It requires more numbers of CMOS transistors and manipulates the power dissipation and time delay. The main advantage of this design style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage and arbitrary transistor sizes with full output voltage swing.

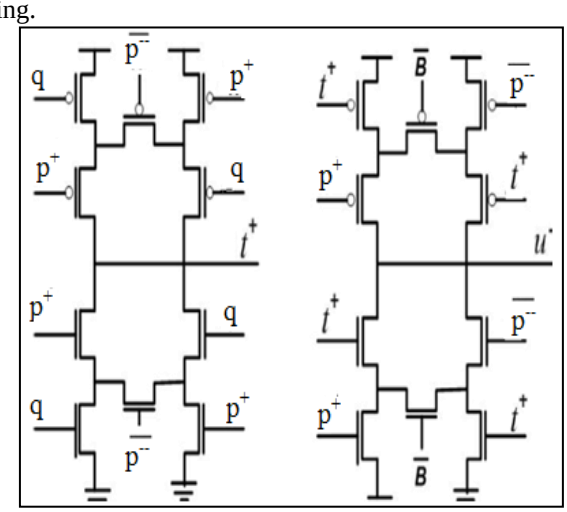

Fig. 2: 24T-PPM Adder[7]

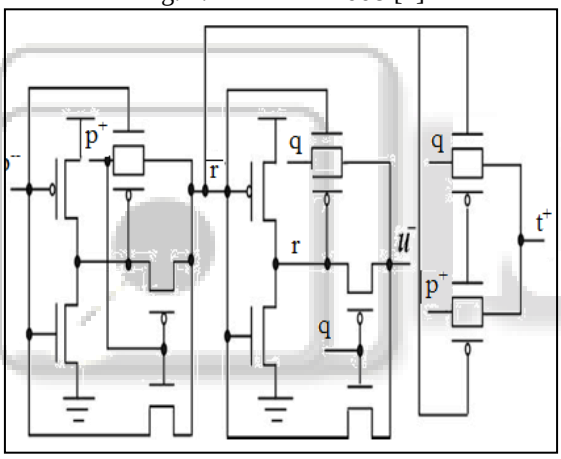

Fig. 3: 16T PPM Adder

Ramracksha Tripathi et al [8], to designed 14 transistor PPM adder with lower energy consumption and higher speed and provide, the better output voltage level for all combinations of input because of the availability of the two cross-coupled PMOS and NMOS transistors (feedback path) connected between XOR and XNOR outputs. The feed path eliminates the output threshold voltage loss, improve the noise immunity and enhance the driving capability of the circuit. This problem of skewed outputs the XOR and XNOR functions.

Rizwan Mudassir et al [9], to design two sets 14 transistor PPM adder different algorithm as shown in figure 5 & 6 and achieve the reduction in the time delay, power consumption, and chip area, compared to the different existing adder. Both circuits designed by the XOR-XNOR module. Author manipulate in this paper, the first PPM adder (set-1) has 36% less power consumption and 13% lower time delay compared to the 24-transistor PPM adder. The second PPM adder (set-2) has also 32% less power consumption and 34% lower time delay compared to 24-T PPM adder.

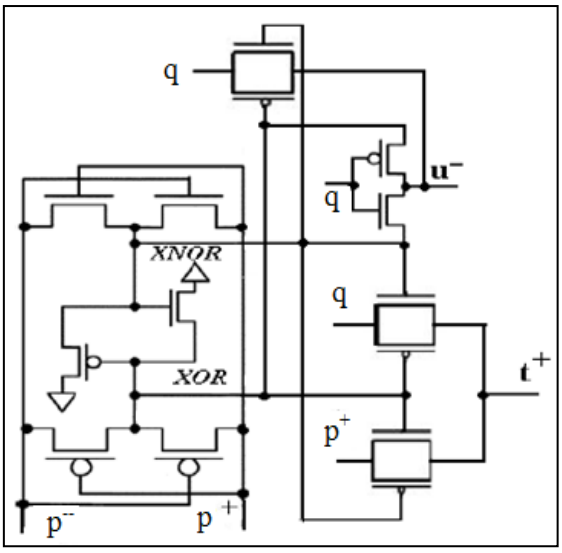

Fig. 4: 14 t PPM Adder [8]

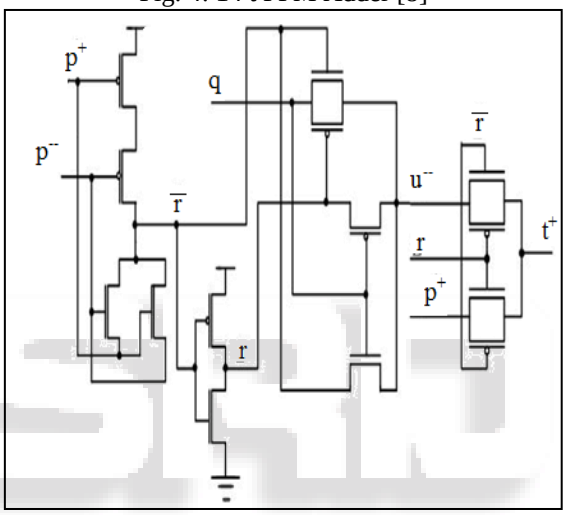

Fig. 5: 14t set 1 PPM Adder [9]

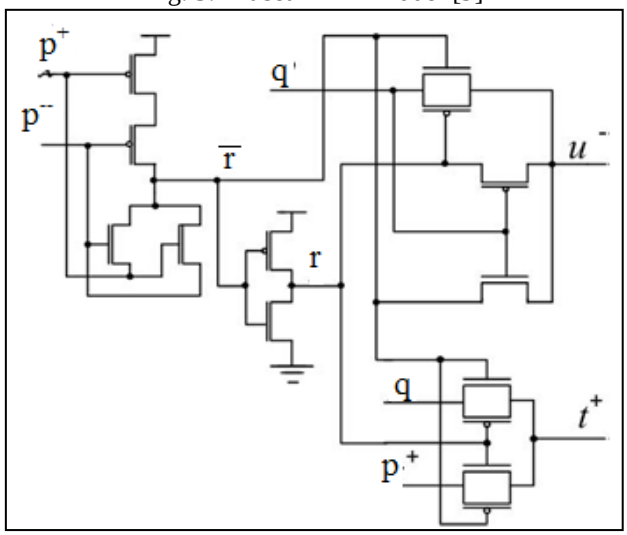

Fig. 6: 14t set 2 PPM Adder [9]

V.K Pandey et al [10], to design a 13 transistor PPM adder using mixed design style and has better performance compared to the existing PPM adder. Also, compared to the power consumption, delay, propagation delay product and faster existing PPM adder.

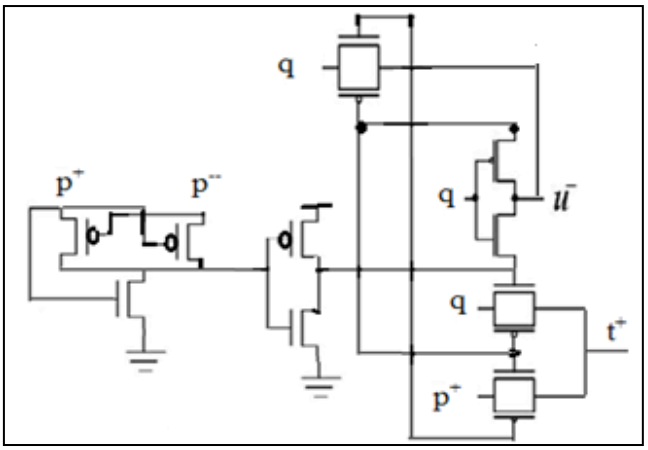

Fig. 7: 13t PPM Adder [10]

III. PROPOSED PPM ADDER

The proposed PPM adder designed by using 4 transistors XNOR-XOR circuit shown in below Figure.8. In this circuit, we are using 4 transistor XNOR-XOR circuits [11] consisting of 4 transistors. The proposed circuit consist of 12 transistors and has better performance compared to the existing PPM adder discussed in the paper. For XNOR circuit, the output signal from the case of 00, 01, and 11 will be complete. While in this case 10, NMOS will be on and pass the poor high signal level at the output end. They give the bad output logic levels, but manipulate the (W/L) ratios of PMOS and NMOS transistors to solve the problem until an acceptable logic level is restored.

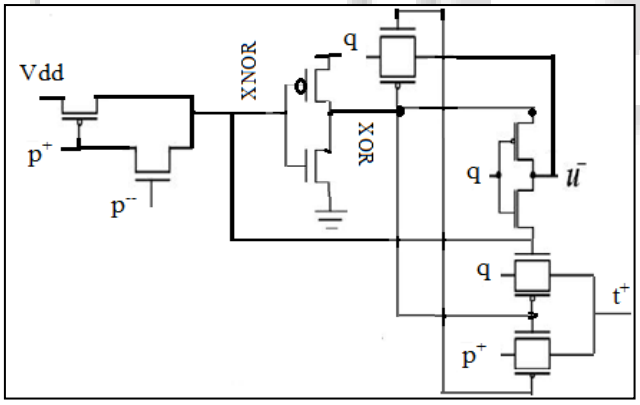

Fig. 8: 12t Proposed PPM Adder

IV. SIMULATION RESULTS AND COMPARISONS

Proposed 12T PPM adder circuit and all existing circuits are simulated in a hspice environment using TSMC 90nm at 1.8V. We need to apply the same input test pattern to all of the circuits. The input test pattern we have used consist of the three input signals, p+, p- and q and these signals are generating the square wave of equal ON and OFF times as shown in figure 9. A consist output load capacitance of 10fF is used for a power, peak power and propagation delay measurement. When changing the input reaches its 50% voltage level to the time when the resulting output reaches its 50% voltage level for both rise and fall output transitions is measured delay.

The comparative performance of various PPM adder circuits at 1 V and 1.8V supply voltage is given in Table I & II.

PPM Adder	Delay t+ (psec.)	Delay u− (psec.)	Average power (µsec)	Peak Power (µsec)
24t	6162	8.41	58.81	606.78
16t	31.70	29.07	229.81	662.66
14t (set1)	33.31	22.59	0.99	9.5
14t (set2)	3.3	5.5	0.66	5.5
14t	12.50	6.36	0.66	7.69
13t	17.56	5.93	0.57	4.1
12t (Proposed)	8.8	8.2	0.53	5.3

Table 2: Comparative Performance Of Various PPM Adders at 1.8 V

PPM Adder	Delay t- (psec.)	Delay u− (psec.)	Average power (µW)	Peak Power (µW)
24t	6241.9	256.88	11.40	89.75
16t	51.78	47.98	23.75	76.71
14t(set1)	79.51	53.46	0.65	8.2
14t(set2)	40.67	38.93	0.53	10.24
14t	56.18	53.57	0.56	9.3
13t	72.88	70.49	0.62	7.7
12t(Proposed)	74.83	22.23	0.46	3.2

Table 3: Comparative Performance Of Various PPM Adders at 1 V

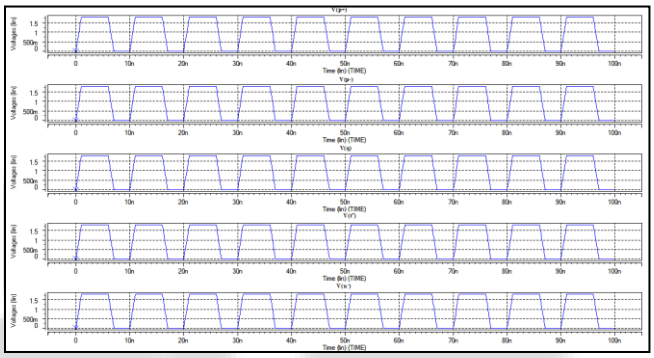

Fig. 9: Waveform of proposed 12T PPM adder

V. CONCLUSION

An all including performance, analysis and simulation PPM (Plus Plus Minus) adder have been presented for Redundant Binary (RB) number systems. The proposed PPM adder designs 12 transistors are derived from different algorithm based XNOR-XOR function. All the simulation results proposed and existing PPM adder has been implemented using 90nm CMOS technology. Show that the simulation results of proposed PPM adder and existing adder have in terms of the power consumption, peak power and Delay at 1V and 1.8V using HSPICE.

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