Design of Reconfigurable Multichannel MRI Receiver on FPGA

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Abstract— A design presented for a Multichannel digital Receiver system for MRI that overcomes the concerns associated with solution regarding cost, scalability. Commercial receivers used for parallel MR imaging often-present researchers with hurdles such as high cost per channel, low scalability for multiple coils and non-accessibility to intermediate data for research. MR signal from up to 16 coils are band passed sampled at RF, with all subsequent down conversion performed on single chip Field Programmable Gate Array (FPGA). The Resulted device is in order of magnitude cheaper and much more scalable

Key words: FPGA, MRI Receiver, ADC, Under sampling, Digital down Converter, Ethernet

I. INTRODUCTION

Magnetic resonance imaging (MRI) systems provide highly detailed images of tissue in the body. The systems detect and process the signals generated when hydrogen atoms, which are abundant in tissue, are placed in a strong magnetic field and excited by a resonant magnetic excitation pulse.

Hydrogen atoms have an inherent magnetic moment because of their nuclear spin. When placed in a strong magnetic field, the magnetic moments of these hydrogen nuclei tend to align. Simplistically, one can think of the hydrogen nuclei in a static magnetic field as a string under tension. The nuclei have a resonant or "Larmor" frequency determined by their localized magnetic field strength, just as a string has a resonant frequency determined by the tension on it. For hydrogen nuclei in a typical 1.5T MRI field, the resonant frequency is approximately 64MHz

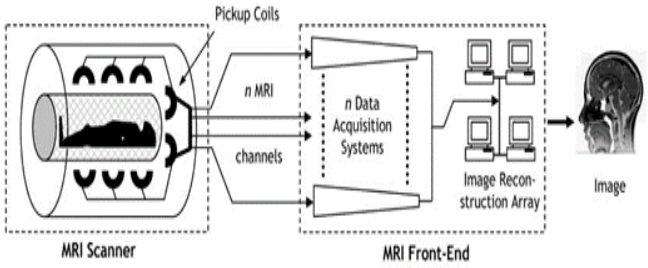

Fig. 1: Conventional MRI Receiver

Conventional MRI imaging of fast motion such as a beating heart used to be difficult because of the long scan times necessary. The current solution is to use parallel imaging, i.e. techniques such as SENSE and SMASH. These employ multiple coils with reduced phase encoding steps to compensate for the artifacts caused by shorter scan times. Each coil is a channel that requires its own receiver; multiple receivers may integrated into one physical device.

Conventional receivers generally use analog demodulation before baseband digital sampling. This system leads to various imperfections including channel-to-channel mismatch, quadrature phase imbalance and dc offsets manifest as degrading artifacts in the final image and available commercial receivers have eight channels at most. Apart from non-scalability, the high cost per channel as well as the lack of access to intermediate data in proprietary receivers.

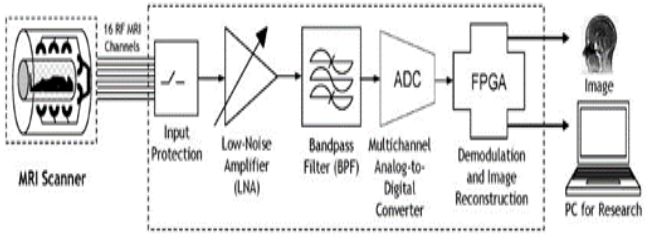

Fig. 2: Multichannel Digital Receiver

Digital receiver we have presented is a low cost scalable 16-channel receiver that band pass-samples RF MR Signal and down converts then on a single FPGA. This system is inexpensive, highly scalable and allows complete access to intermediate data. The system compensate for hardware inaccuracies after digitalization. Received MR Signals are band pass sampled directly, without any analog demodulation. A single field programmable gate array (FPGA) then down coverts and reconstructed them. The system could handle 8-16 channels, scaling modularly beyond that, integration of multiple channels will minimize hardware redundancies. It is easy to access image as well as intermediate data, which is difficult to get in commercial environment needed for research purpose.

II. DESIGN AND IMPLEMENTATION

The Fpga platform is Zedboard with zynq-7000 all programmable Soc XC7Z020-CLG484-1 which combines two ARM Cortex A9 cores and Xilinx programmable logic in a single device. The onboard XC7Z020 Soc contains 85k logic cells ~1.3 million ASIC gates, 53200 look up tables (LUT), 106,400 flip-flops. The board consist of XADC Dual 12-bit 1MSPS Analog to Digital Converter.

The basic digital receiver consist of mainly three stages a) Analog to Digital Conversion b) Digital downconverter c) Data transfer

A. Analog to Digital Conversion:

An Analog Signal must be sampled at rate fS greater than twice its maximum frequency fH to eliminate distortion in the resultant data. For 64 MHz MRI signal, fS > 128 MHz

The fS > 2fH rate is based on assumption that the signal to be sampled has frequency components from DC all the way to fH. For a non-baseband signal whose spectrum does not extend down to DC, the sampling rate is determined by the bandwidth of the signal. For MRI, the information is contained in a narrow 250 KHz band around 64 MHz [4], therefore a sampling rate of 500 KHz is adequate.

The input signal must be band pass filtered to remove any noise and spurious content outside the information bandwidth (63.875 – 64.125 MHz), otherwise these would also fold back into base band and corrupt the

information and the analogy input bandwidth of the ADC used must be higher than the actual frequency (64 MHz) of the Signal. [3]

The on board XADC is used which have the necessary 12-bit resolution and analog input bandwidth (300 MHz). Sampled data are output serially to save on I/O pins; they are converted to parallel data for input to the next stage by a high-speed de-serializer inside the FPGA.

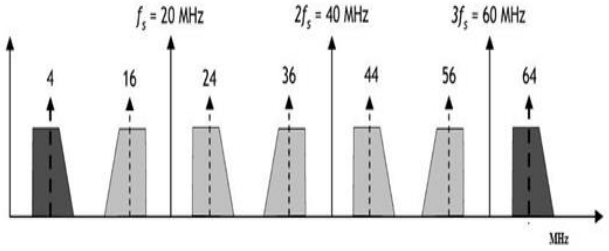

Fig. 3: under sampling MRI Signal

B. Digital down Converter:

The system consists of bandpass filters with multiple bandwidth to have different resolution while forming final image. It is implemented on the FPGA board specifying multiple bands by reloading coefficients.

The bandpass sampled data is demodulated and filtered by digital down converters implemented on Xilinx Zynq-7000 FPGA.

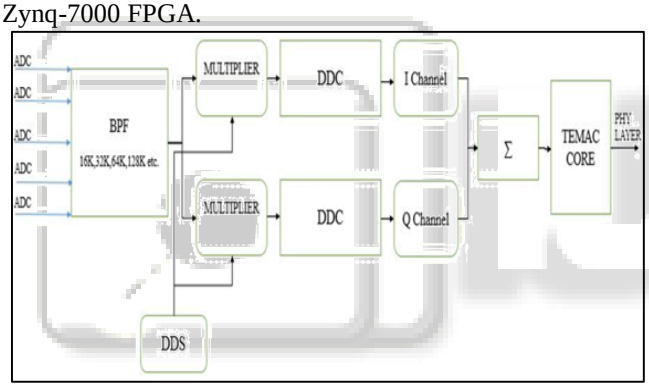

Fig. 4: Digital down Conversion

Fig (4) shows digital down conversion process. A direct digital synthesizer generates 16 bit, 4 MHz I/Q Los that are multiplied with the sampled 20 MSPS data stream. FIR Compiler IP is used to decimate by a decimation factor of 20. Fir Compilers are low pass filters so that reduce noise and simultaneously decimate. Fir filter compensate for the ~ 1dB pass band attenuation. [3] FIR Coefficients can be configured by the user for custom low pass filters. All processing within the DDC is done at 24 to 32 bits fixed-point precision with final output rounded to 16 bits. Thus, the design can easily use high resolution ADCs.

C. Data Transfer:

DDR RAM Controller design of Xilinx core was adapted and down converted baseband, data is buffered to a standard PC RAM module. The Memory serves as program memory for two-power PC microprocessor embedded on FPGA. This information is downloaded to a PC for Analysis. Networking is provided by a fast Ethernet designed with the help of Temac Core.

I.

Fig. 5: Data Transfer

III. Result and Analysis

A Single Channel receiver with different bandwidth for proper image reconstruction is designed; the receiver is tested for single channel. Entire system is simulated and working properly with each sample at output of LPF is generated at rate of 0.45 µsec.

Resource Utilization

Slice LUT	Slice Register	MUX	DSPs
8600	13000	3	190

Table 1:

The 16 Channel receiver implemented on the FPGA takes up to 70 % of the total logic cells and uses only PowerPC. The prototype has less cost per channel, which is cheaper than commercial receivers are.

IV. Conclusion

A Multichannel Reconfigurable digital receiver system for MRI has been presented. On board ADC, Variable band pass sampling at RF, Digital down Converter and data transfer on a single FPGA Provides a System that is cheaper than Available receivers are. The provided system is scalable in future [2] as per blocks required and allows easy access to intermediate data from any stage over the network.

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