High Gain Single-Stage Rail-to-Rail Amplifier with Nested-Current-Mirror

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Abstract— A power efficient, high DC gain, gain-bandwidth product (GBW) and slew rate (SR) rail-to-rail output single-stage amplifiers are replacement of their multi-stage amplifier, especially for LCD display applications that are used in large numbers in their column drivers as a buffer. This paper represents Positive Feedback Nested-Current-Mirror Single-Stage Rail-to-Rail Amplifier to achieve high of DC gain, Specifically, NCM is customizable for different mirror steps, and sub mirror ratios, to balance the performance metrics and capacitive- load (CL) at the output of column driver to get high driving capability under rail-to-rail output swing. Analytical treatments of the Positive feedback NCM technique in terms of performance limits and robustness reveal that the NCM amplifier can surpass the fundamental power-efficiency limit set by the basic differential-pair (DP) amplifier. A prototypes 3-step Positive feedback NCM amplifiers were analyzed with 88 dB DC gain and 0.0028–0.27 MHz GBW over 0.15–15 nF with 86 approx phase margin (PM) with power consumption power 144µW for the load of .15nF.

Key words: Area Efficiency, CMOS, Current Mirror, DC Gain, Differential-Pair (DP) Amplifier, Frequency Compensation, Gain-Bandwidth Product (GBW), Low Temperature Polysilicon LCD, Multi-Stage Amplifier, Nested Current Mirror, Rail-To-Rail Output Swing, Single-Stage Amplifier, Slew Rate (SR), Stability

I. INTRODUCTION

For display applications like wide-measurement low-temperature polysilicon (LTPS) LCD boards that include thousands of buffer amplifiers in their column drivers, the zone and power spending plans of every cradle amplifier are amazingly tight to meet the market weight on cost and show quality [1]. Furthermore, because of the manufacture spread and scale option of the boards, the cushion amplifiers ought to ace an extensive variety of capacitive load (CL) up to several nF, while securing sufficiently substantial DC pick up (e.g., dB for 10 bit determination [2]) and yield swing. Right now, multi-organize amplifiers command those applications inferable from their key favourable circumstances of high DC pick up and rail-to-rail yield swing. Be that as it may, the requirement for recurrence pay expands their outline many-sided quality, which additionally confines their drivability of (range and size), zone and power efficiencies [3].

Single-stage amplifiers using itself for recurrence pay can be an alluring answer for streamline the territory and power. They can be genuinely steady at any, normally broadening the drivability. Specifically, the present reflect amplifier [Fig. 1(a)] demonstrates this forthcoming by safeguarding a rail-to-rail yield swing, and the present reflect calculate offers a flexibility to influence the different execution measurements, for example, powerful transconductance , yield resistance, pick up transmission capacity (GBW) item and slew rate (SR). However, the characteristic DC pick up is generally low, just practically identical to that of the differential-match (DP) amplifier [Fig. 1(b)]. This reality confirms that most established single-stage amplifiers were underused expansive applications when contrasted and their multi-arrange partners. Truth be told, under a similar power spending plan regardless of how huge is , the present reflect amplifier is as yet lingering behind the DP amplifier for most execution measurements (Table I). Accordingly, the DP amplifier is when all is said in done picked as the "brilliant reference" for benchmarking distinctive amplifier topologies [4].

Table I additionally incorporates the two-organize amplifier with basic Miller remuneration (SMC) [Fig. 1(c)]. We see that aside from the DC pick up and yield swing, the DP amplifier normally performs superior to the SMC amplifier for most measurements at equivalent power, paying little respect to estimate. This paper presents a settled current-reflect (NCM) single stage amplifier [5] that can ease the tight execution trade-offs in routine single-stage amplifier topologies, including the essential DP amplifier. The prototyped 3-stage and 4-stage NCM amplifiers accomplish good exhibitions regarding the standard DP amplifier, and are practically identical with the state-of the-craft of three-phase amplifiers. The created NCM standard and circuit usage are not quite the same as those as of late produced for low-dropout (LDO) controller [6] and vast amplifier [7], even they likewise mean to enhance the DC pick up, GBW and SR through efficiently utilizing the little pick up stages.

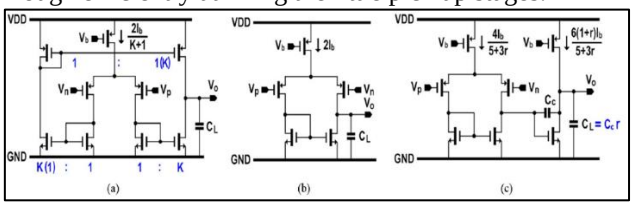

Fig. 1: Conventional (a) current-mirror amplifier (b) Differential pair amplifier (c) Simple Miller compensation amplifier (SMC) [3]

	Current-Mirror Amplifier	Differential-Pair (DP) Amplifier	SMC Amplifier*
$G_{m,eff}$	$\frac{K}{K+1}g_{mp}$	g_{mp}	$\frac{2}{5+3r}g_{mp}$
R_o	$\frac{K+1}{K}(r_{on}\|\|r_{op})$	$r_{on}\|\|r_{op}$	$\frac{5+3r}{6(1+r)}r_{on}\|\|r_{op}$
GBW	$\frac{K}{K+1}\frac{g_{mp}}{C_L}$	$\frac{g_{mp}}{C_L}$	$\frac{2r}{5+3r}\frac{g_{mp}}{C_L}$
DC Gain	$g_{mp}(r_{on}\|\|r_{op})$	$g_{mp}(r_{on}\|\|r_{op})$	$[g_{mp}(r_{on}\|\|r_{op})]^2$
Slew Rate	$\frac{K}{K+1}\frac{2I_b}{C_L}$	$\frac{2I_b}{C_L}$	$\frac{2r}{5+3r}\frac{2I_b}{C_L}$
Noise	$\frac{8k_BT\gamma}{g_{mp}}\frac{(K+1)^2}{K}\left(1+\frac{g_{mn}}{g_{mp}}\right)$	$\frac{8k_BT\gamma}{g_{mp}}\left(1+\frac{g_{mn}}{g_{mp}}\right)$	$\frac{5+3r}{2}\frac{8k_BT\gamma}{g_{mp}}\left(1+\frac{g_{mn}}{g_{mp}}\right)$
Phase Margin	< 90° depends on K	~90°	~70°

Transconductance & output resistance of NMOS [g_{mn}, r_{on}] and PMOS [g_{mp}, r_{op}];
*For the SMC amplifier, the pole associated with the output is placed at 3x GBW to achieve ~70° PM.

Table IPerformance Comparison between (a) current-mirror amplifier (b) Differential pair amplifier (c) Simple Miller compensation amplifier (SMC)

II. BENEFIT AND PERFORMANCE LIMITS OF EXISTING SINGLE-STAGE AMPLIFIERS

This section evaluates the benefit and performance limits of the state-of-the-art single-stage amplifiers [8]–[10] that are variants of the rail-to-rail output current-mirror topology [Fig. 1(a)]. Their capability of enhancing the DC gain, GBW and SR are explored that stimulates the proposed solution.
In the refrence [1] for method are proposed to enhance the gain of single stage are as:

1) Current-Mirror Amplifier With Shunt Current Sources
2) Current-Mirror Amplifier With Current Reuse
3) Current-Mirror Amplifier With Local Positive Feedback
4) Multi-Step NCM Single-Stage Amplifier

III. BASIC PRINCIPAL OF NCM AMPLIFIER

The description of the NCM technique consists of two steps (Fig. 2). The first step is to split the DP transistor of the current-mirror amplifier into N sub-transistors M1 to Mn , and alternately connect their inputs with Vn and Vp . Next, the of M to are Mn combined in sequence via the NCM formed by subdividing a current mirror into pieces with different ratios, which concurrently increases the effective transconductance $G_{m\ NCM}$ and output resistance R_{oNCM} beyond those of the DP, and other single-stage amplifiers [8]–[10]. Specifically, by sharing the current Ib1 (for the left-half side) with N divided DP transistors [(I1,M1) (I2,M2)……(IN,MN) ,their outputs are combined via nested current mirrors with ratios [(1:K1), (1:K2),….. (1:KN),.. Their inputs are alternately routed with Vn and Vp to ensure their outputs are in-phase summed. Since M1-MN are located in the signal path, all their transconductance contribute to $G_{m\ NCM}$,and are customizable via choosing K1 to KN properly. For instance, for Signal Path 1gm1(M1), is multiplied by times, contributing (K1.K2.K3…..KN) gm1 to $G_{m\ NCM}$. If high DC gain and GBW are desired, more mirror stages and bigger of their ratios are preferred. Yet, to reduce the noise and random offset voltage, the largest amount of current should be allocated to the 1st mirror with a small. To enhance SR, most of the current can be assigned to the 2nd-last mirror with augmented KN-1and KN. Indeed, the mirror stages and ratios are limited by the PM and transistor mismatches. If a large CL is imposed, PM is no longer the stability constraint. For the mismatches, the W and L of transistors can be upsized for better matching and higher intrinsic gain. Both are decisive to the expected value of $G_{m\ NCM}$, and R_{oNCM}. For very low-power design (e.g., nW regime), the leakage current might be a factor that limits the number of mirror stages. This is because at the highest temperature and fast corners the intrinsic gain of the transistors is significantly reduced. Along such a NCM process, $R_{O\ NCM}$ is improved as well since less current is directed to the output stage. Thus, the DC gain can be as high as that of single-stage Cascode amplifier, but without the output swing penalty. Moreover, unlike the typical current-mirror amplifier, cutting the current of the output stage does not essentially degrade the SR. In fact, as long as KN.IN>Ib, the SR of the proposed NCM amplifier can still outperform that of the DP amplifier. The number of NCM step is a design parameter. We show below the 3-step and 4-step designs as they can provide appreciable performance gain, while allowing the design metrics to be analytically tractable and usable. A NCM step ≥ 5will raise the design complexity dramatically as there will be many parameters to manage. In addition, the benefit of SR boost will diminish.

IV. THREE-STEP NCM SINGLE-STAGE AMPLIFIER

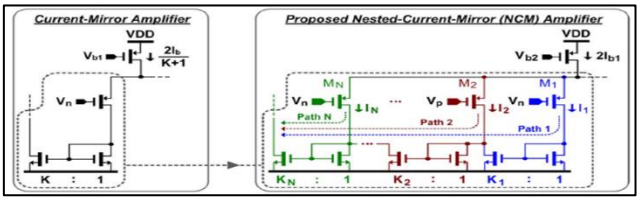

Fig. 2: Development of the NCM amplifier from the current-mirror amplifier

Fig. 3 shows the schematic of a 3-step NCM amplifier, with the sizing details marked on the right half. The DP transistors are split intoM1 –M3 Their outputs are summed via the NCM mirrors realized by M4–M9 .M10 collects the output of the left, to form the single-ended output together with .To show how the mirror ratios to contribute to the effective transconductance, GBW, DC gain, SR, and noise, quantitative analyses are conducted, and they are valid for both

Single-ended output and differential output implementations.

1) Is first calculated by finding the small-signal
2) Short current at the output with respect to the input

V. QUANTITATIVE ANALYSIS OF PROPOSED OPERATIONAL AMPLIFIER "THREE STAGE NESTED CURRENT- MIRROR"

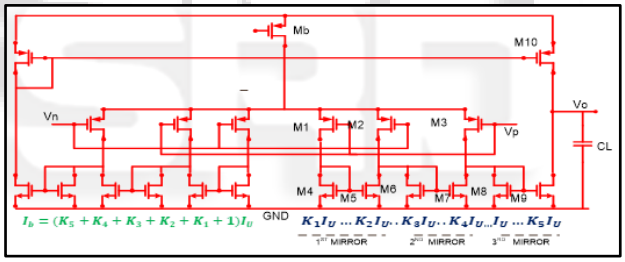

Fig. 3: Three stage NCM amplifier from the current –mirror amplifier

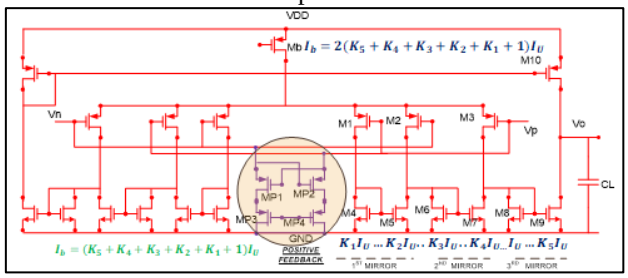

Fig. 4: Three stage Positive feedback NCM amplifier from the current –mirror amplifier

Fig. 3 shows the schematic of a 3-step NCM amplifier and Fig. 4 shows the schematic of a 3-step positive feedback NCM amplifier, with the sizing details marked on the right half. The DP transistors are split into M_1- M_3 Their outputs are summed via the NCM mirrors realized by M_4- M_9 . M_{10}collects the output of the left, to form the single-ended output together with M_9 .To show how the mirror ratios K_1 to K_5 contribute to the effective transconductance ($G_{m,NCM3}$),

GBW, DC gain, SR, and noise, quantitative analyses are conducted, and they are valid for both single-ended output and differential output implementations.

$G_{m,NCM3}$ Is first calculated by finding the small-signal short current at the output with respect to the input, which is given by

$$G_{m,NCM3} = \frac{K_5\left[2K_4\left(\frac{K_3+K_2}{K_3}\right)+1\right]}{\sum_{i=1}^{5} K_i + 1}\, g_{mp"}$$

$$g_{mp"} \approx \frac{g_{mP}}{\left(\frac{1}{R_0} - G_m\right)},\ R_0 = \frac{\sum_{i=1}^{5} K_i + 1}{K_5}\left(r_{on}||r_{op}\right)$$

$$G_m \approx \frac{r_{MP1} g_{MP1}}{r_{MP1} + \frac{1}{g_{MP3}} + (g_{MP1} + g_{MPb1}).\, r_{MP1}\frac{1}{g_{MP3}}}$$

As indicated in above eq., $G_{m,NCM3}$ is mainly determined by the product of K_5 and $K_4(K_3+K_2)/K_3$ with a given sum of K_1 to K_5 . Since the product is readily sized to be much higher than the sum $G_{m,NCM3}$, is significantly boosted, usually in one or two order(s) of magnitude higher than that of the DP amplifier (i.e., g_{mp}) for the same power consumption. This also indicates that the 3-step NCM amplifier has the same GBW improvement over the DP amplifier.

The DC gain of the 3-step NCM amplifier is expressed as the product of $G_{m,NCM3}$ and its output resistance$R_{O,NCM3}$. In addition to $G_{m,NCM3}$ that already considerably improves its DC gain, $R_{O,NCM3}$ is also enhanced over that of the DP amplifier, and can be represented by

$$R_{O,NCM3} = \frac{\sum_{i=1}^{5} K_i + 1}{K_5}\left(r_{on}||r_{op}\right)$$

The gain enhancement seen in is attributed to substantial bias current reduction in the output stage in comparison with that of the DP amplifier. Thus, an overall DC gain enhancement of > 30 dB over the DP amplifier can be observed, while should be better than those (10 to 20 dB) of other topologies.

SR determines the amplifier's settling performance. The SR of the 3-step NCM amplifier SR_{NCM3} can be analyzed according to Fig. 4. Suppose a large negative step appears at, it follows that the 2nd mirror turns off. Consequently, almost all the current in M_3 is directed into M_8 and amplified by the 3rd mirror to discharge C_L . As long as the amplified current is $> 2I_b$, the negative SR can be better than the DP amplifier. Similar analyses can be applied when there is a large positive input step occurring at V_p, resulting in a symmetric SR expressed by

$$SR_{NCM3} = \frac{K_5(K_4+1)}{\sum_{i=1}^{5} K_i + 1}\frac{2I_b}{C_L}$$

Examining (15) implies that if $K_5(K_4+1) > K_5 + K_4 + K_3 + K_2 + K_1 + 1$, the SR of the proposed amplifier surpasses that of the DP amplifier at equal power, which can be realized by selecting relatively large K_5 and K_4.

Noise can be a limiting factor in certain applications. Since the analysis of both thermal and flicker noise follows the same procedure outlined in [13], only the input-referred thermal noise of the 3-step NCM amplifier is provided here, which is given by

$$\overline{V_{n,NCM3}^2} \approx \frac{(\sum_{i=1}^{5} K_i + 1)\left[\left(\frac{K_4K_2}{K_3K_1}\right)^2 K_1 + \left(\frac{K_4}{K_3}\right)^2 (K_3+K_2) + K_4 + 1\right]}{\left[2\left(\frac{K_4}{K_3}K_2 + K_4\right)+1\right]^2 . \frac{8k_BT\gamma}{g_{mp"}}\left(1+\frac{g_{mn"}}{g_{mp"}}\right)}$$

Compared to that of the DP amplifier, it is unobvious from above eq. that the NCM amplifier generates more noise. But intuitively when $G_{m,NCM3}$ is enhanced by the NCM, the transistors' noise is also amplified by the mirror ratios. Thus, the NCM amplifier has to tradeoff the noise performance for a better $G_{m,NCM3}$.

The main sources of random mismatch in a pair of identically designed MOS transistors are from the threshold voltage (ΔV_{th}) and the current factor ($\Delta\beta$) where $\beta=\mu C_{OX} W/L$ [14].Assume that A_{thn} and A_{thp} are threshold mismatch factors of NMOS and PMOS, respectively, while $A_{\beta n}$ and $A_{\beta p}$ correspond to the current mismatch factors of NMOS and PMOS. The input-referred offset voltage of the 3-step NCM amplifier can be obtained by calculating the total drain-current standard deviation (σ) at the output and then referred to the inputs of the DP transistors by dividing $G_{m,NCM3}$, which is given below,

$$\sigma_{NCM3}(V_{OS}) \approx \frac{\sqrt{\left[\left(\frac{K_4}{K_3}\right)^2\left(K_3+K_2+\frac{K_2^2}{K_1}\right)+K_4+1\right]\left[\frac{A_{thp}^2}{W_{up}L_{up}}+\left(\frac{I_u}{g_{mpu}}\right)^2\frac{A_{\beta p}^2}{W_{up}L_{up}}\right]+\left[\left(\frac{K_4}{K_3}\right)^2\frac{K_2(K_2+K_1)}{K_1}+\frac{K_4(K_4+K_3)}{K_3}+1\right]\left[\left(\frac{g_{mun}}{g_{mpu}}\right)^2\frac{A_{thn}^2}{W_{up}L_{up}}+\left(\frac{I_u}{g_{mpu}}\right)^2\frac{A_{\beta n}^2}{W_{up}L_{up}}\right]}}{2\left(\frac{K_4}{K_3}K_2+K_4\right)+1}$$

Since the mirror ratios are the key sizing parameters of NCM, using multiple unit-transistors in parallel is helpful for accurate matching (this often translates into the finger design in the layout). Thus, the unit-transistors with the device area $W_{un}.L_{un}$(NMOS) and $W_{up}.L_{up}$ (PMOS) are utilized in above eq. Also, g_{mnu} (g_{mpu}) denotes the transconductance of the unit-NMOS (PMOS) transistor biased with the unit-current. Generally, the offset contribution due to the current factor mismatches can be neglected as it is much smaller than that from the threshold voltage mismatches with a typical g_m/I_D designed for the input transistors. To further simplify above eq., and obtain quantitative assessment of the offset voltage tradeoff, we assume both unit-NMOS and PMOS transistors generate the same transconductance (i.e. $g_{mnu} = g_{mpu}$) and contribute the same amount of offset voltage. For instance, if the mirror factors are selected as the design case to be given below (i.e. $K_1 = 2, K_2 = K_4 = 3$, $K_3 = 1$ and $K_5 = 5$), the 3-step NCM amplifier has to tradeoff 1.8 increment of the offset voltage when compared with that of the DP amplifier.

VI. Simulation Results

A. Schematic of Proposed NCM Amplifier Which Is Simulated Using In 180nm CMOS Technology in LT-Spice. Using BISM IV Model of CMOS.

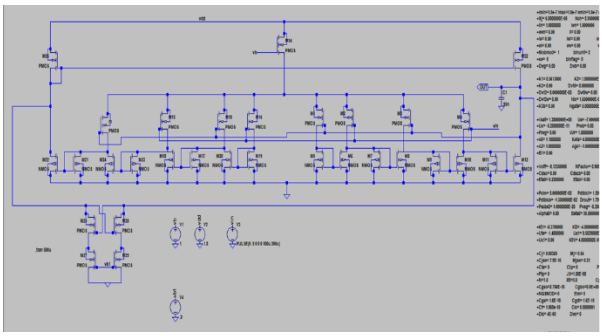

Fig. 5: Schematic of Proposed Positive Feedback NMC Amplifier

B. Transient Response of the Positive Feedback NMC Amplifier with Square Wave of Time Period 200us with Load Capacitance 15nf.

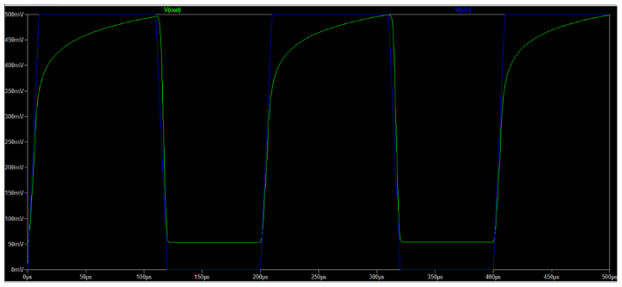

Fig. 6: Transient Response of the Positive Feedback NMC Amplifier

C. Transient Response of the Positive Feedback NMC Amplifier with Square Wave of Time Period 200us With Variable Load Capacitance Range From .15nf to 5nf With Step Size .5nf

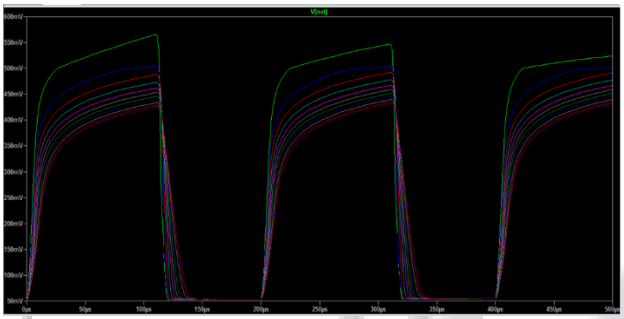

Fig. 7: Transient Response of the Positive with Parametric Load of Capacitance Range from .15 to 5n Feedback NMC Amplifier

D. Static Power Loss of Positive Feedback NMC Amplifier with Variable Load Capacitance Range From .15nf to 5nf With Step Size .5nf

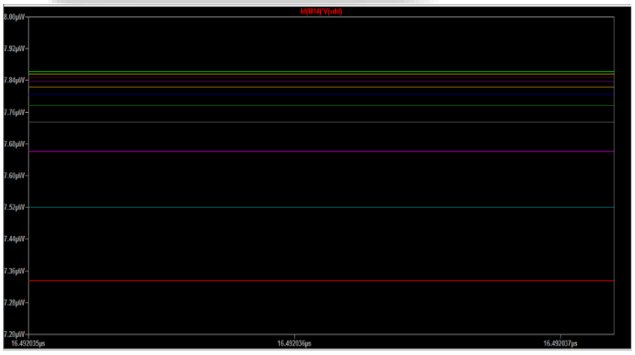

Fig. 8: Static Power Loss of Positive Feedback NMC Amplifier

E. Dynamic Power Loss at Output of Positive Feedback NMC Amplifier with Variable Load Capacitance Range From .15nf To 5nf With Step Size .5nf With Square Wave Of Time Period 200us.

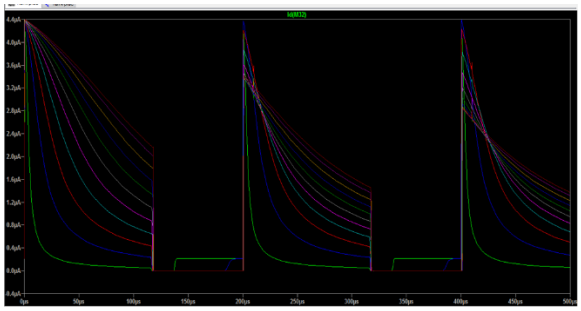

Fig. 9: Dynamic Power Loss at Output of Positive Feedback NMC Amplifier

F. AC Response of the Positive Feedback NMC Amplifier Load Capacitance Of .15nf

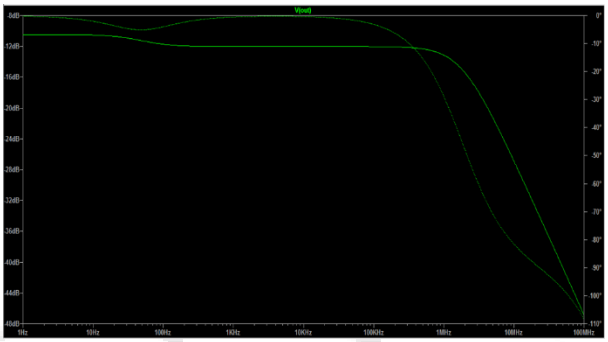

Fig. 10: AC Response of the Positive Feedback NMC Amplifier

G. AC Response of the Positive Feedback NMC Amplifier with Square Wave of Time Period 200us With Variable Load Capacitance Range From .15nf to 5nf With Step Size .5nf

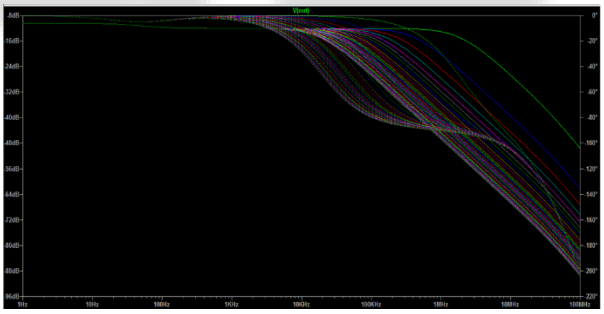

Fig. 11: AC Response of the Positive Feedback NMC Amplifier with Variable Capacitive Load

H. Noise Response of the Positive Feedback NMC Amplifier with Load Capacitance Of .15nf.

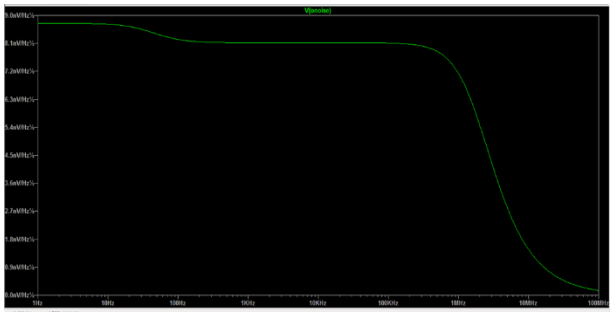

Fig. 12: Noise Response of the Positive Feedback NMC Amplifier

I. Noise Response of the Positive Feedback NMC Amplifier with Variable Load Capacitance Range From .15nf to 5nf With Step Size .5Nf

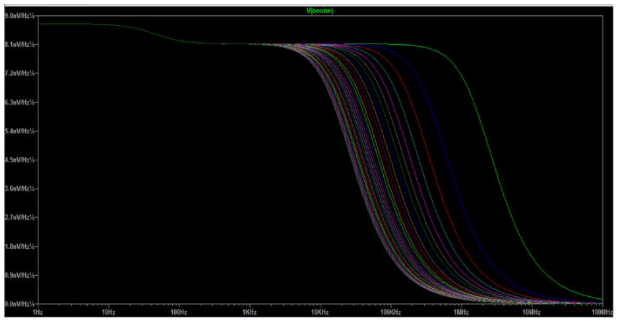

Fig. 13: Noise Response of the Positive Feedback NMC Amplifier with Variable Load Capacitance

VII. RESULT

Circuit characteristics	Ref [38]	Ref [39]	Ref [1] Base paper	Propose work
supply voltage	2V	.9V	1.2V	1.8V
Total current	111µA	NA	NA	6µA
Power dissipation	288 µW	5.7µW	15.24µW	144µW
DC gain (open loop)	>100db	>100db	72db	>88db
Phase margin	84/1nF	53/.5nF	87/.15nF	85/.15nF
Gain margin(db)	9.8/1nF	NA	31.5/15nF	26/.15nF
Unity gain frequency	1.37 MHZ/1nF	1.34 MHZ	.29 MHZ	.47 MHZ
Noise (µv/hz)	172/10kHz	NA	1470/ 0.1kHzµV/hz	3.6µv/hz
Slew rate	.59(V/µs)/1 nF	.62(V/µs)/. 5nF	.025(V/µs)/.1 5nF	.36(V/µs)/.15 nF

Table 1: Comparison Table

VIII. CONCLUSIONS

This paper introduced a NCM single-stage amplifier that has more design flexibilities (mirror steps and sub mirror ratios) to optimize the performance metrics (GBW, DC gain and SR), while preserving a rail-to-rail output swing, and wide Load capcitancedrivability without entailing any compensation capacitor or resistor. Both the performance limits and robustness of the NCM technique have been analytically explored, and the fabricated DP, 3-step amplifiers confirmed the theoretical study and performance claims.

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