Review on Different Types of Binary Code Converters

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Abstract— In digital electronic, analog to digital converter is most important fundamental in wide variety of digital system. Adiabatic logic brings about a great deal of power minimization in digital circuits. The digital circuits and digital signals provide greater advantages when compared to analog circuits in processing efficient transmitting and speed. This research paper presents the analog to digital converter (ADC) for low power applications, so selection of suitable architecture is extremely difficult.

Key words: Analog to Digital Converter, Power Minimization

I. INTRODUCTION

Adiabatic Logic is the term given to electronic circuits with low-power consumption that implement reversible logic. The term adiabatic is obtained from the aspect that an adiabatic process is one in which the total energy or heat in the system remains constant. Research in this area has mainly been fueled by the fact that as circuits gets faster and smaller, a problem of a huge increment in their energy dissipation that an adiabatic circuit promises to solves. Analog to digital converters are one of the most important elements in processing of signal and communication system. It is a mixed system which converts the analog signals into the digital signals for transformation of sensor data. There are several types of ADC's available such as, delta sigma ADC, successive approximation ADC, and pipeline ADC etc. Whenever analog signal is needed back, digital to analog converter is required. Analog to digital converters are important block in many recent systems that require the combination of analog signals with digital systems. In various mixed-signal systems, Analog-to-Digital Converters (ADC) are necessary for interfacing of analog signals to digital circuits.

II. LITERATURE REVIEW

A number of research papers of various journals and conference were studied and survey of existing literature in the proposed area is reported below:

Michat Szermer et al.(2003) proposed "Modeling and Simulation Sigma-Delta Analog to Digital Converters using VHDL-AMS"- The aim of this research paper is to introduce the technique of modeling and simulation of the sigma-delta modulators using VHDLAMS. A few ligma-delta modulators structures are presented. From 1" to 41h order sigma delta modulator and also a triple cascade structures are shown. The optimal solution is submitted to use as a part of silicon micro system. The analog to digital conversion is performed using sigma-delta method. Modulators are modeled and tested with application of VHDLAMS simulator. The sigma-delta converters presented in this paper had been fully described in VHDL-AMS language. Results of the simulations were presented on this paper. On the basis of obtained results the best solution will be chosen to implement in silicon micro system. The main target of this work was to simplify design process of the integrated circuits.

P.Iyappan et al. (2009) proposed "Design of Analog to Digital Converter Using CMOS Logic" –The signals in the real are all analog in nature. The digital circuits and digital signals provide greater advantages when compared to analog circuits in processing efficient transmitting and speed. The System on Chip (SoC) forces the integration of analog circuits with digital circuits. A new type of encoder (fat tree encoder) has been developed for advanced TIQ flash ADCs. The TIQ flash ADC offers higher data conversion rates while maintaining comparable power consumption level so that it is also highly suitable for the complete SoC integration using the standard digital CMOS process. The simulation test results showed that the fat tree encoder outperformed the commonly used ROM type encoder in terms of speed.

Ashwini V. Kale et al. (2012) proposed "Comparative analysis of 6 bit Thermometer-to-Binary Decoders for Flash Analog-to-Digital Converter- This research paper describes different topologies of decoder suitable for Flash ADCs. A comparative analysis among them is presented in terms of power consumption, hardware required, & propagation delay. Implementation of different thermometer to binary decoders show that MUX based decoder is more efficient in terms of power consumption. Fat tree decoder requires less propagation delay but its layout design is more complex & time consuming. Wallace tree decoder requires more power but there is no need of extra BEC circuit. MUX based decoder has less hardware & lower critical path compared with others. Hence MUX based decoder is a compact & fast decoder for Flash ADC implementation. However integrating bubble error detection & correction circuit for MUX based decoder will be more promising for future designs.

Wei-Hsin Tseng and Pao-Cheng Chiu (2014) proposed "A 960MS/s DAC with 80dB SFDR in 20nm CMOS for Multi-Mode Baseband Wireless Transmitter"- this DAC is fabricated in a 20nm CMOS process and operates from a single 1.8V supply.The measured DNL/INL comparison between calibrated and non-calibrated results. After calibration, DNL is improved from -1.1/+0.7 to -0.2/+0.2LSB and INL is improved from -2.1/+0.3 to -0.3/+0.2LSB. The calibrated INL drift over temperature is smaller than +/-0.3LSB, using the calibration values derived at 40oC.The measured SFDR after calibration is 80.2dB for a 235 kHz tone. The calibration improves SFDR by 18dB. The two channel 10-bit I/Q DACs occupy only 0.01mm2 which is 12.5% of the area for an uncalibrated I/Q DACs. The calibration technique presented here is extremely effective in reducing DAC area. The total current consumption is 5mA and 9mW from 1.8V power domain.

Anshul Pathak and Shyam Akashe (2014) proposed "An effective 3-bit Flash Analog to Digital Converter using 45-nm Technology"- This research paper using 45-nm technology, a 0.7-V, 3-bit CMOS flash analog to digital converter is presented. In this paper a design and simulation of 3-bit flash ADC have been presented by using 45-nm technology. Simulation shows that with no digital calibration performance the proposed 3-bit flash ADC achieves ENOB of 0.689 at consuming low power. This work conventional flash ADC and proposed Flash ADC is compared in table 1. The proposed flash ADC substantially reduced the power and leakage at different supply voltage. Active power of flash ADC is 218.9-µW and leakage current is 68.47-pA at 0.7-V power supply and input voltage is 0.5-V at 5-MHz and SNR of 2.39-dB. This structural design is able to extensive medium-to-high resolution appliances because it is easiness for circuit.

Shruti Konwar (2014) proposed "power efficient code converters using adiabatic logic"-Adiabatic logic brings about a great deal of power minimization in digital circuits. An application of the same is presented here by proposing a new design of some code converters-BCD to Excess-3, Binary to Gray and Gray to Binary, using the Adiabatic Array Logic. The main aim behind the whole work was to design and propose new low power digital circuits for the common code converters- BCD to excess-3, binary to gray and gray to binary employing the adiabatic logic. A close look into the total power dissipation reveals that the proposed circuits dissipate only about a quarter amount of power in comparison to the conventional CMOS in each of the converters Thus, the cumulative power saving when used in large scale will be very high. So, the proposed circuits are a promising candidate for ultra-low energy computing and telecommunication domain where they find widespread applications.

Hao Huang et al. (2014) proposed "An 8-bit 100-GS/s distributed DAC in 28-nm CMOS", This paper presents an 8-bit 100-GS/s digital-to-analog converter (DAC) using a distributed output topology in 28-nm low-power CMOS. This design achieves a -3dB bandwidth which is greater than 10 GHz. With 1-kbyte on-chip memory the DAC can convert 1k symbols cyclically, which is sufficient for characterizing the DAC performance. The DAC consumes 2.5 W from a 1.1V/1.5V/2V power supply. The area of the test chip is 1.5mm². It suppresses the frequency image introduced by the 50 GS/s sub-DACs and thus increases the usable frequency band utilization. Therefore it is best suited for frequency domain modulation schemes like OFDM.

Nikhil A. Bobade et al. (2014) proposed "A Review: Design of Successive Approximation Analog to Digital Converter"- This research paper presents the analog to digital converter (ADC) for low power applications, so selection of suitable architecture is extrmely difficult. Day by day number of applications is built on the basis of efficient power consumption with moderate sampling rate. This SAR ADC will be utilized for high speed with low power consumption and medium resolution. A SAR ADC is suitable for medium bit resolution with higher sampling rate from kS/s to MS/s. In future, SAR ADC using minimum capacitor technique will be energy efficient and cost-effective. Proposed work will achieve efficient successive approximation analog to digital converter having medium bit resolution of the data convertor with efficient power consumption and moderate sampling rate.

M. S. Yenuchenko (2016) proposed "Thermometric Decoders for High Resolution Digital-to-Analog Converters"- Digital-to-analog converters with High-resolution frequently use segmented architecture. The design process for high resolutions is becoming a challenge due to complexity of decoder. In this research paper, common design techniques for a thermometric decoder have been discussed in details. Generalizing of a 2-D structure is proposed. These techniques can simplify a design process of a thermometric decoder for high-resolution DACs. The rule for getting logical functions of thermometric decoder outputs is presented. It helps to design a thermometric decoder by individual forming of output logical functions. Formulas for a transistor number and estimation for delay time are given. The results of the simulation confirm the ratio of characteristics for decoders and the tendency that a more complex design technique provides a decoder with a smaller transistor number and delay time.

Vishal Moyal and Dr. Neeta Tripathi (2016) proposed Implementation of Stacked-CMOS Inverter based TIQ Comparator for FADC. this research paper proposes a Threshold Inverter Quantizer (TIQ) for implementation of a 3-bit, 1.2V Flash Analog to Digital Converter (FADC). A Stacked-CMOS Inverter which is based on Threshold Inverter Quantizer is utilized for implementing Comparator section in the Flash ADC; the comparator is operating on different reference voltages, which is obtained by systematic adjustment of aspect ratio of each stacked CMOS TIQ comparator. In this research work, flash type ADC is designed as well as simulated using stacked-CMOS inverter based Threshold Inverter Quantizer. The key goal of this research work is to minimize the power dissipation requirement in an ADC. This proposed design provides the total power dissipation of ADC simulated at Vdd of 1.2V and a capacitive load of 1fF for an input frequency ranges from 1 Hz to 1 MHz is observed as 5.98µW.

T. Durga Prasad et al. (2016) proposed "Design and Implementation of Energy Efficient Code Converters" - One of the major concerns of power dissipation in CMOS circuits is charging and discharging of capacitor. The power dissipation can be reduced by restoring this energy back to the source instead of discharging. An observation shows that if we charge the capacitor slowly the energy requirements are lesser as compared to the faster charging method. Adiabatic circuits use this methods viz. slow charging and discharging of capacitor, and recycling of charge to minimize the power consumption. Simulation is done using mentor graphics tool with TSMC 180nm technology for the designing of circuits. In this research paper Gray to Binary, Binary to Excess-1 and Binary to Gray code converters are designed using adiabatic logic techniques at 180nm technology. The PFAL logic gives more efficiency than ECRL logic at both low and high frequencies.

III. CONCLUSION

In this paper, we presented a review on different code converters necessary in digital logic design. The PFAL logic gives more efficiency than ECRL logic at both low and high frequencies. Fat tree decoder requires less propagation delay but its layout design is more complex & time consuming. Wallace tree decoder requires more power but there is no need of extra BEC circuit. MUX based decoder has less hardware & lower critical path compared with others. Hence MUX based decoder is a compact & fast decoder for Flash ADC implementation. However integrating bubble error detection & correction circuit for MUX based decoder will be more promising for future designs.

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