Faster Approach to Image Processing using Vedic Mathematics

RanjanaKumari[1] Monali Chinchamalatpure [2]
[1]PG Student [2]Assistant Professor
[1,2]Department of Electronics & Telecommunication Engineering
[1,2]DPCOE Pune, India

Abstract— This review paper Faster Approach to Image Processing using Vedic Mathematics. Multipliers are fundamental and area intensive component in the architecture of any DSP system. In many areas, there are situations where the complexity and delay of the whole circuit increases because of inefficient multipliers. So it is necessary to reduce such complexity of Multipliers for efficient DSP architecture with high throughput and time consuming. The algorithm is implemented using verilog HDL and is tested and verified with MATLAB also. The multiplier can be substituted for conventional multipliers in various applications. The exploration of Vedic algorithms in Digital Signal Processing prove to be extremely advantageous. Hence it can be applied for discrete cosine transform application.

Key words: DCT, MATLAB, Vedic Mathematics, FPGA, Xilinx

I. INTRODUCTION

The rapid progress of VLSI technologies, many processors based on audio and image signal processing have been developed recently. The basic requirement of these processors is faster addition and multiplication capabilities which aid them in image and digital signal and thus are of extreme importance to the field. So there is always need for new algorithms and efficient hardware to implement them. This can be achieved or made possible by using the proposed Vedic Mathematics [1][2] [3]method which enhances the multiplication capabilities.

Vedic Mathematics is the name given to the ancient system of Indian Mathematics. Vedic mathematics was rediscovered from the ancient Indian scriptures between 1911 and 1918 by Sri Bharati Krisna Tirthaji (1884- 1960), a scholar of Sanskrit, mathematics, history and philosophy. He studied these ancient texts for years and, after careful investigation, was able to reconstruct a series of mathematical formulae called Sutras. Bharati Krishna Tirthaji, who was also the former Shankaracharya of Puri, India, delved into the ancient Vedic texts and establishing the techniques of this system in his pioneering work, Vedic Mathematics (1965), which is considered the starting point for all work on Vedic Mathematics Computational unit is key unit of many high performance systems such as microprocessor, DSP processor various Filters. Multiplier units of a digital image or signal processing system [4][5][6][7][8] are deciding factors for its performance as increasing the time taken for processing and overcoming other constraint are major areas of concerns in these systems[11].

The Sanskrit word 'Veda' means 'knowledge'. The Vedas consist of a huge number of documents there are said to be thousands of such documents in India, many of which have not yet been translated, which are shown to be highly structured, both within themselves and in relation to each other. Some documents, called 'Ganita sutras', were devoted to mathematical knowledge. Sri Bharati Krishna Tirtha Maharaj, who is generally considered the doyen of this discipline, in his seminal book Vedic Mathematics, wrote about this special use of sutras. Vedic Mathematics was the name given by him to this collection of mathematical sutras derived by him from ancient Vedic literatures. He was the person who collected lost formulae from the writings of "Atharwa Vedas" and wrote them in the form of Sixteen Sutras and thirteen sub-sutras. Vedic Mathematics is based on 16 sutras dealing with mathematics related to arithmetic, algebra, and geometry out of these many sutras Vedic multiplication is one popular and pronounced formula used in area of digital image and signal processing.

II. LITERATURE REVIEW

The word 'Vedic' is derived from the word 'veda' which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. These Sutras along with their brief meanings are enlisted below alphabetically.

1) (Anurupye) Shunyamanyat – If one is in ratio, the other is zero
2) Chalana-Kalanabyham – Differences and Similarities.
3) Ekadhikina Purvena – By one more than the previous one
4) Ekanyunena Purvena – By one less than the previous one
5) Gunakasamuchyah – The factors of the sum is equal to the sum of the factors
6) Gunitasamuchyah – The product of the sum is equal to the sum of the product
7) Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10
8) Paraavartya Yojayet – Transpose and adjust.
9) Puranapuranabyham – By the completion or non-completion
10) Sankalana-vyavakalanabhyam – By addition and by subtraction
11) Shesanyankena Charamena – The remainders by the last digit
12) Shunyam Saamyasamuccaye – When the sum is the same that sum is zero
13) Sopaantyadvayamantyam – The ultimate and twice the penultimate
14) Urdhva-tiryakbyham – Vertically and crosswise
15) Vyashtisamanstih – Part and Whole
16) Yaavadunam – Whatever the extent of its deficiency

The study of these formulae is a field of diverse study. The proposed design uses only Urdhva-Tiryakbhyam method hence the detailed description of other formulae is beyond the scope of this project.

III. METHODOLOGY

A. Vedic Multiplier

The Vedic Multiplication Method as per follow:

– These methods aids faster Multiplication and reduces time and increases the throughput via Digital Logic which compare with DCT process from DSP[10] with input factor as image which gives better and faster result:

Vedic Mathematics works on the 16 algorithms or sutras developed and derived from ancient Vedic texts. This particular method for fast multipliers used in digital image and signal processing techniques is named Urdhva Triyakbhyam is more efficient and which consume less time and improves the speed and performance. This method performs multiplication in crosswise and vertically manner it makes all the numeric computations faster by generating partial product and sum in single iteration[4]. The Vedic multipliers are much faster than the conventional multipliers. This gives a scheme for hierarchical multiplier design. This design has high speed, smaller area and less power consumption as compared to the conventional multipliers. Vedic Multiplier also reduces the memory usage of the system [9].

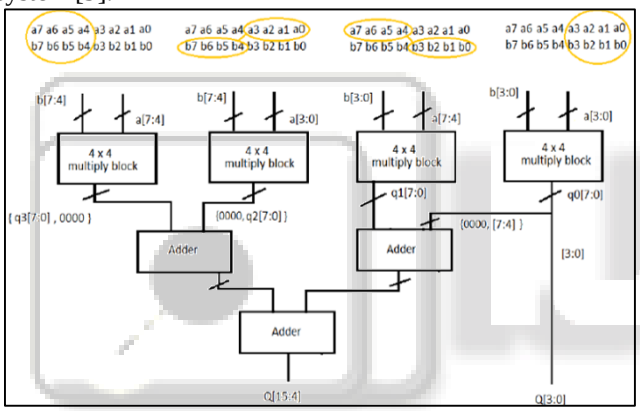

Fig. 1: Block diagram of 16x16 UT Multiplier

B. Discrete Cosine Transform

The discrete cosine transform is a fast transform.

It is a widely used and robust method for image Compression. It has excellent compaction for highly correlated data. DCT has fixed basis images DCT gives good compromise between information packing ability and computational complexity. It transforms the input data into a format to reduce inter pixel redundancies in the input image. Transform coding techniques use a reversible, linear mathematical transform to map the pixel values onto a set of coefficients, which are then quantized and encoded. The key factor behind the success of transform-based coding schemes is that many of the resulting coefficients for most natural images have small magnitudes and can be quantized without causing significant distortion in the decoded image. DCT separates images [12][13][14] into parts of different frequencies where less important frequencies are discarded through quantization and important frequencies are used to retrieve the image during decompression. Compared to other input dependent transforms, DCT has many advantages: It has been implemented in single integrated circuit; It has the ability to pack most information in fewest coefficients; It minimizes the block like appearance called blocking artifact that results when boundaries between sub-images become visible.

IV. PROPOSED SYSTEM

Following ate the series of steps involved in the propose method of digital image and signal processing using Vedic mathematics

A 16*16 Vedic mathematic multiplier is designed using the Urdhva Triyakbhyam sutra. Apply the 16*16 multiplier to a DCT algorithm. Implement and simulate the developed DCT algorithm in MATLAB. Compare the simulated results of these proposed DCT algorithm with normal multiplies and derive a conclusion based on these comparisons.

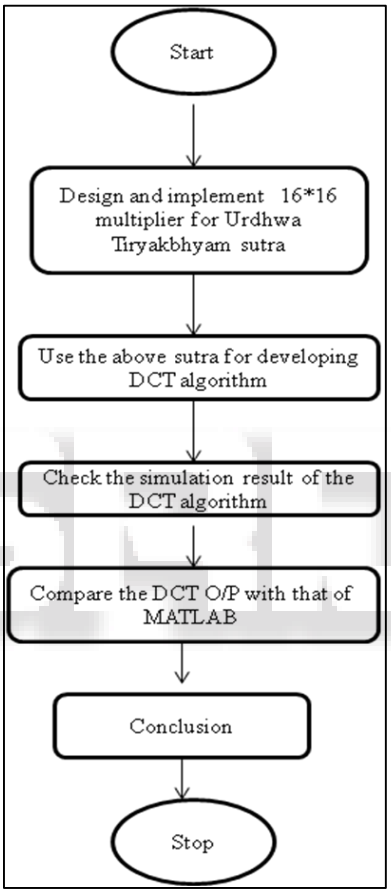

Fig. 2: Flow of Faster Approach to Image Processing using Vedic Mathematics

V. CONCLUSION

Vedic Mathematics gives a clue of symmetric computation. Vedic mathematics deals with various topics of mathematics such as basic arithmetic, geometry, trigonometry, calculus etc. All these methods are very efficient as far as conventional method of multiplication is concerned. The proposed Vedic multiplier proves to be highly efficient in terms of the speed. Vedic multipliers can find immense use in applications of image processing to save time and area.

REFERENCES

[1] S.P.Pohokar, R.S.Sisal,K.M.Gaikwad, M.M.Patil, Rushikesh Borse,"Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics", 2015 International Conference on Industrial Instrumentation

and Control (ICIC), College of Engineering Pune, India. May 28-30, 2015
[2] Honey Durga Tiwari,Ganzorig Gankhuyag, Chan Mo Kim, Yong Beom Cho,"Multiplier design based on ancient Indian Vedic Mathematics",Dept. of Electronics Engineering, Konkuk University, Seoul, South Korea
[3] Rakshith Saligram,Rakshith T.R ,"Optimized Reversible Vedic Multipliers for High Speed Low Power Operations", Proceedings of 2013 IEEE Conference on Information and Communicatio Technologies (ICT 2013)
[4] Akhalesh K. Itawadiya, Rajesh Mahle, Vivek Patel, Dadan Kumar,"Design a DSP Operations using Vedic Mathematics",International conference on Communication and Signal Processing, April 3-5,2013, India
[5] Sudeep. M. C, Sharath Bimba. M, Mahendra Vucha, "Design and FPGA Implementation of High Speed Vedic Multiplier", International Journal of Computer Applications, Volume 90-No. 16, March 2014.
[6] A.M.Raid,W.M.Khedr, El-dosuky, Wesam Ahmed, "Jpeg Image Compression using Discrete CosineTransform - A Survey", International Journal of Computer Science & Engineering Survey (IJCSES) Vol.5, No.2, April 2014
[7] Prakash Narchi, Siddalingesh S Kerur, Jayashree C Nidagundi, Harish M Kittur and Girish V A. Implementation of Vedic Multiplier for Digital Signal Processing. IJCA Proceedings on International Conference on VLSI, Communications and Instrumentation (ICVCI) (16):1–5, 2011. Published by Foundation of Computer Science
[8] Sumit Vaidya and Deepak Dandekar. "Delay-power perfor-mance comparison of multipliers in VLSI circuit design", International Journal of Computer Networks & Communications (IJCNC), Vol.2, No.4, July 2010.
[9] Dr. K.S. Gurumurthy, M.S Prahalad "Fast and Power Efficient 16×16 Array of Array Multiplier using Vedic Multiplication",
[10] Anvesh kumar,Ashish Raman,R K Sarin,Arun Khosla "Small Area Reconfigurable FFT Design by Vedic Mathematics " in Proc IEEE ICAAE'10,Singapoure, vol 5,pp. 836-838,Feb. 2010
[11] T. Stockhammer, M. M. Hannuksela, and T. Wiegand, ―H.264/AVC in wireless environments,‖IEEE Trans. Circuits Syst.Video Technol., vol. 13, no. 7, pp. 657–673, Jul. 2003.
[12] H. Schwarz, D. Marpe, and T. Wiegand, ―Overview of the scalable video coding extension of the H.264/AVC standard,‖IEEE Trans. Circuits Syst. Video Technol., vol. 17, no. 9, pp. 1103–1120, Sep. 2007.
[13] D. Marpe, H. Schwarz, and T. Wiegand, ―Contextadaptive binary arithmetic coding in the H.264/AVC video compression standard,‖IEEE Trans. Circuits Syst. Video Technol., vol. 13, no. 7, pp. 620–636, Jul. 2003
[14] Koren Israel, "Computer Arithmetic Algorithms," 2nd Ed, pp. 141-149, Universities Press, 2001.
[15] J.Bhasker, "Verilog HDL Primer" BS P Publishers, 2003.

