A Review Paper on Reconfigurable Techniques to Improve Critical Parameters of SRAM

Yogit Palan[1] Sangani Vivekkumar D[2] Kalpesh Chheladiya[3] Divyang Shah[4]
[1]P.G. Student
[1,4]Noble Group Of Institutions, Junagadh,Gujarat
[2,3]Dr. Subhash Technical Campus, Junagadh,Gujarat

Abstract— Very Large Scale Integration (VLSI) is the process of manufacturing an integrated circuit (IC) by combining thousands of transistor into a single chip for the production of processors, memories and various application specific ICs. In the world of Electronics Technology, memory devices have always played a noteworthy role in technical advancement. In recent years, the demand of SRAM memory in portable devices and high speed processors has increased significantly. Static means it needs not to be refreshed periodically unlike DRAM. This feature makes SRAM significantly faster than DRAM. In this review paper, different SRAM cell variants are compared and reviewed based on simulation results of various critical parameters like power, dynamic power, delay, area and read/write delay, lower bit line capacitance, reduced metal complexity and notch-less design. These parametric comparisons are dynamically shown for 4T, 6T, 7T, 10T configurations of SRAM cells by using 65, 45 & 32 nm CMOS technologies.

Keywords: SRAM, dynamic power, read/write delay, area, leackage parameters

I. INTRODUCTION

In Design and Analysis of Different Types SRAM Cell Topologies [1] paper, design of different SRAM cells is carried out. This paper compares the performance of five SRAM cell topologies, which include the conventional 6T, 7T, 8T, 9T and the 10T SRAM cell implementations. In particular, the leakage currents, leakage power and read behavior of each SRAM cells are examined. Also, the aim of this paper is to reduce the leakage power, leakage current and improve the read behavior of the various SRAM cell structures using cadence tool at 45nm technology while keeping the read and write access time and the power as low as possible.

In the same way, the main objective of Performance Evaluation of SRAM Cells in 22nm Predictive CMOS Technology[2] paper is to characterize the speed and power consumption of five different SRAM cells in a predictive high performance 22nm transistor process and in a predictive low power 22nm transistor process. The five types of studied cells are traditional 6T, gated-ground 7T, full Self Controlled Voltage Level (SVL) 12T, SVL 9T Footed, and SVL 9THeaded. The simulation results indicate that the timing behavior of SRAM cells are largely the same but power dissipation, leakage power in particular, vary significantly in 22nm technology. The gated-ground 7T cells are deemed superior in the high performance process, while traditional 6T cells are deemed the best in the low power process.

While in Design and evaluation of 6T SRAM layout designs at modern nanoscale CMOS processes [3], Six layout variations of the 6T SRAM cell are examined and compared. The comparison includes four conventional cells, plus the thin cell commonly used in industry and a recently proposed ultra-thin cell. The layouts of the cells are presented and corresponding memory arrays are implemented at 65, 45 and 32 nm using 3-metal CMOS n-well process. The obtained designs are compared in terms of area, power dissipation and read/write delay, using proper BSIM4 level simulations. The thin cell presents the best results regarding area efficiency and delay. In terms of power dissipation, it performs poorly at 65 and 45 nm but appears to be the best at 32nm, presenting great improvement with downscaling. The ultra thin cell provides a more lithographically friendly alternative to the thin cell, with lower power dissipation at 65 and 45 nm and higher at 32 nm. Overall, it performs worse in area and power relative to most conventional designs and gets worse with downscaling.

As given in New category of ultra-thin notchless 6T SRAM cell layout topologies for sub-22nm[4] paper, the extent to which the 6T SRAM bit cell can be perpetuated through continued scaling is of massive technological and economic significance Understanding the growing limitations in lithography, design and process technology, coupled with the mechanisms which drive systematic mismatch, provides direction in identifying more optimum solutions. We propose an alternative, ultra-thin(UT) SRAM cell layout topology as a means to address many of the challenging bit cell design constraints facing the most advanced CMOS process technologies today. Compared to the industry standard 6T topology, the newly proposed cell offers: 1) a lower bit line capacitance, 2) reduced M1 complexity and 3) notch-less design for improved resistance to alignment induced device mismatch.

II. POWER AND LEAKAGE PARAMETERS ANALYSIS

In conventional 6T SRAM, the read operation is performed by pulling the word line high and accessing the latch by access transistors. This may lead to disturbance and corruption of the data stored in the cell, due to static noise.

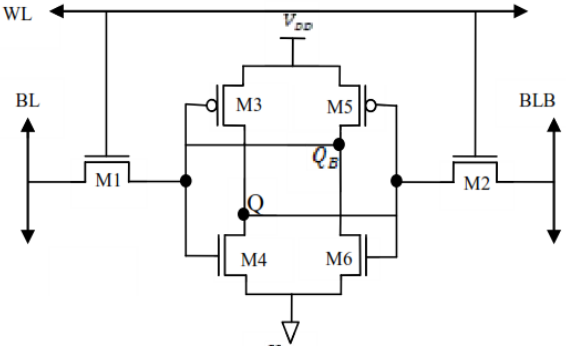

Fig. 1: Schematic of 6T SRAM cell [1]

In 7T SRAM cell structure, the cell consists of an additional transistor placed in the ground path of a 6T SRAM cell to reduce leakage while the cell is in standby mode [1]. In the standby mode, the bottom transistor is intended to cut-off the ground path and to eliminate the leakage paths through the inverter transistor sources but this cell cannot increase the read speed.

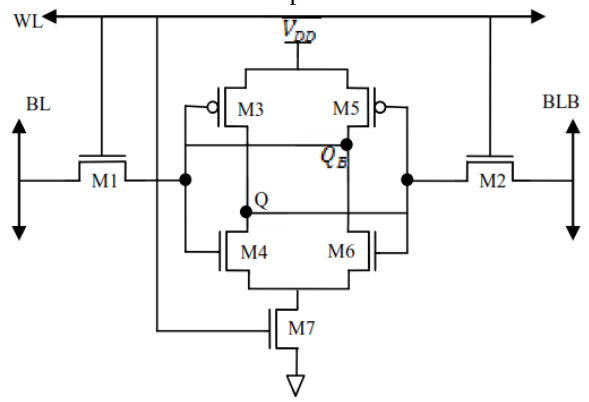

Fig. 2: Schematic of 7T SRAM cell [1]

To overcome the problem of data storage destruction during the read operation, an 8T-cellimplementation was used, for which separate read/write bit and word signal lines are used to separate the data retention element and the data output element. In turn, the cell implementation provides a read-disturb-free operation.

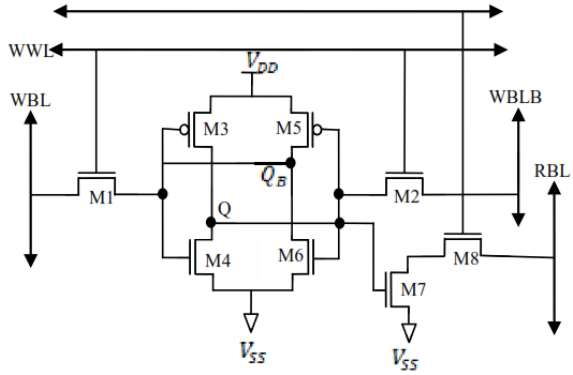

Fig. 3: Schematic of 8T SRAM cell [1]

A 9T SRAM cell is used for simultaneously reducing leakage power and enhancing data stability. The 9T SRAM cell completely isolates the data from the bit lines during a read operation. The read static-noise-margin of the used circuit is thereby enhanced as compared to a conventional 6T SRAM cell. The idle 9T SRAM cells are placed into a super cut-off sleep mode, thereby reducing the leakage power consumption.

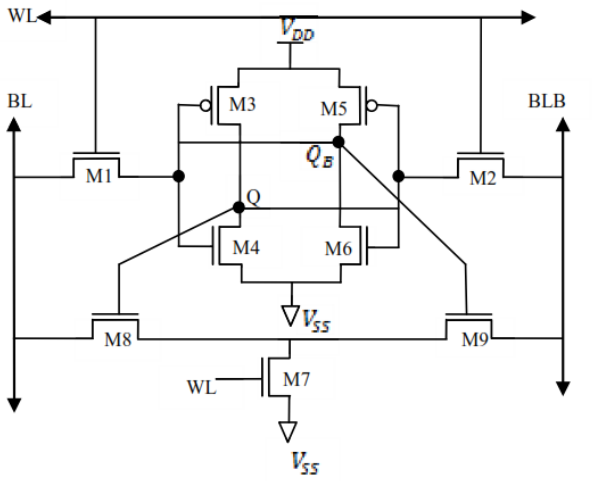

Fig. 4: Schematic of 9T SRAM cell [1]

The SRAM structures have been designed to limit the noise in read operation by adding a different circuit for read operation which isolates the basic memory element from the external noise keeping the access transistors disabled while reading the cell. The 10T structure, shown in Fig .5, employs an inverter as transmission gate connected to the Qb (QBar) of the cell.

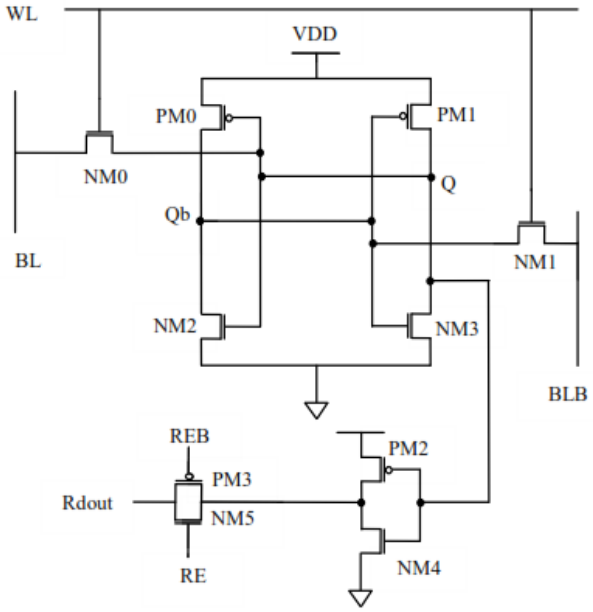

Fig. 5: Schematic of 10T SRAM cell [1]

The variation of power against supply voltage Vdd as been illustrated in Fig .6. These Figs confirm the power stability of the cell even at raised temperature and supply voltage. Fig .6 shows the leakage power waveform of 10T SRAM cell.

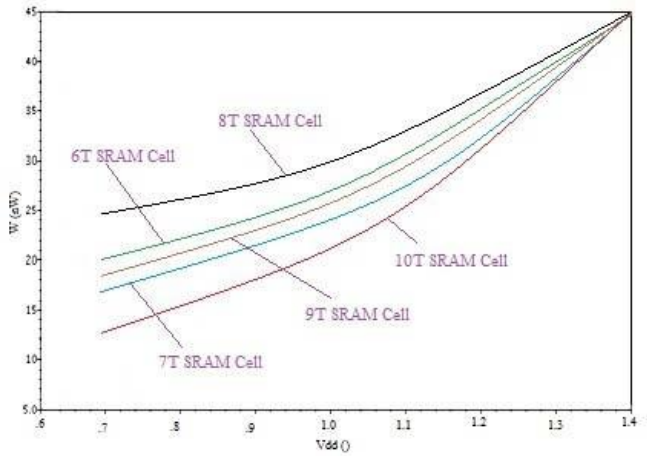

Fig. 6: Power versus Vdd Curves of 6T, 7T, 8T, 9T and 10T SRAM Cells.

Unlike the high performance transistor SRAM cell implementations, the write timing performance amongst the different SRAM cells implemented in the low power process is not the same[2]. In this case, the 6T SRAM cell is approximately 50% slower than any of the other cells. With the exception of the 6T SRAM cell, the write timings of the low power transistor SRAM cells are approximately the same. This seems to indicate the the transistor stacking along the rails in the low power transistor technology substantially weakens an SRAM cell, allowing it to more easily be overwhelmed by the write pump. The read times for the low power transistor SRAM cells are generally twice as long as the read times for the cells implemented with the high power transistors. However, within the low power transistor SRAM cells, the relative read speed profile between the cells is identical to the relative read speed profiles within the high power transistor SRAM cells. Once again, the 6T is the fastest cell and the 7T is the slowest cell.

	6T	7T	SVL 12T	SVL 9T Footed	SVL 9T Headed
$P_{leakage}$	0.010	0.017	0.034	0.028	0.020
P_{read0}	372	276	340	339	369
P_{read1}	337	272	323	324	355
$P_{write0\rightarrow0}$	92	45	43	58	89
$P_{write0\rightarrow1}$	1485	1637	1775	1768	2112
$P_{write1\rightarrow0}$	1338	1068	1259	1022	1403
$P_{write1\rightarrow1}$	37	20	16	13	30

Table 1: Ptm Low Power (Lp) 22nm V2.1 Sram Cell Rms Power Innanowatts(Nw)

III. AREA COMPARISON OF CELL VARIANTS

The cells presented above are to be used for the construction and evaluation of memory arrays, thus we used each cell type to design 4x4 (16-bit) SRAM arrays. Every array type is implemented with the maximum area efficiency that the corresponding cell can provide, given the design rules followed. Hence, some cells are properly flipped horizontally or vertically in order to partially merge and overlap with neighboring cells. This results in different cells sharing the same polysilicon, diffusion or n-well areas, as well as metal wires and contacts. Furthermore, n-well taps and substrate contacts may be shared among multiple cells for additional area efficiency.

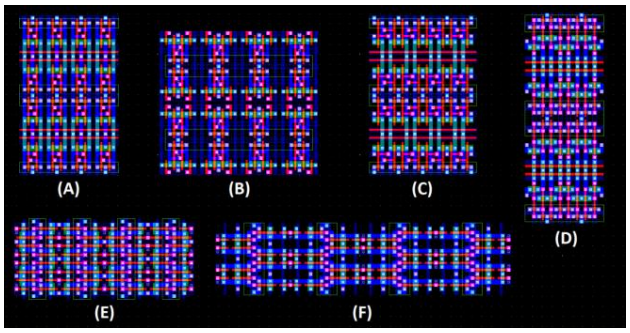

Fig. 7: Layout of Type 1a (A), 1b (B), 2 (C), 3 (D), 4 (E) and 5 (F) 16-bit SRAM memory array[3]

The connections inside the cells are implemented with metal-1 wires and polysilicon gates, while the I/O routing (word lines and bit lines) is implemented withmetal-2 and metal-3 wires. The layouts of the 16-bit arrays are shown in Fig. 7[3].

After comparing the layouts of the various 16-bit SRAM architectures, it can be safely assumed that the T4 thin cell presents the highest area efficiency. TheT4 cells overlap on all four sides, thus saving significant area by shared diffusions and contacts. The T5 cells also overlap on all sides, but they leave a lot of area unoccupied between them, resulting in an area-inefficient structure. Indicatively, at the 32 nm, the T4 array covers an area of 3.186 µm, which is7.97%, 13.14%, 14.9%, 32.6% and 36.0% less than the T1a, T3, T2, T5 and T1b designs, respectively. The T1a, T3 and T2cells are close at 3.462, 3.668, and 3.744 µm. The T5 ultrathin cell performs worse than most basic cells, at 4.730 µm.The T1b cell results in the largest layout at 4.984 µm. A similar analogy can be derived for the 65 and 45 nm circuits. The area and bit density of the SRAM arrays is shown in Table II.

	65 nm		45 nm		32 nm	
SRAM Type	***Area (μm^2)***	***Bit Density (μm^2/bit)***	***Area (μm^2)***	***Bit Density (μm^2/bit)***	***Area (μm^2)***	***Bit Density (μm^2/bit)***
T1a	18.849	1.178	6.154	0.385	3.462	0.216
T1b	27.136	1.696	8.861	0.554	4.984	0.312
T2	20.386	1.274	6.657	0.416	3.744	0.234
T3	19.970	1.248	6.521	0.408	3.668	0.229
T4	17.346	1.084	5.664	0.354	3.186	0.199
T5	25.754	1.610	8.410	0.526	4.730	0.296

Table 2: Area And Bit Density Of Sram Arrays[3]

Using the same set of pushed SRAM layout rules, the newly defined bit cell does not achieve the density calculated for the type 4 layout. This is partially due to the fact that the pushed rules used today are clearly optimized for the type 4layout topology. The calculated cell areas based on the equations given here and published 6T bit cell areas are shown in Fig. 8. It is not clear if the deviation from $120\lambda^2$evident in published conventional cell sizes is driven purelyby W and L up-sizing or if lithography limitations are playing a larger role. This deviation from the traditional scaled area may indicate that the type 4 layout is hitting limitations in scaling, which will renew interest in alternative topologies such as proposed here[4].

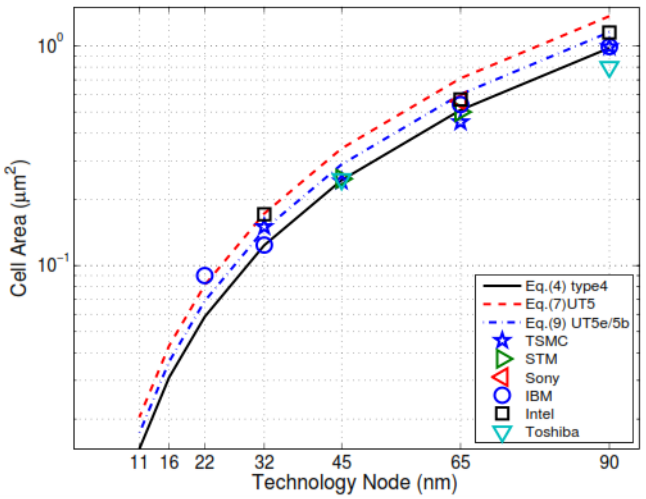

Fig. 8: calculated area for topology 5 cell across multiple technology nodes

A comparison of bit cell metrics[4] that highlight the key differences by cell type is given in Table III. The bit cell area, BL length (L), and number of required metal levels is summarized. Because the number of contacts required per cell is also a metric of interest, this metric highlights an additional advantage of the type 5 topology.

	Cell Type			
Metric	**4**	**5**	**5e**	**5b**
Number contacts/cell	6	8	4	4
Number shared contacts/cell	2	2	2e	2b
Cell area (λ^2)	120	168	142	142
L_{BL} (λ)	7.5	6.5	5.5	5.5
Number metal levels	3	3	3	2

Table 3: SRAM bit cell metric comparison by cell type[4]

IV. Read and Write Delay Analysis

All SRAM cells, as well as the 16-bit SRAM arrays, are simulated [5]with five different operating voltages (0.8, 0.7, 0.6, 0.5 and 0.4 V) at room temperature (27° C) and 1 GHZ frequency. For all the designs and simulations, a BSIM4 level model for low-leakage nMOS and pMOS transistors at 32nm is used.

Two major delays i.e. write and read delay are considered as one of the significant performance oriented parameter for the working of any SRAM cell variants.

A. *Write Delay:*

Write delay is defined as the interval time between the assertion of word line and the recording of new data in bit cell nodes. To calculate the write delay [5], two cases need to be taken into account, from which we calculate and present the average value: writing '1' when the bit-cell contains '0' and writing '0' when the bit-cell contains '1'. There is no delay when writing the same binary value in bit-cell.

According to the simulations, the type 4 cell achieves the best write delay for all supply voltages. In contrast, type 5 cell has slightly worse write delay than the other cells. The write delay simulation results are presented on Table IV.

Cells	Supply Voltage				
	0.4 V	**0.5 V**	**0.6 V**	**0.7 V**	**0.8 V**
Type 1b	21 ps	12 ps	8.5 ps	7.5 ps	6.5 ps
Type 2	20 ps	11.5 ps	8.5 ps	7.5 ps	6 ps
Type 4	17 ps	10 ps	7.5 ps	6 ps	5.5 ps
Type 5	22 ps	13 ps	10 ps	8 ps	7 ps

Table 4: Write Delay Of Sram Cell Variants [5]

B. *Read Delay:*

To calculate the delay of the read operation, an external circuit has to be used for signal sensing. In this simulation, large signal sensing method can be used [5], specifically a pair of HI-skew inverters connected to the bit lines. The layout of the inverter pair is shown in fig. 9. The transistor sizes for the inverters are: Wp = 7λ, Wn = 3λ, Lp = Ln = 2λ.

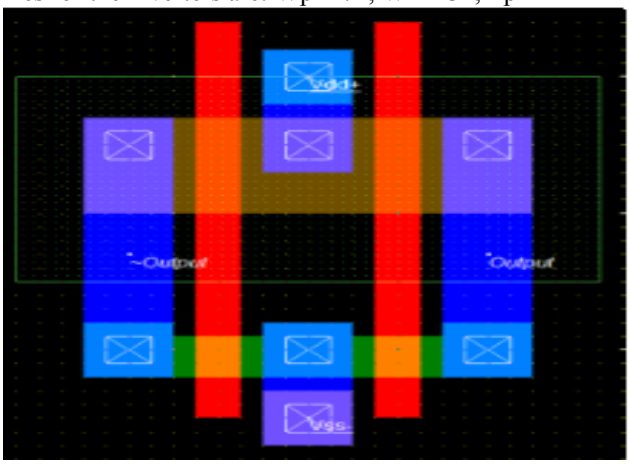

Fig. 9: Layout of Hi-skew inverter pair

Therefore, the read delay is defined as the interval time between the assertion of the word line and the rise of Output node when reading '0' or the rise of Output node when reading '1'. The average delay time of the two cases is considered.

According to the simulations, all cells provide similar read delay measurements, since the reading speed largely depends on the external circuit that is used, which is identical in all cases. The read delay simulation results are presented on Table V.

Cells	Supply Voltage				
	0.4 V	**0.5 V**	**0.6 V**	**0.7 V**	**0.8 V**
Type 1b	21 ps	11 ps	8 ps	6 ps	6 ps
Type 2	20 ps	11 ps	8 ps	6 ps	5 ps
Type 4	20 ps	11 ps	8 ps	6 ps	5 ps
Type 5	20 ps	11 ps	8 ps	6 ps	5 ps

Table 5: Read Delay Of Sram Cell Variants [5]

V. Conclusion

Various types of 6T SRAM cell layout architectures and corresponding 16-bit arrays have been reviewed and conclusively compared at the 32 nm, in terms of effective area, power dissipation and read/write delay. The T4 (thin) cell seems to be the most viable layout topology among all topologies for further development, since it seems to get comparatively better with downscaling. The recently proposed ultra-thin cell (T5) provides a more lithographically friendly alternative to the thin cell but introduces a significant penalty in area and power/delay performance, presenting overall worse results than the conventional designs.

REFERENCES

[1] Design and Analysis of Different Types SRAM Cell Topologies
[2] Performance Evaluation of SRAM Cells in 22nm Predictive CMOS Technology
[3] Design and evaluation of 6T SRAM layout designs at modern nanoscale CMOS processes
[4] New category of ultra-thin notchless 6T SRAM cell layout topologies for sub-22nm
[5] "Design and simulation of 6T SRAM cell architecture in 32nm technology"

