Simulation of Neutral Point Clamped Multilevel Inverter

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Abstract— In this paper MATLAB simulation of neutral point clamped type multilevel inverter is consist. Previously two level inverter was widely used in power industry but in case of two level inverter major problems was power quality so to compensate this problem multilevel topology comes in the power industry. Multilevel inverter is beneficial in power quality improvement compare to the two level inverter.

Key words: Clamping Diodes, Neutral Point

I. INTRODUCTION

The diode-clamped multilevel inverter employs clamping diodes and cascaded dc capacitors to produce ac voltage waveforms with multiple levels. The inverter can be generally configured as a three-, four-, or five-level topology, but only the three-level inverter, often known as neutral-point clamped (NPC) inverter, has found wide application in high-power medium-voltage (MV) drives. The main features of the NPC inverter include reduced *dv*/*dt* and THD in its ac output voltages in comparison to the two-level inverter discussed earlier. More importantly, the inverter can be used in the MV drive to reach a certain voltage level without switching devices in series. For instance, the NPC inverter using 6000-V devices is suitable for the drives rated.

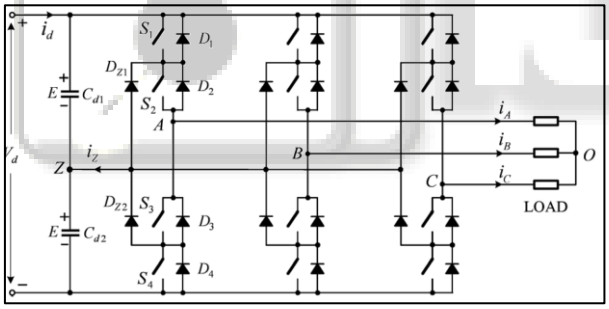

Fig. 1: Three Level NPC Inverter

II. SWITCHING STATE

The operating status of the switches in the NPC inverter can be represented by switching states shown in Table. Switching state 'P' denotes that the upper two switches in leg *A* are on and the inverter terminal voltage *VAZ*, which is the voltage at terminal *A* with respect to the neutral point *Z*, is +*E*, whereas 'N' indicates that the lower two switches conduct, leading to *VAZ* = –*E*. Switching state 'O' signifies that the inner two switches *S*2 and *S*3 are on and *VAZ* is clamped to zero through the clamping diodes.

Switching State	Device Switching Status (Phase *A*)				Inverter Terminal Voltage
	S_1	S_2	S_3	S_4	v_{AZ}
P	On	On	Off	Off	E
O	Off	On	On	Off	0
N	Off	Off	On	On	$-E$

Fig. 1.1: Switching States

It can be observed from Table that switches *S*1 and *S*3 operate in a complementary manner. With one switched on, the other must be off. Similarly, *S*2 and *S*4 are a complementary pair as well.

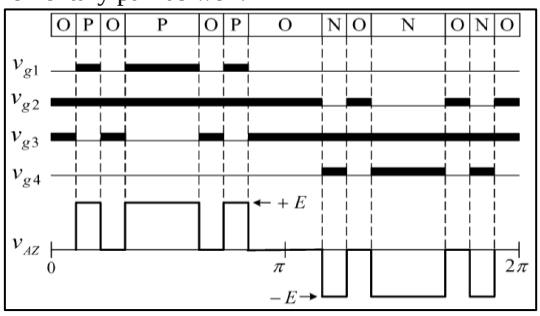

Fig. 2: Switching States, Gate Signals And Inverter Terminal Voltage VAZ

A. Case 1: Commutation with iA > 0.

It is assumed that (a) the load current iA is constant during the commutation due to the inductive load, (b) the dc bus capacitors Cd1 and Cd2 are sufficiently large such that the voltage across each capacitor is kept at E, and c) all the switches are ideal. In switching state [O], switches S1 and S4 are switched off while S2 and S3 conduct. The clamping diode DZ1 is turned on by the positive load current (iA > 0). The voltages across the on-state switches S2 and S3 are given by vS2 = vS3 = 0, while the voltage on each of the off-state switches S1 and S4 is equal to E. During the _ interval, S3 is being turned off. The paths of iA remain unchanged. When S3 is completely switched off, the voltages across S3 and S4 become vS3 = vS4 = E/2 due to the static voltage sharing resistors R3 and R4. In switching state [P], the top switch S1 is gated on (vS1 = 0). The clamping diode DZ1 is reverse-biased and thus turned off. The load current iA is commutated from DZ1 to S1. Since both S3 and S4 have already been in the off-state, the voltage across these two switches is equally divided by R3 and R4, leading to vS3 = vS4 = E.

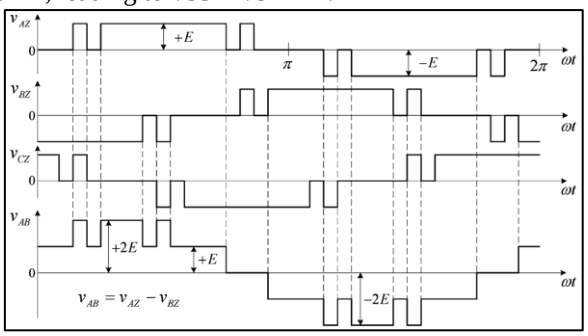

Fig. 3: Inverter Terminal And Line-To-Line Voltage Waveforms

B. Case 2: Commutation with iA < 0.

In switching state [O], S2 and S3 conduct, and the clamping diode DZ2 is turned on by the negative load current iA. The voltage across the off-state switches S1 and S4 is vS1 = vS4 = E. During the _ interval, S3 is being turned off. Since the

inductive load current iA cannot change its direction instantly, it forces diodes D1 and D2 to turn on, resulting in vS1 = vS2 = 0. The load current is commutated from S3 to the diodes. During the S3 turn-off transient, the voltage across S4 will not be higher than E due to the clamping diode DZ2, and it will also not be lower than E since the equivalent resistance of S3 during turn-off is always lower than the off-state resistance of S4. Therefore, vS3 increases from zero to E while vS4 is kept at E. In switching state [P], the turn-on of S1 does not affect the operation of the circuit. Although S1 and S2 are switched on, they do not carry the load current due to the conduction of D1 and D2

- To summarize, the three-level NPC inverter offers the following features:
- No dynamic voltage sharing problem. Each of the switches in the NPC inverter withstands only half of the total dc voltage during commutation.
- Static voltage equalization without using additional components. The static voltage equalization can be achieved when the leakage current of the top and bottom switches in an inverter leg is selected to be lower than that of the inner switches.
- Low THD and dv/dt. The waveform of the line-to-line voltages is composed of five voltage levels, which leads to lower THD and dv/dt in comparison to the two-level inverter operating at the same voltage rating and device switching frequency.

III. MATLAB SIMULINK DIAGRAM

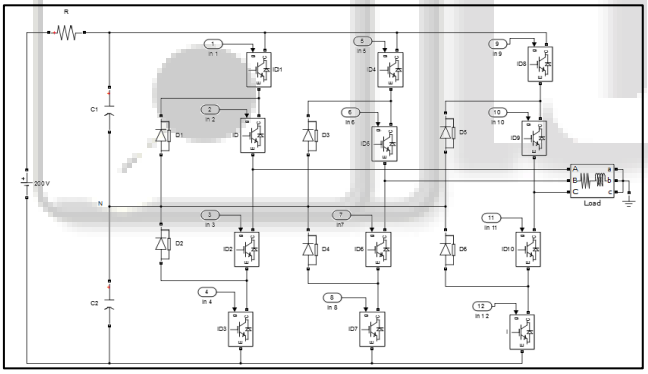

Fig. 4: Simulation of Three Level NPC Inverter

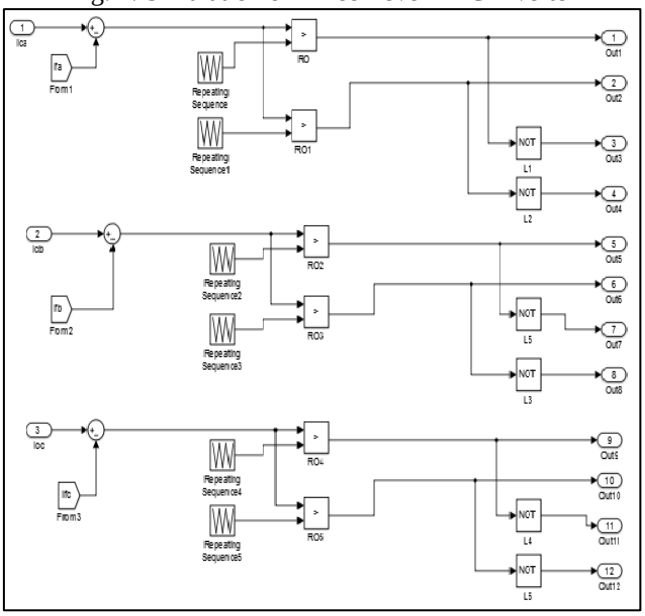

Fig. 5: Sub System of Firing Circuit

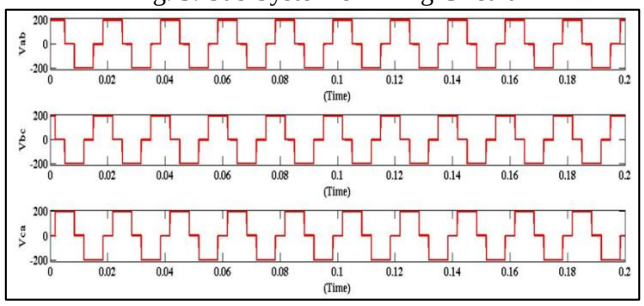

Fig. 6: Output Waveform of Terminal Voltage

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