# Modeling and Comparison of Single Gate and Dual Gate Organic Thin Film Transistor

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*Abstract*— In this paper OTFT basics, working, analytical model and dual gate OTFT is presented in detail with methodology and simulation setup used in the work. Furthermore a comparison in single and dual gate OTFT parameters has been given. And shows that dual gate OTFT has superior performance over single gate OTFT in terms of mobility, current on–off ratio, transconductance, sub-threshold slope and threshold voltage.

***Key words:*** OTFT, Dual Gate, Mobility, Current On–Off Ratio, Transconductance, Sub-Threshold Slope and Threshold Voltage

## I. INTRODUCTION

The thin-film transistor (TFT) is a special type of field-effect transistor in which the semiconductor is deposited as a thin film on an insulating substrate, such as glass or plastic foil. Generally, intrinsic (undoped) semiconductors are used in TFTs.

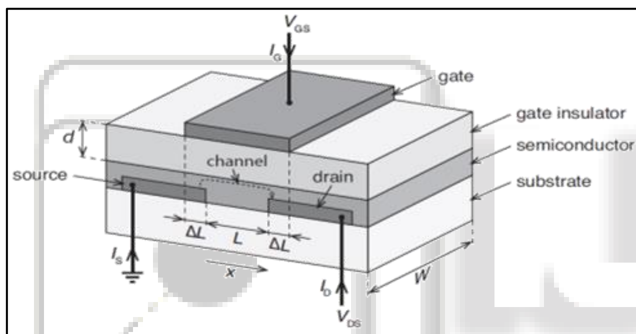


Fig. 1: Schematic structure of a thin-film transistor with channel width W, Channel length L and parasitic gate overlap ΔL.

Inorganic TFTs are usually based on either hydrogenated amorphous silicon (a-Si:H) or polysilicon, and are widely used in the addressing backplane for active-matrix liquid crystal displays (AMLCDs). thin-film transistor is a three-terminal device that consists of an electronically insulating material, which commonly referred as the gate insulator, or the gate dielectric sandwiched between a thin semiconductor layer and a gate electrode. Furthermore, a source and a drain electrode are in direct contact with the semiconductor, as for MOSFETs the Source terminal for inject carriers, and the Drain for extract carriers. The region between source and drain electrodes represents the channel, channel width $W$ is given by the extension of the electrode and channel length $L$ is given by the separation of the electrodes. The source electrode is usually grounded, and thus it can be used as the reference for the gate voltage and drain voltage. The potential difference between the gate and the source is called the gate-source voltage ($V_{GS}$) or just the gate voltage. Similarly, the drain-source voltage ($V_{DS}$) or simply the drain voltage is referred as the potential difference between the drain and the source. The gate-insulator-semiconductor interface work as a capacitor. A dielectric gate insulator capacitance per unit area, $C_i$, is given by

$$C_i = \frac{\epsilon_0 k}{d} \qquad (1.1)$$

Where $\varepsilon_0$ is the vacuum permittivity, κ is the relative permittivity and $d$ is the thickness of the gate insulator layer.

Hence, by applying a voltage to the gate electrode, charges can be induced at the insulator-semiconductor interface. Negative charges (electrons) induce in the semiconductor with a positive gate voltage, while a negative voltage induces positive charges (holes). These charges, at the insulator semiconductor interface, [1] formed a conducting path between the source and drain electrodes called channel that will dramatically increase the conductivity of the semiconductor surface. A channel formed by positive charge is called *p*-channel, and a negatively charged channel is called *n*-channel. By using varying gate voltage the conductance of this channel can be modulated. Ambipolar Materials can form both *p*- and *n*-channels, depending on the applied voltage [2]. However, the applied gate voltage at which the Channel becomes conducting called the threshold voltage $V_t$. Organic TFTs are based on intrinsic semiconductors and operate in the accumulation regime. Therefore practically the threshold voltage should be zero. But, the threshold voltage is generally nonzero due to differences in the work functions of the semiconductor and the gate material, the presence of localized states (traps) at the insulator-semiconductor interface and residual charges in the bulk of the semiconductor film [3].

## II. STRUCTURES OF OTFT

Primarily, An OFET can be distinguished in several configurations (Fig.2). Regarding to the gate deposition, the structure of a thin film transistor is described as the top gate (TG) and the bottom gate (BG) structures. Gate can be deposited over the substrate with the dielectric layer on top i.e. bottom-gate configuration or the gate dielectric at the top of the whole structure i.e. top-gate configuration similar to the conventional MOSFET structure. However, bottom gate structure is commonly used because it is easy to deposit the organic material on the insulator rather than converse; also there is less possibility for the OSC layer to get contaminated by the fabrication processes. On the basis of the position of the source and drain contacts deposited on the semiconducting layer or under the semiconductor while keeping gate electrode at the same position, the structure is called the top-contact configuration and the bottom-contact configuration respectively [4]. The top contact configuration gives better performance in comparison to the bottom contact because of the less morphological disorders in the active layer in top contact [5]. Accordingly we can have top-contact bottom-gate configuration (Fig.2 a), bottom-contact bottom-gate configuration (Fig.2 b), bottom-contact top-gate

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configuration (Fig.2 c) and top-contact top-gate configuration (Fig.2 d).

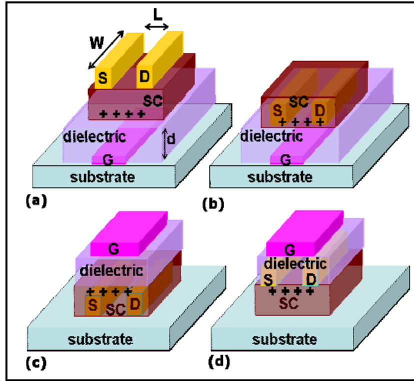


Fig. 2: Different OFET structures: (a) top-contact bottom-gate, (b) bottom-contact bottom-gate, (c) bottom-contact top-gate and (d) top-contact top-gate

## III. SIMULATION SETUP OF SINGLE GATE OTFT

The dimensions of a single gate p-type pentacene OTFT used in this work are obtained from a fabricated commercial technology, summarized in Table 1 [6]. This single gate has a channel length of 25 mm and a channel width of 800 mm. For device fabrication a heavily doped silicon wafer was used as a bottom gate electrode 150 nm and the substrate. The silicon wafer was thermally oxidized to form a layer of SiO2 100 nm thick as bottom gate dielectric. Next, a layer of Au, 80 nm thick, was sputtered on top of SiO2 gate dielectric, to form the source and drain electrodes. After that, the pentacene 200 nm thick was deposited as an organic semiconductor layer.

### A. *Device Dimensions*

| S.N | Parameters | Dimension | Material |
|---|---|---|---|
| 1. | Width (W) | 800μm | |
| 2. | Length (L) | 25μm | |
| 3. | Organic Semiconductor thickness ($t_{osc}$) | 200nm | Pentacene |
| 4. | Source & Drain thickness | 80nm | Au |
| 5. | Bottom Dielectric thickness BG ($t_{ox}$) | 100nm | $SiO_2$ |
| 6. | Bottom Gate thickness (BG) | 150nm | $n^+$ Si |

Table 1: Structural dimensions and materials of single gate OTFT

### B. *Simulated Device Structure*

Fig.3 shows the device structure of the OTFT after the numerical simulation on the physically- based device simulator.

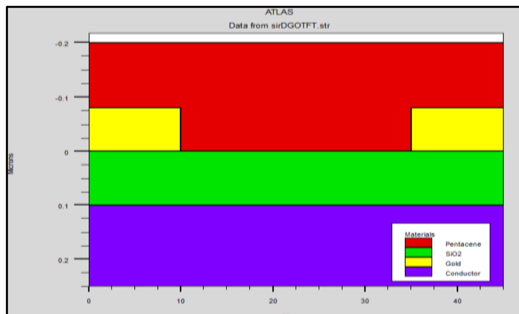


Fig. 3: Structure of Single Gate OTFT

## IV. SIMULATION RESULTS OF SINGLE GATE OTFT

The transfer characteristics of OTFT with a thin 200 nm pentacene semiconducting layer have been shown in fig.4.

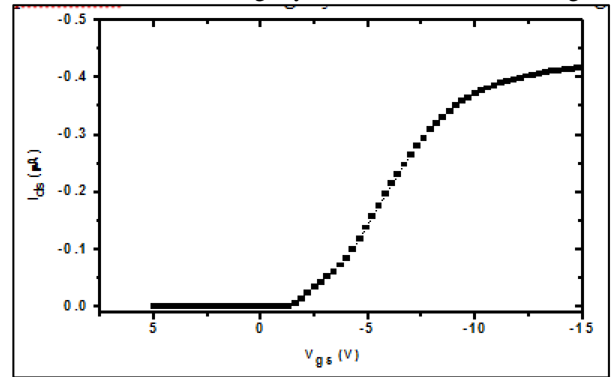


Fig. 4: Transfer characteristics ($I_{ds}$-$V_{gs}$) of single gate OTFT

Directly after pentacene deposition, the transfer and output characteristics were measured to determine the performance of the initial OTFT prior to the formation of the top-gate dielectric and top-gate electrode. The drain current-voltage characteristics of the initial OTFT as a function of the gate voltage exhibited good current saturation as well as negligible contact resistance, as presented in Fig.5.

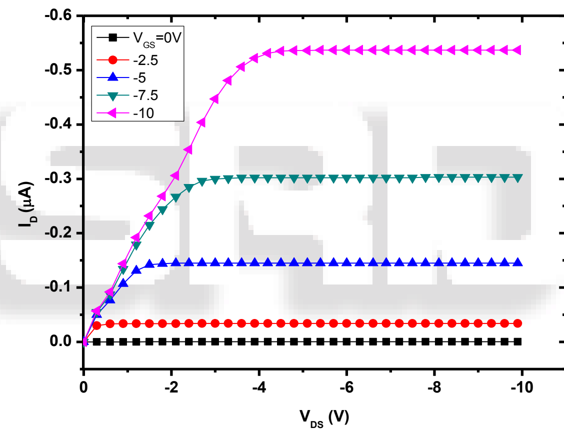


Fig. 5: Output characteristics ($I_{ds}$-$V_{gs}$) of single gate OTFT

Applying a voltage above the threshold voltage and a drain voltage will generate a flow of charge carriers through the channel, from the source to the drain. When the applied drain voltage is small ($V_{DS} < V_{gs} - V_T$), the resistance of the channel is not changed effectively so The drain current $I_D$ is proportional to the drain voltage (Fig.5), defines the *linear regime* in the output characteristics. In the *saturation regime*, When $V_{DSsat} > V_{GS} - V_T$ , number of charge carriers arriving at pinch off point is constant, as a result the drain current become saturate at $I_{Dsat}$ as shown in the output characteristics. The electrical parameters of initial i.e. single gate structure are tabulated in Table2.

| Parameters | Simulated values | Theoretical values |
|---|---|---|
| mobility (μ) | 0.0241708 | 0.02 cm2/V s |
| Threshold voltage (Vt ) | -2.77399 | -2.0 V |
| Ion/Ioff | 3.223e+003 | 3.2e+003 |
| Subthreshold slope (S.S) | 2.33328 | 2.0 V/dec. |
| Transconductance ($g_m$) | 0.03954 | 0.044 μS |

Table 2: Simulated electrical parameters of single gate OTFT

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## V. DUAL GATE OTFT STRUCTURE

The DG-OFET is basically a combination of a top-gate (top-contact) stacked on a bottom-gate (bottom-contact) OFET and these two OFET shares the source and drain electrodes and the semiconductor layer, at the same time as the two gates can be designed to be independent or alternatively electrically connected.

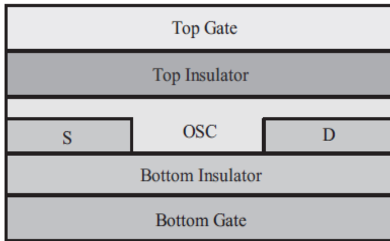


Fig. 6: Schematics of dual-gate OTFT structure

So this structure consists of a gate in the bottom (BG) along with its bottom insulator (BI), a top gate (TG) with a top insulator (TI), organic semiconductor, and S/D contacts. The bottom gate accumulates the carriers in the channel, while the conductivity of the channel electrostatically when a bias on the top gate further increases. Therefore, the additional gate can control the threshold voltage (*Vt*), but at an extra cost of gate material and increased fabrication steps.

## VI. SIMULATION SETUP OF DUAL GATE OTFT

The organic dual gate structure is analyzed through organic module of Silvaco Atlas 2-D numerical device simulator. Material parameters are specified in table 3.2. These values are typical for pentacene organic semiconductor. For calculating the current in the dual-gate transistors, a mesh was defined and at each point Poisson's equation, the continuity equations and the drift-diffusion equations were iteratively solved. P-type OSC material pentacene is formed the conducting channel. Intended for finite element based simulation, Poole-Frenkel mobility model is expressed as

$$\mu(E) = \mu_0 \exp[-\frac{\Delta}{kT} + (\frac{\beta}{kT} - \gamma)\sqrt{E}] \qquad (6.1)$$

| Parameter | Symbol | Value |
|---|---|---|
| Dielectric permittivity | $\epsilon_i$ | 3.9 |
| Semiconductor permittivity | $\epsilon_{osc}$ | 4 |
| Electron affinity | Qχ | 2.5Ev |
| Energy gap | $E_g$ | 2.8eV |
| Valance band density | $N_v$ | $1.0 \times 10^{21}$ $cm^{-2}$ |
| Conduction band density | $N_c$ | $1.0 \times 10^{21}$ $cm^{-2}$ |
| Metal work function | $\phi_m$ | 5.1 |

Table 3: Material parameters used in simulation

Where μ (E) represent field dependent mobility, E electric field and $\mu_0$ zero field mobility. Activation energy specified by D, hole Poole-Frenkel constant is b and c is used as the fitting parameter. The activation energy is in the range of 0.005–0.050 eV [7]. For pentacene material the values of D and b are considered as $1.792\times10^{-2}$ eV and $7.758\times10^{-5}$eV $(cm/V)^{0.5}$, respectively. However, the activation energy is reported in the range of 0.02–0.04 eV for high mobility P3HT material [8]. relative permittivity of pentacene is considered as 4 whereas, Effective density of states in the conduction ($N_C$) and valence band ($N_V$) are assumed in the order of ~$10^{21}$ [9]. The dimensions of dual gate p-type pentacene OTFT used in this work are obtained from a fabricated commercial technology, summarized in Table 3.3. This FET has a channel length of 25 mm and a channel width of 800 mm. For device fabrication a heavily doped silicon wafer was used as a bottom gate electrode 150 nm and the substrate. the silicon wafer was thermally oxidized to form a layer of SiO2 100 nm thick as bottom gate dielectric.

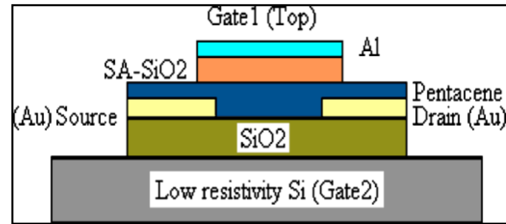


Fig. 7: Schematic of dual gate organic thin film transistor

Next, a layer of Au, 80 nm thick, was sputtered on top of $SiO_2$ gate dielectric, to form the source and drain electrodes. After that, the pentacene 200 nm thick was deposited as an organic semiconductor and a top gate layer of Al, 150 nm thick, was evaporated on top of gate dielectric SiO2 layer is about 300 nm.

### A. Device Dimensions

| S.N. | Parameters | Dimensions | Material |
|---|---|---|---|
| 1. | Width (W) | 800µm | |
| 2. | Length (L) | 25µm | |
| 3. | Organic Semiconductor thickness ($t_{osc}$) | 200nm | Pentacene |
| 4. | Top Dielectric thickness TG ($t_{ox}$) | 300nm | $SiO_2$ |
| 5. | Source & Drain thickness | 80nm | Au |
| 6. | Bottom Dielectric thickness BG ($t_{ox}$) | 100nm | $SiO_2$ |
| 7. | Top Gate thickness (TG) | 150nm | Al |
| 8. | Bottom Gate thickness (BG) | 150nm | $n^+$ Si |

Table 4: Structural dimensions and materials of dual gate OTFT

### B. Simulated Device Structure

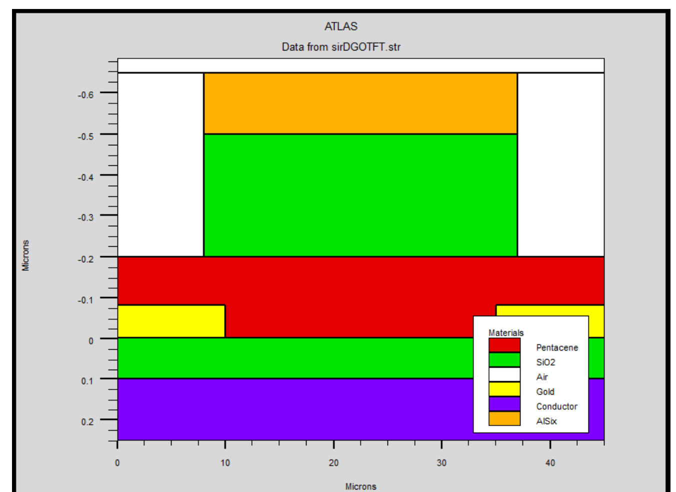


Fig. 8: Structure of dual gate OTFT device

## VII. SIMULATION RESULTS OF DUAL GATE OTFT

The linear transfer characteristics of dual gate mode measured at a drain bias of -2.5 V are presented in Fig9.

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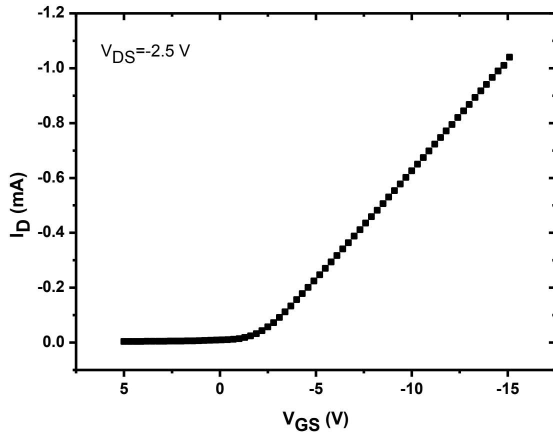

Fig. 9: Transfer characteristics ($I_{ds}$-$V_{gs}$) of DG-OTFT structures, Channel length L = 25µm.

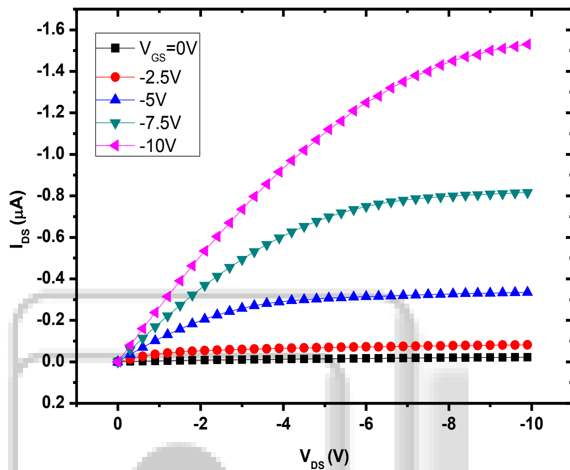

Fig. 10: Output characteristics ($I_{ds}$-$V_{ds}$) of DG-OFET structures. $V_{GS}$ varies from 0 to -10V in 5 steps. Channel length L = 25µm.

The output characteristics of dual gate device are validated with a drain to source voltage bias range of 0V to -20V with different gate voltage bias of 0V to -20V. The obtained electrical parameters are listed below.

| Parameters | Simulated values | Theoretical values |
|---|---|---|
| mobility (µ) | 0.157672 | 0.1 cm2/V s |
| Threshold voltage (Vt ) | -2.36659 | -2.2 V |
| Ion/Ioff | $3.545\times10^3$ | $3.8\times10^3$ |
| Sub threshold slope (S.S) | 1.15005 | 1.3 V/dec. |
| Transconductance ($g_m$) | 0.1432 | 0.12 µS |

Table 5: Simulated electrical parameters of dual gate OTFT

## VIII. Comparison of Single and Dual Gate Parameters

Simulated electrical parameters of single gate OTFT and dual gate OTFT has been given in table 6. As we can see from the table single gate OTFT has mobility 0.02 $cm^2$/V.S whereas dual gate OTFT has mobility 0.1$cm^2$/V.S. and threshold voltage for single gate and dual gate OTFTs is -2.0V and -2.2V, respectively. Transconductance value for single gate is less then dual gate OTFT i.e., 0.04 µS and 0.12 µS. Hence when dual gate OTFTs compared to single gate OTFTs, the dual gate organic TFTs have many benefits that include improvement in mobility ($\mu$), current on–off ratio *(Ion/Ioff)* and transconductance (*gm*). It also exhibits steeper sub-threshold slope (*SS*) and better control of threshold voltage (*Vt*).

| Parameters | SG-OTFT | | DG-OTFT | |
|---|---|---|---|---|
| | Simulated | Experimental | Simulated | Experimental |
| µ ($cm^2$/V s) | 0.0241708 | 0.02 | 0.157672 | 0.1 |
| Vt (V) | -2.77399 | -2.0 | -2.36659 | -2.2 |
| Ion/Ioff | $3.223\times10^3$ | $3.2\times10^3$ | $3.545\times10^3$ | $3.8\times10^3$ |
| SS (V/dec.) | 2.33328 | 2.0 | 1.15005 | 1.3 |
| gm (µS) | 0.03954 | 0.044 | 0.1432 | 0.12 |

Table 3.6: comparison of single gate and dual gate OTFT simulated electrical parameters.

## IX. Conclusion

This paper described the single gate and dual gate OTFT with its working principle, structure, and characteristics. Additionally, both single gate and dual gate OTFT analysed using its simulation results and make a comparison that dual gate OTFT has superior performance over single gate OTFT in terms of mobility, current on–off ratio, transconductance, sub-threshold slope and threshold voltage.

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