A High Performance Current Mirror using Dual Gate Organic Thin Film Transistor

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Abstract— OTFT is a key element for building electronic circuits on a low cost flexible substrate. In OTFT, Dual gate structure is a promising method to improve the device performance. As p type OTFT is better than n type OTFT, p type dual gate structure is used in this work. In this paper we propose a current mirror using dual gate thin film transistor with excellent characteristics.

Key words: OTFT, Dual Gate, Current Mirror, Flexible Substrate

I. Introduction

Now days, organic electronics have a huge concentration from both industrial and academic research because of the great improvement in the performances of organic materials when used in Organic Thin Film Transistors (OTFTs), in solar cells, in Organic Light Emitting Diodes (OLED), etc. On the other hand, unusual properties such as flexibility, light weight, and disposability give a new era of devices and applications based on the development of Post Silicon Technologies. Accordingly in the last decades for the improvement of materials properties and devices processing many efforts has been done. To obtain appropriate features of electronic applications, Organic materials have been modified, as for example improved lifetime, environmental stability, solution processability, and reasonable charge mobility. The most important module of the organic electronics is organic thin film transistor (OTFT) that is basically a field effect transistor (FET) uses organic semiconductors and organic dielectrics. OTFTs have many advantage as, it can be realize on flexible substrates at room temperature, low cost, mechanically flexible, and large area electronics applications. These properties of OTFT allow it for their use in different merging application fields, such as in electronic paper or in flexible displays [1], in sensors [2], and in low-cost radiofrequency identification cards (RFIDs) [3, 4]. The limitation of organic material is low mobility due to this where is fast response (ns) speed and low size (nm) are required in electronic applications they are not allowed , but some application where slow responses of OTFT are accepted: for example smart tag, displays, photovoltaic, radio-frequency identification (RFID) circuitry, and chemical sensor OFETs are normally P type transistors although N type OFETs have been reported during the last years [5, 6], but N type OTFTs suffer from low carrier mobility then P type OTFTs, process complexity, and stability problems. The pantacene based OTFTs have the superior performances as high field effect mobility and large on/off current ratio. Other issues of the practical OTFTs that should be improved are the improvement of passivation performance and the control of electrical parameters such as threshold voltage (V_{th}) and on-current. These problems can be solved using dual-gate OTFT structure and it has different bias configuration and offers higher flexibility. So in this work a current mirror is implemented using dual gate OTFT. For simulation of dual-gate OTFT and OTA industry standard Atlas (Silvaco) 2-D device simulator is used. In Section II, an overview of current mirror is given. In Section III, configuration of current mirror and its implementation is given. in Section IV, simulation results of current mirror are discussed in detail. Finally, in Section V, the conclusions of this work are given.

II. Current Mirror

In analog integrated circuits, Current mirrors using active devices are extensively used as load devices and also as biasing elements for the amplifier stages. The current mirrors used widely for biasing in analog circuits because its performance is insensitive to variations in power supple and temperature variations. Furthermore current mirrors are favoured for small bias current requirements over resistors because they are more reasonable in terms of die area. At low power-supply voltages the high resistance of the current mirror results in high voltage gain. These apart in analog design the current mirrors and current sources also have other applications. An electronic circuit designed to regulate and control the current through one active device depending on the current through another active device is called current mirror. It keeps the output current constant irrespective of the output load. The controlling current or the current depending on the value of which the output current is determined is often a varying signal current. Basically, an ideal current mirror can also be considered as an ideal current amplifier. In analog circuits to provide bias currents and active loads current mirrors are used. A current mirror is characterized by three main specifications, the current level it produces, the AC output resistance and the minimum voltage. The AC output resistance determines how much the output current varies with the applied voltage of the mirror and the minimum voltage needs to be maintained across the output terminal of the current mirror for it to work properly. In current mirror at the output transistor minimum voltage to be applied that keeps transistor in active mode and then dictates the voltage specification. So the compliance range is the voltage range in which the current mirror works and the compliance voltage is the voltage beyond which the current mirror performance is no longer satisfactory. Temperature stability is the secondary performance issues with current mirrors also dictate the design procedure. An ideal current mirror has the output current which is a product of a desired voltage gain and the input current. In unity gain current mirror the input current to be copied at the output. Ideally the output current of current mirror should be independent of the voltage at the output node and the current mirror gain should be independent of input current frequency. Actually the real current mirrors experience many deviations from the ideal behaviour of current mirror. For example neither does the gain independent of the input frequency nor is the current mirror output current stays independent of voltage variations at the output node.

A. Output Resistance

Practical current mirrors have finite output resistance unlike the ideal current that depends on the channel length modulation of the transistors of the output stage:

$$R_N = r_0 = \frac{1/\lambda + V_{DS}}{I_D} \qquad (2.1)$$

Where, λ and V_{DS} is the channel-length modulation index and the drain-to-source voltage, respectively.

B. Compliance Voltage

When analyzing the current mirror working we assumed that the both transistors are operating in saturation, so for the current mirror to behave correctly required minimum output voltage is determined by the minimum drain to source voltage that needs to be applied to the output stage transistors to keep them in saturation. As the drain and gate terminals of the transistor M_1 connected together this forces transistor M_1 to operate in the saturation mode in this current mirror circuit if ID ≠ 0. In this mode

$$I_{D1} = \frac{1}{2}K_{P1}\left(\frac{W_1}{L_1}\right)(V_{GS} - V_{t1})^2 \qquad (2.2)$$

When gate current is zero, then $I_{REF} = I_{D1}$ and we can see easily from the circuit that

$$I_{REF} = (V_{DD} - V_{GS} - (-V_{SS}))/R_{REF} \qquad (2.3)$$

Now we assume that in the circuit both MOSFETS have the same V_{GS} and the drain of both transistors are connected to their gates and their sources are connected to the V_{DD}.

As a result the drain current of second transistor is

$$I_{D2} = \frac{1}{2}K_{P2}\left(\frac{W_2}{L_2}\right)(V_{GS} - V_{t2})^2 \qquad (2.4)$$

If these two transistors are matched perfectly then $K_{P1} = Kp_2$ and $Vt_1 = Vt_2$ so that by comparing the above equations we obtain

$$I_{D2} = ((W_2/L_2)/(W_1/L_1))I_{D1}$$
$$= ((W_2/L_2)/(W_1/L_1))I_{REF} \qquad (2.5)$$

In this PMOS current mirror, M_2 acts as a current source as it pushes current $I_0 = I_{D2}$ into the load.

III. Current Mirror Configuration and Implementation

Implementation of the basic current mirror using pmos transistors is as shown in Figure 1. We assume that both transistors M_1 and M_2 operate in saturation or active region for the proper functioning of the device in the figure 4.1.

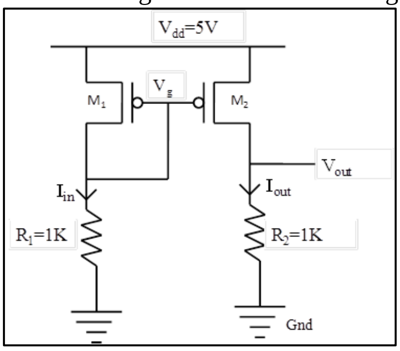

Fig. 1: Schematic of basic current mirror.

In this current mirror circuit, there is a direct relation between I_{REF} and I_{OUT}, the drain current I_D of a MOSFET is determined by the voltage across the gate and source terminals and also the drain-to-gate voltage of the MOSFET. Thus, the drain current is a function of V_{GS}, V_{DG} and can be given by $I_D = f(V_{GS}, V_{DG})$. Functionality of the MOSFET device derived this relationship. The drain-to-source voltage is expressed as, $V_{DS} = V_{GS} + V_{DG}$, with this substitution, it is an approximate form of function $f(V_{GS}, V_{DG})$,

$$I_D = f(V_{GS}, V_{DS}) = \frac{1}{2}K_P\left(\frac{W}{L}\right)(V_{GS} - V_{th})2(1 + \lambda V_{DS})$$
$$= \frac{1}{2}K_P\left(\frac{W}{L}\right)(V_{GS} - V_{th})2(1 + \lambda(V_{DS} + V_{GS})) \qquad (3.1)$$

Here Kp depends on the technology of fabrication of transistors, W/L defines the ratio of width to length of the transistor, V_{GS} defines the gate-source voltage, V_{th} defines the threshold voltage, V_{DS} defines the drain source voltage respectively, and λ is the transistor's channel length modulation constant.

Now in mirror circuit $I_D = I_{REF}$ for the transistor M_1 and the reference current I_{REF} is a well-known current of constant value independent of supply voltage variations. To provide this constant reference current use a resistor as shown or even can be used a "self-biased" or "threshold-referenced" current source. Now to provide this constant reference current the drain and gate is shorted. For $M1$ transistor $V_{DG}=0$, thus the function for the drain current of transistor M_1 can be given by $I_D = f(V_{GS}, V_{DG}=0)$, therefore I_{REF} depends only on the gate to source voltage and so the value of V_{GS} determined by the I_{REF} current. when, $V_{DG}=0$ and the same V_{GS} is applied to transistor M_2 and if M_1 and M_2 are matched means they have identical channel length, width, threshold voltage *etc*, then the output current I_{OUT} depends only on V_{GS} and therefore $I_{OUT} = I_{REF}$ current; i.e. the output current equals to the reference current of a current mirror when for the output transistor $V_{DG}=0$, and both transistors are matched with identical *W/L*.

IV. Simulation Results of Current Mirror

DC analysis of the current mirror circuit is shown in Figure 2. The DC analysis shows that, the drain current of M_2 is a replica of drain current of M_1 means output current is equals to reference current which confirms the proposed current mirror copying the accurate current.

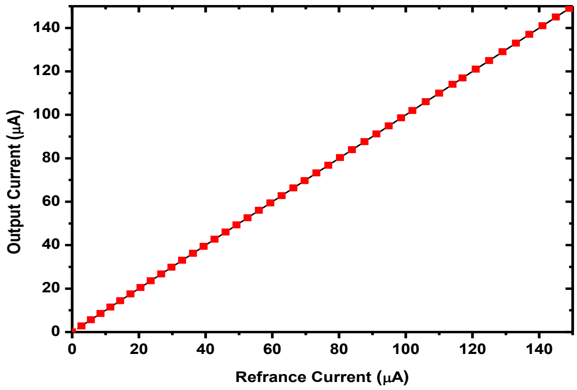

Fig. 2: DC Analysis of Current Mirror Circuit.

V. Conclusion

This chapter described the basic current mirror with basic working principle and simulation results. From simulation result of current mirror we observe that output current copying the reference current.

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