Design of High Speed 32-bit Single Precision Floating Point Complex Multiplier using Vedic Mathematics

Miss Ashwini B. Kewate[1] Prof. P. R. Indurkar[2] Prof. A .W. Hinganikar[3]
[1]P.G. Student [2]Associate Professor [3]Assistant Professor
[1,2,3]Department of Electronics & Telecommunication Engineering
[1,2,3]B.D.C.E. Sevagram, India

Abstract— This paper describes the design of 32-bit single precision floating point complex multiplier using Vedic mathematics. Multipliers are key components of many high performance systems such as microprocessors, FIR filters, digital signal processors, etc. Performance of a system is generally determined by the performance of the multiplier. Complex number operations are the backbone of many digital signal processing algorithms, which mostly depend on extensive number of multiplications. Complex multiplication is of immense importance in Digital Signal Processing (DSP) and Image Processing (IP). The IEEE 754 standard provides the format for representation of Binary Floating point numbers in computers. The Binary Floating point numbers are represented in Single and Double formats. Vedic mathematics is the Indian system of mathematics which is mainly based on 16 Sutras. The "Urdhva Tiryagbhyam" sutra is used for the design. 32-bit adder, sub-tractor, 24bit Vedic multiplier and 32 bit floating point complex multiplier are designed. All the modules in the design are coded in VHDL Finally. Simulation of the design is done in XILINX 14.5i ISE Simulator.

Key words: Complex Multiplier, Vedic Mathematics, IEEE 754 Single Precision Standard Format Urdhva Tiryagbhyam

I. INTRODUCTION

The fundamental and the core of all the digital signal processors (DSPs) are its multipliers, and the speed of the DSPs is mainly determined by the speed of its multiplier. Complex multipliers are essential component of electronics device. Complex number multiplication is performed using four real number multiplications and two additions/ subtractions. In real number processing, carry needs to be propagated from the least significant bit (LSB) to the most significant bit (MSB) when binary partial products are added. Therefore, the addition and subtraction after binary multiplications limit the overall speed. Furthermore, multiplier is generally the most area consuming. Hence, optimizing the area and speed of the multiplier is a major design issue. However, speed and area are usually conflicting constraints so that improving speed results mostly in larger areas.

Multipliers can be used for multiplication of fixed point integer, floating point number and floating point complex numbers. The performance of any processor depends upon its power dissipation and delay, so there is always the need of high speed multipliers and the performance of any floating point multiplier depends upon the performance of mantissa calculation unit. Nowadays, almost every language has a floating point data type, computers from PCs to supercomputers have floating point compilers and every operating system must respond to floating point exceptions. The major application areas of floating point numbers today are in the field of medical applications, image processing, motion sensing, scientific computing, audio applications, DSP applications etc.

A. The IEEE 754 Standard Format

The IEEE 754 standard provides the format for representation of Binary Floating point numbers in computers. The Binary Floating point numbers are represented in Single and Double formats. Following figure shows IEEE Format for single and double precision bit.

Sign	Exponent	Mantissa
1 bit	8 Bit	23 Bit

Fig. 1: IEEE Format for 32 bit single precision standard

In the Single Precision format it contains 32 bits in that 1 bit is sign bit, 8 bit is exponent bit and 23 bit is mantissa bit. The sign bit is used for showing result whether number is positive or negative. If sign bit contains 1 then result is negative and if it contains 0 then result is positive. Exponent bit is of 8 bit and it used for the normalization. The mantissa bit is of 23 bit and it is used for the addition.

B. Vedic Mathematics

Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in early twentieth century. The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Swami Bharati Krishna Tirthaji, (1884-1960). Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc.

The Vedic mathematics approach is totally different and considered very close to the way a human mind works. Vedic Mathematics is easier to understand as compared to modern mathematics. Vedic Mathematics performs basic as well as complex mathematical calculations.

C. Urdhava Tiryakbhyam Sutra

The designed Vedic multiplier is based on the "Urdhva Tiryagbhyam" sutra (algorithm). The basic meaning of Sanskrit word Urdhva–Triyakbyham Sutra is "Vertically and crosswise". The vertical and crosswise multiplication can be implemented starting either from left hand side or from right hand side. Significance of vertically is straight above multiplication and significance of crosswise is diagonal multiplication and add them. Thus any multi-bit multiplication can be reduced down to single bit multiplication and addition using this method.

II. LITERATURE REVIEW

Laxman P. Thakare et.al [1] designed complex number multiplier using Urdhva Tiryakbhyam sutra which has been implemented using VHDL. The complete code is

synthesized using Xilinx synthesis tool (XST). The Vedic sutra ''Urdhva Tiryakbhyam'' is used for the implementation of complex number multiplier. The Urdhva Tiryakbhyam sutra (method) was selected for implementation since it is applicable to all cases of multiplication. The use of Vedic multiplier will increase the speed of system. The implementation of complex number multiplier using Gauss's multiplication equations, and Urdhva Tiryakbhyam sutra of Vedic mathematics. The delay obtained by 32 bit complex multiplier is 40.250ns.

Rajashri Bhongade S. G. Mungale Karuna Bogavar et.al. [2] presents s report on Performance Evaluation of High Speed Complex Multiplier Using Vedic Mathematics. In this design technique vedic mathematics used. The multiplication is done using

Urdhva Tiryakbhyam. The coding is done for complex multiplier using VHDL and synthesized using Xilinx ISE version 9.1i. The delay required for this complex multiplier using the Vedic Mathematics was found to be 40.25ns.

Deepak Kurmi1, V. B. Baru et.al [3] design a High Speed 32 Bit Multiplier Architecture Using Vedic Mathematics and Compressors. Xilinx 14.5 tool has been used for the simulation. In this multiplier architecture design 4:2 and 7:2 compressor has been used. The delay obtained for multiplier using Vedic Mathematics is found to be 44.294ns.

Ankush Nikam et.al [4] presents Design and Implementation of 32bit Complex Multiplier using Vedic Algorithm. Vedic mathematics helps to reduce the complexity in calculations that exist in conventional mathematics. Hence, for the designing of this multiplier they used a Vedic mathematics technique. Urdhava Tiryakbhyam sutra is used for the designed and this multiplier is implemented using VHDL. The delay obtained for this multiplier is 29.84 ns and 62 mw powers is required. They required 7874 number of slice LUT's and 258 numbers of IOB's.

III. DESIGN OF COMPLEX MULTIPLIER

For designing of floating point complex multiplier adder, sub-tractor and floating point vedic multiplier are required. These combine three modules are the essential for the design of complex multiplier. For the complex number multiplier design, the most important procedure is mantissa calculation As the performance of floating point complex multiplier is depend upon mantissa calculation unit. Here we have designed the 32 bit floating point complex multiplier. Fig.3 shows the block diagram of 32 bit floating point complex multiplier module which is easily designed using four 32 bit floating point vedic multipliers modules.

Suppose the two 32bit numbers are X_r [31:0] and X_i [31:0] and Y_r [31:0] and Y_i [31:0] are taken for the multiplication of real number X_r and real number of Y_r is done. In the second step of multiplication of imaginary number X_i and imaginary number of Y_i is done. In the next step multiplication of real number X_r and imaginary number of Y_i is done. and in the last step multiplication of imaginary number X_i and imaginary number of Y_i is done respectively. And finally Z_r and Z_i gives the output of two complex number multiplication.

A. Example of 32 Bit Multiplier

For the 32 bit single precision IEEE 754 format the Mantissa Calculation Unit requires a 24 bit multiplier. In this paper we propose the Multiplication of two, 32 bit floating point number. These numbers are as follows in that X_{am} is the first real number and X_{bm} is the first imaginary number. Similarly Y_{am} is the second real number and Y_{bm} is the second imaginary number.

$$Z = X * Y$$

Where,

$$X = X_{am} + j\ X_{bm}$$
$$Y = Y_{am} + j\ Y_{bm}$$
$$X = (2.1 + j\ 3.1)_{10}$$
$$Y = (2.2 + j\ 3.2)_{10}$$

The 32 bit IEEE format for these two number are as follows.

X_{am}=01000000000001100110011001100110
X_{bm}=01000000010001100110011001100110
Y_{am}=01000000000001100110011001101101
Y_{bm}=01000000010011001100110011001101

The result obtained by multiplication of these two numbers is given by,

$$Z = Z_{am} + j\ Z_{bm} = -5.3 + j\ 13.54$$

Z_{am} =11000000101010011001100110011000
Z_{bm} =01000001010110001010001111010110

B. 32 Bit Floating Point Complex Multiplier

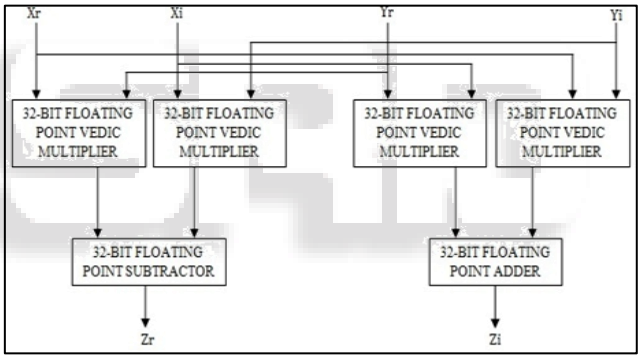

Fig. 2: Block Diagram of 32 Bit Floating Point Complex Multiplier

IV. EXPERIMENTAL RESULTS

A. RTL View

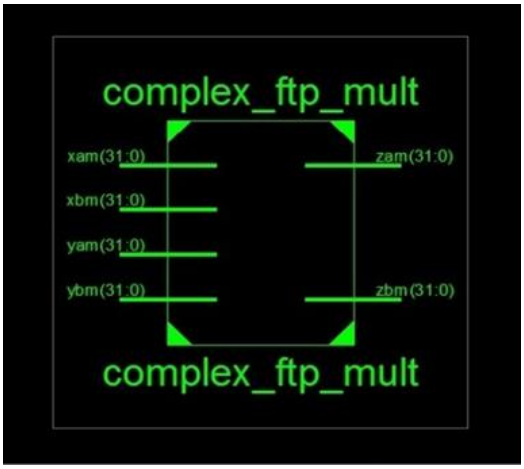

Fig. 3: RTL View of 32 Bit Floating Point Complex Multiplier

B. Technology Schematic

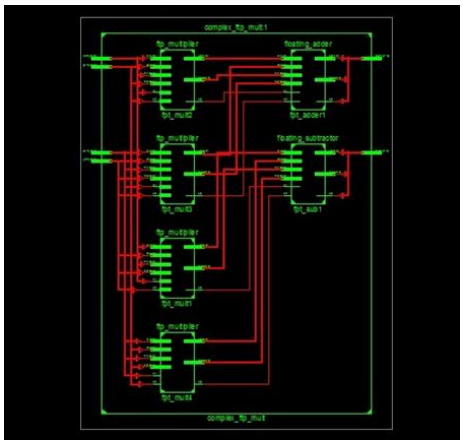

Fig. 4: RTL View of 32 Bit Floating Point Complex Multiplier

Figure 4 shows the RTL (Register Transfer Logic) view of 32 bit floating point complex multiplier. In that it consists of two floating point complex number. The real part consists of X_{am} and X_{bm} number and imaginary part consist of Y_{am} and Y_{bm}.

C. Simulation Results

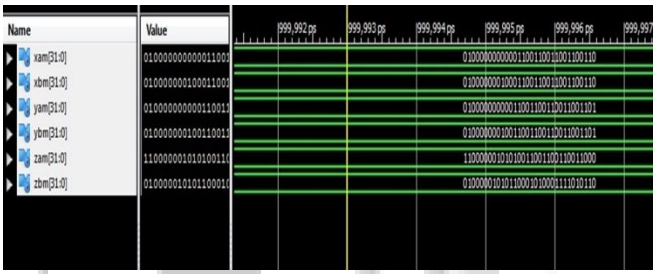

Fig. 5: Simulation Result of 32 Bit Floating Point Complex Multiplier

Figure 5 shows the simulation result of 32 bit floating point complex multiplier. In that multiplication of two floating complex number is performed and result is separately stored in Zam and Zbm.

The following tables shows the device utilization of 32 bit complex multiplier, bit performance of 32 bit complex multiplier, comparison of 32 bit complex multiplier and experimental results of 32 bit complex multiplier.

Parameters	Proposed Design
Delay (ns)	25.418
Power (mw)	143
No. of Slice LUTs	4408
No. of bonded IOBs	192
Input voltage (v)	1.0
Junction temperature (c)	25.02
Ambient temperature (c)	84.8
Frequency (MHz)	39.34

Table 1: Device Utilization Of 32 Bit Complex Multiplier

Complex Multiplier 32Bit	Parameters	
Modules Design	Power(mw)	Delay(ns)
Adder	143	12.064
Sub-Tractor	143	14.633
24 Bit Floating Point Vedic Multiplier	143	56.44
Floating Point Multiplier	143	18.623
Complex Multiplier	143	25.418

Table 2: 32 Bit Performance of 32 Bit Complex Multiplier

Complex Multiplier	[1]	[2]	[3]	[4]	Proposed Multiplier
Technology	Vedic maths	Vedic maths	Vedic maths	Vedic algorithm	Vedic maths
Delay (ns)	40.25	40.25	44.249	29.84	25.418
Power	-	-	-	62mw	143mw
No. Slice of LUTS	2038	2038	-	7874	4408
No. of Bonded IOBs	128	128	-	258	192

Table 3: Comparison of 32 Bit Complex Multiplier

Sr. No.	Inputs		Outputs	
	Real	Imaginary	Real	Imaginary
1.	$X_{am}=(2.1)_{10}$ $Y_{am}=(2.2)_{10}$	$X_{bm}=(3.1j)_{10}$ $Y_{bm}=(3.2j)_{10}$	$Z_{am}=(-5.3)_{10}$	$Z_{bm}=(13.54j)_{10}$
2.	$X_{am}=(2.1)_{10}$ $Y_{am}=(2.2)_{10}$	$X_{bm}=(-3.1j)_{10}$ $Y_{bm}=(-3.2j)_{10}$	$Z_{am}=(-5.3)_{10}$	$Z_{bm}=(13.54j)_{10}$
3.	$X_{am}=(-2.1)_{10}$ $Y_{am}=(-2.2)_{10}$	$X_{bm}=(3.1j)_{10}$ $Y_{bm}=(3.2j)_{10}$	$Z_{am}=(-5.3)_{10}$	$Z_{bm}=(13.54j)_{10}$

Table 4: Experimental Results of 32 Bit Complex Multiplier

V. Conclusion

This paper presents the design of 32 bit floating point complex multiplier using a VHDL. The design is synthesized using Xilinx ISE 14.5 tool targeting the Xilinx Virtex7. A test bench is used for the generation of stimulus result and the 32 bit floating point complex multipliers operation is verified. The 32Bit floating point complex multiplier has delay of 25.418 ns.

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