Design and Analysis of a High Performance-Low Power Conditional Discharge Flip Flop using 90 nm CMOS Technology

Sonam Parihar[1] Rachana Arya[2]
[1]P.G. Student [2]Assistant Professor
[2]Department of Electronic & Communication Engineering
[1,2]Bipin Tripathi Kumaon Institute of Technology, Dwarahat, Almora, Uttarakhand

Abstract— Low power flip-flops are crucial for the design of low-power digital systems. In this paper, a novel low-power high performance pulse-triggered flip-flop using Modified (proposed) conditional discharging flip-flop (MCDFF) circuit is presented. It is based on the conditional discharging technology. The modified design reduces the number of transistor and achieves better speed and power performance other flip flop (ep-CDO, CDFF, SCDFF, MHLFF). All the simulation results, based on 90-nm CMOS technology, reveal that the proposed design features the best power-delay-product performance. Here, a comparison of existing Flip-Flop (FF) system with different parameters is presented.

Key words: CMOS circuits, low power, flip-flops, power consumption

I. INTRODUCTION

The demand of high performance and low-power is getting higher and higher, due to the explosive growth of multimedia application. In the past few years the transistor densities is continuously increasing which in turn constantly increases the power consumption of the chip. The clock system is the most power consuming components in a very large scale integration system. About 30-60% of the total chip power is consumed by the clock system [1].

Flip-flop choice and design has a great effect both in reducing power dissipation and in high performance system. In high-speed operations, pulse-triggered has been considered a alternative to the conventional master-slave flip-flop. Its circuit simplicity is also beneficial in lowering the power consumption of the system. A Pulse triggered flip flop consists of pulse generator and a latch [2] ,[3].

A universal flip-flop with the best performance, low power consumption, and highest robustness against noise would be an ideal component. A set of different flip-flops latches and with different performances are essential to limit the use of more power consuming and noise-sensitive elements. The factors which are desirable in latches and flip-flops are:

1) High speed
2) Low power consumption
3) Robustness and noise stability
4) Small area and less number of transistors
5) Supply voltage capability of a system
6) Low glitch
7) Insensitivity to clock edge
8) Less internal activity when data activity is low

The designer while choosing a structure for flip-flops has to consider all these parameters according to the requirements of the system.

II. CONVENTIONAL FLIP FLOP DESIGN

P-FF designs can be either implicit or explicit depending on the method of pulse generation. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, we have separate the designs of pulse generator and latch. Implicit pulse generation is often considered to be more power efficient as compared to explicit pulse generation. This is because implicit just controls the discharging path while explicit needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design due to which they have inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional precharge, conditional capture, conditional discharge, or conditional data mapping are applied. Explicit-type P-FF designs face a similar pulse width control issue, but in the presence of a large capacitive load the problem is further complicated, e.g., when one pulse generator is shared among several latches.

Here few existing design are discussed for the purpose of comparison.

A. EP-DCO: Explicit Pulse Data Close To Output

Fig.1.show a classic explicit data close to output (ep-DCO). Its latch design is a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured. In this P-FF design, data latching is done with the help of inverters I3 and I4 and inverters I1 and I2 are used to hold the internal node X. The delay of three inverters determines the pulse width. The drawback of this design is that on every rising edge of the clock pulse the internal node X is discharged in spite of the presence of a static input "1." Due to this large switching power is dissipated. To overcome this problem, many techniques such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed [2].

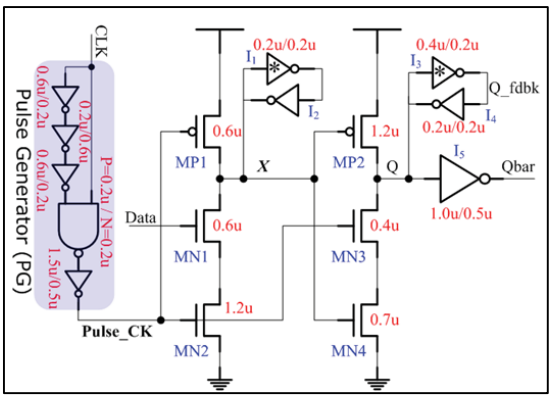

Fig. 1: EP-DCO

B. CDFF: Conditional Discharge Flip Flop

Fig.2. shows a conditional discharged (CD) technique [3]. Similar to ep-DCO, the CDFF structure is also the semi-dynamic structure [4]. The first stage is dynamic and the second stage is static. The advantage of this design is that it eliminates the extra switching activity by controlling the discharge path. An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1". The logic at internal node X is simplified and consists of only an inverter and a pull up pMOS transistor [2].

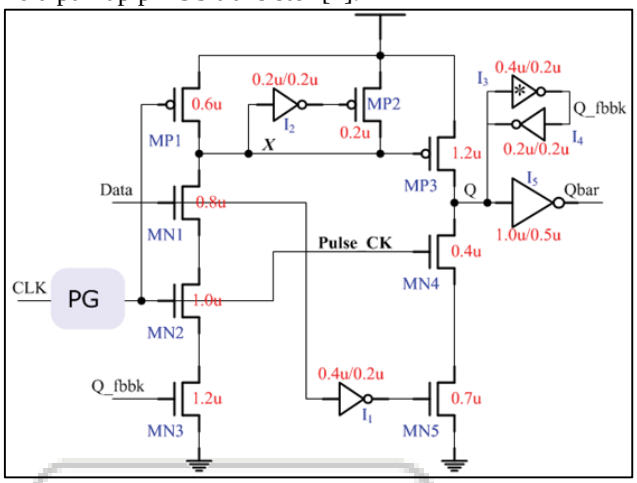

Fig. 2: CDFF

C. SCDFF: Static Conditional Discharge Flip Flop

SCDFF and CDFF are almost similar, the difference is only in their latching structure. Fig.3. shows almost similar to CDFF but with changed position of static latch and node X having keeper logic as two back-to back end inverters. Here node X is not periodically precharge and it also exhibit longer D to Q delay. The problem with both design is the three stacked transistor in the discharging path i.e MN1-MN3 [7].

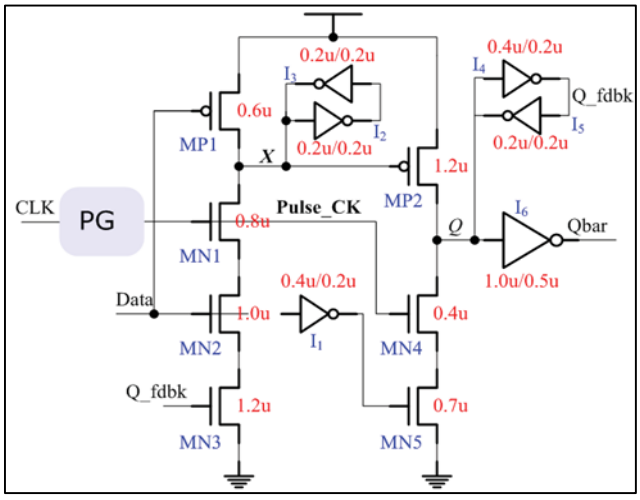

Fig. 3: SCDFF

D. MHLFF: Modified Hybrid Latch Flip Flop

To overcome this delay MHLFF is introduced. MHLFF also uses static latch. The keeper logic at X is removed. But the drawback with this is that X floating in certain cases and its value may drift causing extra dc power [5].

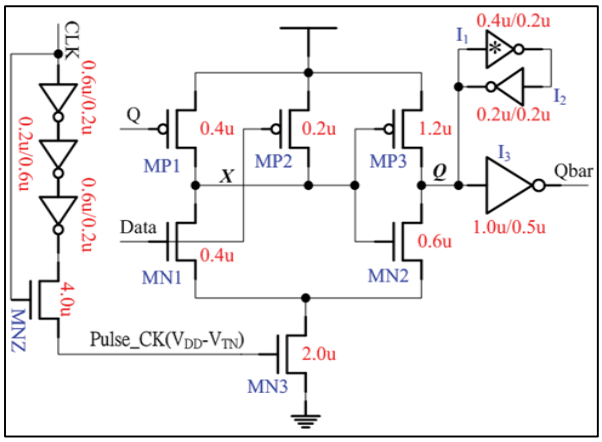

Fig. 4: MHLFF

III. PROPOSED FLIP FLOP DESIGN

In this brief a high performance low-power flip-flop (FF) design is proposed. In the four circuits discussed in above section, we observed that they all exhibit a longer data-to-Q (D-to-Q) delay. These designs have large power dissipation as well as large layout area. The proposed design employs a latch structure almost similar to CDFF. However, there are three major differences that make the proposed design distinct from the above discussed flip flops. First, the simplicity of pulse-generation circuitry. Here the count of transistor reduces and hence the layout area. Second, inverter in second stage of the pull-down network is completely removed. Third, the nMOS transistor is removed from the discharging path.

Compared with the latch structure of CDFF design, the proposed circuit design saves a control inverter and a nMOS from the discharge path. The proposed design have reduced count of transistor, less power consumption and hence less power-delay product as compared to other P-FF designs such as ep-DCO, CDFF, MHLFF and SCDFF.

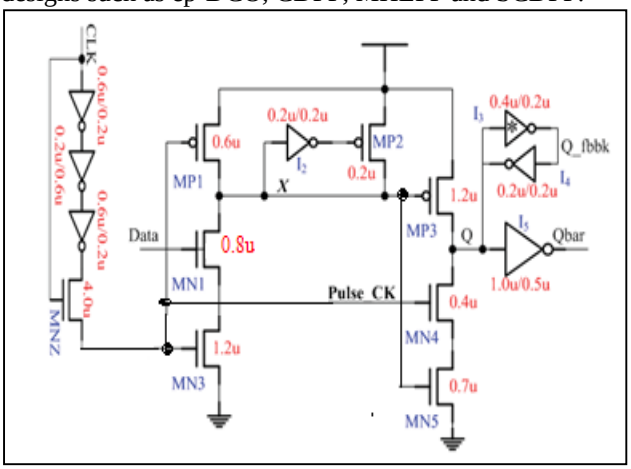

Fig. 5: Proposed P-FF Design

IV. PERFORMANCE ANALYSIS AND SIMULATION RESULTS

The comparison of result summarizes some important performance indexes of the above discussed P-FF designs. The simulation results for all the flip flop were obtained by using 90nm.

CMOS technology at room temperature using Tanner Tool 13, the supply voltage is 1.8V. Comparison table shows the simulation results of various flip flops. In

view of power consumption and PDP, proposed flip flop has least value as compare to other flip flop.

Flip Flop	No. of Transistor	Propagation Delay of Q (n)	Propagation Delay of QBAR (n)	Power Consumption (f)	PDP of Q (n*f)	PDP of (n*f)QBAR
Ep-DCO	28	22.516	13.526	31.1	699.75	420.47
CDFF	30	22.511	13.514	12.37	278.46	167.16
Static-CDFF	31	22.512	13.51	13.79	308.25	185.087
MHLFF	19	22.5	22.47	49.8	1120.50	1268.406
Proposed MCDFF	22	10.6117	10.51	4.5296	48.067	47.6061

Table 1: Feature Comparison of Various FF Design

A. Propagation Delay

The propagation delay of a gate is way to describe how quickly it responses to input. For inverter, it is measured between the 50% transition points of the input and output waveforms. Because the gate displays different response times for rising or falling input waveforms, so there are two other definitions related to the propagation delay,t_{PHL} and t_{PLH}. The overall propagation delay is the average of t_{PLH} and t_{PHL} , where t_{PLH} defines the time of the output from low to high and t_{PHL} defines the time of the output from high to low:

$$\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

For sequential circuits, propagation delay time is the time between the clock signal and the output signal with the corresponding wave edges, so it is called clock-to-output as well. The measurements of low to high transitions and high to low transitions are between 50% of the transition points of the waveforms. But they are different, so we choose the maximum value between them, which means:

$$t_{clock-to-output} = max(t_{clock-to-output\ LH}, t_{clock-to-output\ HL})$$

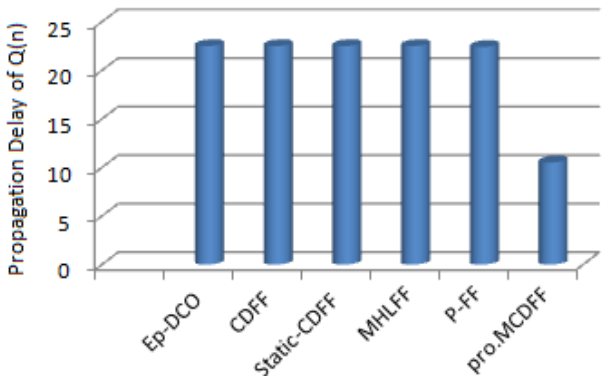

Fig. 6: Propagation Delay of Q (n)

B. Power Consumption

There are three power dissipations of a flip-flop mentioned in this paper:

- Internal Power dissipation: it concludes the power consumed by the flip-flop and the powered used by driving the output load.
- Local data Power dissipation: concludes the power consumed by driving the data input of the flip-flop.
- Local clock Power dissipation: concludes the power consumed by driving the clock input of the flip-flop.
- The total power consumption is got from adding these three power dissipations,

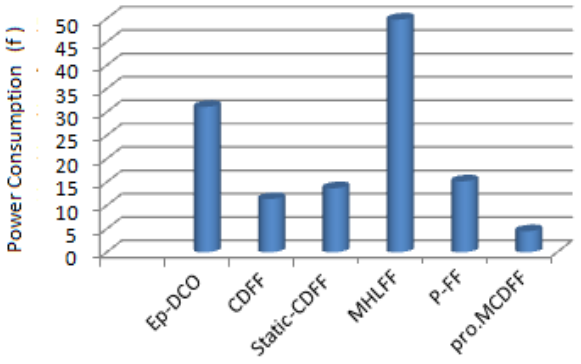

Fig. 3: Power Consumption (f)

C. Propagation Delay

The propagation delay time is related to the power consumption, since it is always used to measure the speed of the response from the changes of inputs to the outputs. The gate capacities can store the energy when the change happens. The faster the state changes, the higher the power consumed, so power-delay product can be used to measure the devices with switching properties.

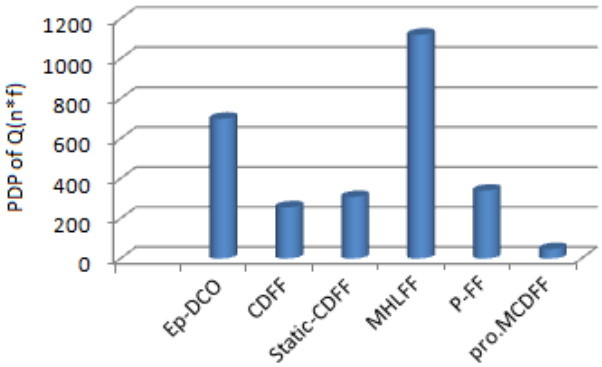

Fig. 4: PDP of Q (n*f)

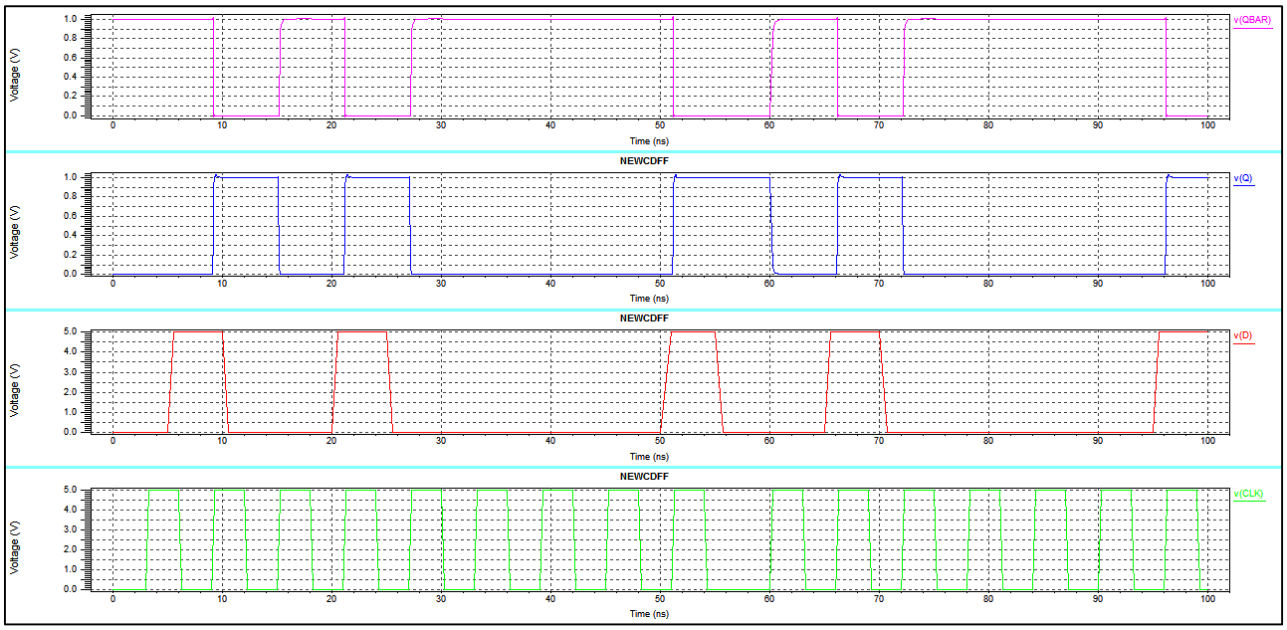

Fig. 9: Waveform of modified (proposed) Flip Flop

V. CONCLUSION

In this paper, a high performance low-power flip-flop (FF) design is proposed (Modified). The proposed design reduces the count of transistor and achieves better speed and power performance. The quality and performance of a CMOS process and gate design is measured in terms of power-delay product. The power-delay product can be interpreted as the average energy required for a gate to switch its output from low to high and from high to low. The simulation is performed in 90nm technology CMOS technology, using power supply of 1.8V and clock frequency of 250MHz. Simulation results indicate that the modified design is better in performance indexes such as power, D-to-Q delay, and PDP. In view of power consumption and PDP, Simulation results indicate that the modified design has least value as compare to other flip flop.

REFERENCES

[1] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 807–811, May 1998

[2] Jin-Fa Lin, "Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme" IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 22, No. 1, January 2014.

[3] P. Zhao, T. Darwish, M. Bayoumi ,"High-performance and low power conditional discharge flip-flop", IEEE Trans. Very Large Scale Integration. (VLSI) Syst., Vol. 12, No. 5, pp. 477–484, May 2004.

[4] J.Tschanz, S.Narendra, Z. Chan, S.Borkar, M.Sachdev and V.De, "Comparative Delay and Energy of Single Edge-Triggered & Dual Edge-Triggered Pulsed Flip-Flops for High-Performance Microprocessors", in Proc. ISPLED, 2001, pp. 207-212.

[5] Y.-T. Hwang, J.-F. Lin, and M.-H. Sheu, "Low power pulsetriggered flip-flop design with conditional pulse enhancement scheme," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 2, pp. 361–366, Feb. 2012

[6] Shashank Uniyal, Rajeev kumar, Krishna Chandra, Vishal Ramola, " Low Power explicit type pulse-triggered flip flop design at minimum transistor" IJEDR, vol 3, Issue 2, 2015.

[7] M.-W. Phyu, W.-L. Goh, and K.-S. Yeo, "A low-power static dual edge triggered flip-flop using an output-controlled discharge configuration," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 2429–2432.

