Design and Implementation of Multisoft Core Architecture for Image Processing Application

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Abstract— To achieve the high performance of multimedia applications, multiple processing units are required which are integrated into embedded systems. Field programmable gate arrays (FPGAs) and Soft core processors are best option to develop systems. For implementation of multi core system various platforms are available, but still performance of the system is not that much of efficient. This paper describes a design methodology to implement multi soft core architecture using microblaze processor on virtex 6 FPGA and implementation of median filter on multi soft core architecture which gives a better performance in terms of fast processing.

Key words: Microblaze soft core processor, median filter, FPGA

I. INTRODUCTION

Digital image processing is a wide area with tremendous applications including our day to day life such as image authentications, automated control equipments, military surveillance, automated industry inspections etc. Images captured form image sensors are affected by several types of noises know as Impulse noise or Salt and Pepper noise causes due to errors in data transmissions, to remove this type of noise Median filter is used because it preserve edge information. A median filter operates on each pixel in an image therefore it is easy to filter out damaged pixels in an image. Median filter implementation is complex because of large amount of dada involved in it. Capability of single core processor is not much efficient to process an image. Therefore to achieve a better performance in terms of fastest speed multi soft core architecture is designed and implemented on reconfigurable platform ,in this paper microblaze processor is adopted ,system is connected using AXI bus and to achieve synchronization between two cores xps_mailbox and xps_mutex cores are adopted to design a multi soft core architecture.

II. SOFT CORE PROCESSOR

Soft core processor is an IP core synthesized for both ASIC and FPGA as per application requirements, advantages of soft core processors are easier to understand, designer can change core by simply editing source code. In past years systems have been built using general-purpose processors implemented as Application Specific Integrated Circuits (ASIC), placed on printed circuit boards Application specific integrated circuits are designed to perform a specific application. They perform very efficiently and fast while executing a given computation, also circuit cannot be modified after its fabrication, if any parts of the circuit requires a modifications then it is necessary to redesign a chip. Using soft-core processors, systems can be integrated on a single FPGA chip, assuming that the soft-core processor provides adequate performance. Recently, two most popular soft-core processors have become available are Nios II from Altera and Micro Blaze from Xilinx. In this paper we use microblaze processor for designing multi soft Core architecture development.

III. THE MICRO BLAZE PROCESSOR

The Micro Blaze is a microprocessor that is built inside a Xilinx Field Programmable Gate Array (FPGA). The approach of using soft core processorsis that you only used as many of microprocessor as you want depending upon application and device utilization performance You can also used other peripherals to project as per your specific needs (i.e.: General Purpose Input/output peripherals, FLASH and UART etc.). The Micro Blaze processor[3] is a 32-bit Harvard (RISC) architecture optimized for implementation in Xilinx FPGAs with separate 32-bit instruction and data buses and access data from both on-chip and external memory at the same time.

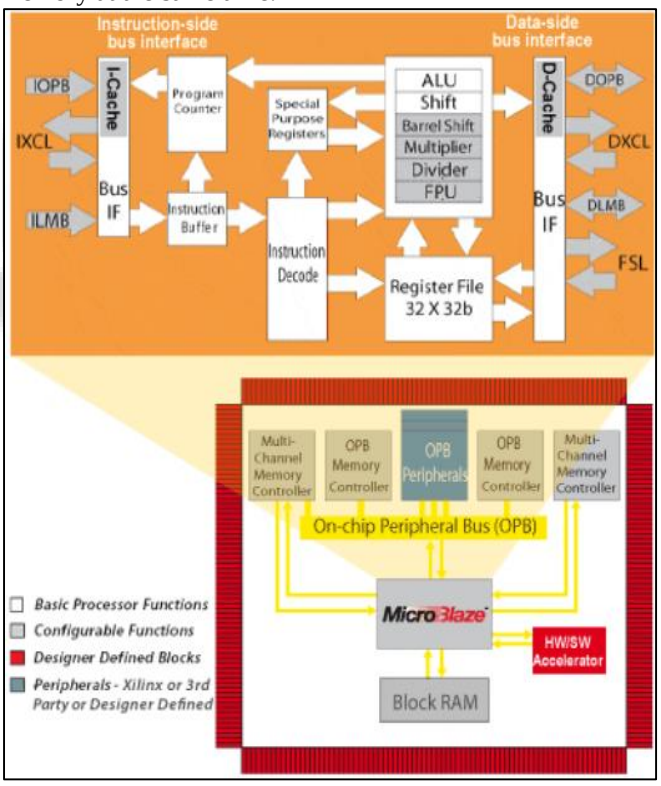

Fig. 1**:** A view of a Micro Blaze system

The MicroBlaze embedded soft-core includes thefollowing features:

- Thirty-two 32-bit general purpose registers
- 32-bit instruction word with three operands and twoaddressing modes
- Separate 32-bit instruction and data buses thatconform to IBM's OPB (On-chipPeripheral Bus) specification
- Separate 32-bit instruction and data buses withdirect connection to on-chip blockRAM through a LMB (Local Memory Bus)
- 32-bit address bus

- Single issue pipeline
- Instruction and data cache

IV. MEDIAN FILTER

Median filter is one of the image processing techniques for image filtering an image is stored in 2D matrix form [4]. Median filter uses a 2D mask applied on each pixel in an input image. In Median operation sliding a window of size 5x5 is used over an image at each position of window a pixels values are sorted and copied. Value of center pixel of window that is 13th pixel replaced with a median value. The obtained median value will be replaced with the value for that pixel in the output image.Figure2 shows an example of median filter.

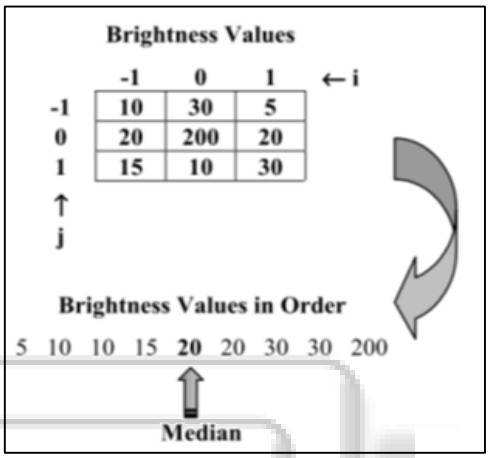

Fig. 2: example of median filter.

V. PROPOSED SYSTEM

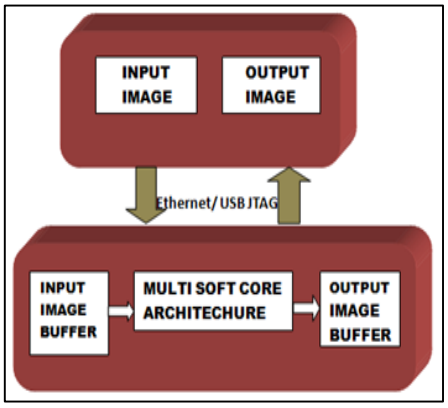

Fig. 3: Block Diagram of proposed system

An image was created in MATLAB .MATLAB transmits input image to FPGA using Ethernet or USB JTAG connection. Input image is stored in FPGA input image memory buffer. Input image is processed through multi soft core architecture which is implemented on FPGA. Multi soft core architecture consist of multiple soft core processors they assign a specific task to process an input image as per our applications, resultant image is stored in FPGA output image memory buffer. Then Output image is transmitted back to MATLAB. Connection between MATLAB and FPGA is established using Ethernet or USB JTAG. Output image is displayed in MATLAB. In this way, a proposed system can actually be tested with hardware in-the-loop, with input and output from MATLAB, to ensure that it is working. Furthered we elaborated detailed view of multi soft core architecture as shown in figure 4.

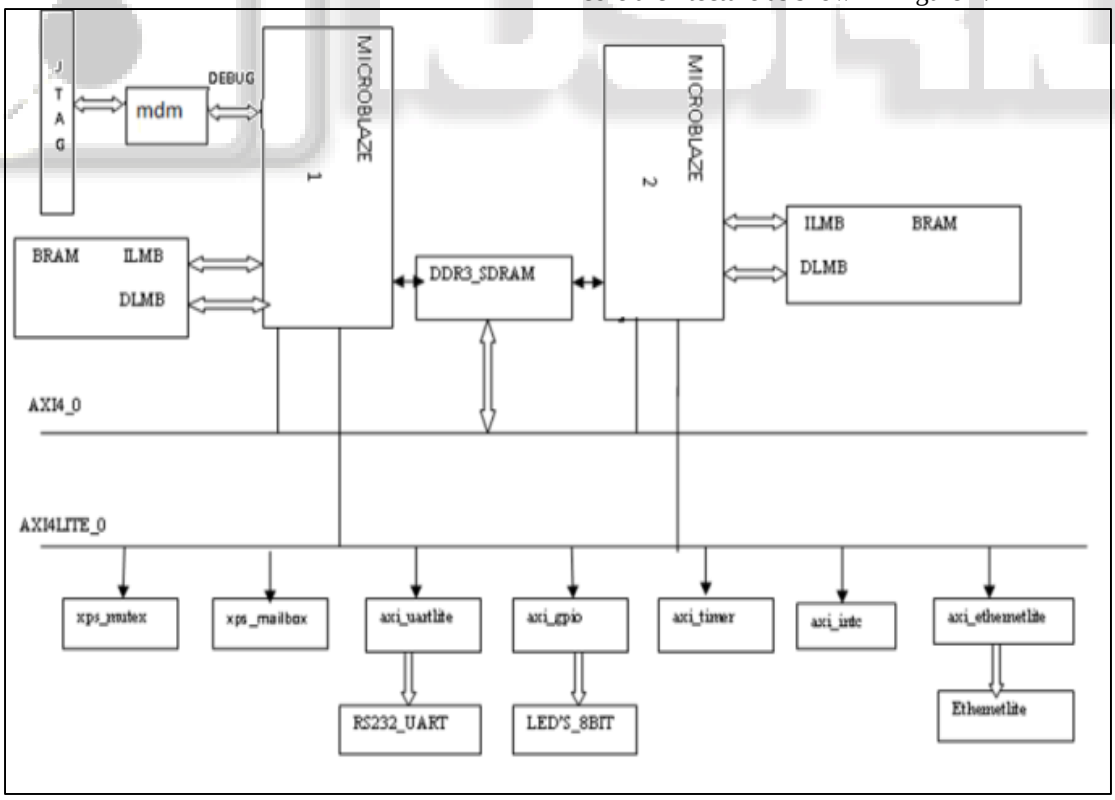

Fig. 4: Multi soft core architecture

The proposed architecture of multi core processors is interconnected using AXI bus. Among the two processors one is designed as a master, the rest was designed as slave processor. In This paper master slave configuration used control microblaze to receive all commands and slave microblaze are follow the commands, the Master slave configuration require good amount of work distribution. Xilinx system edition (EDK & SDK version 14.5) was used

to implement the interconnected architecture. Most of people preferred C/C++ language to write software application. Xilinx SDK used this format because EDK contain in built C/C++ compilers to generate necessary machine code that a microblaze processor understand. The proposed multi soft core architecture system was build by using two microblaze processor cores; detailed structure of the proposed system is shown in Figure 4.

VI. Design and Implementation

Design of any system involved software and hardware development. Xilinx Embedded development kit (EDK) used to design and implement multi soft core architecture. With the help of EDK any one can design a complete system and implemented on any FPGA devices as per user applications. EDK tool consist of Xilinx Platform Studio Software Development kit (SDK), with the help of SDK it is possible to design a software application for Microblaze processor in Xilinx EDK application which is written in C/C++ language, after designing complete system debug and download the Bitstream into FPGA then FPGA behaves like as multi soft core processor architecture implemented on Virtex 6 FPGA.

A. Design and implementation of multi soft core architecture

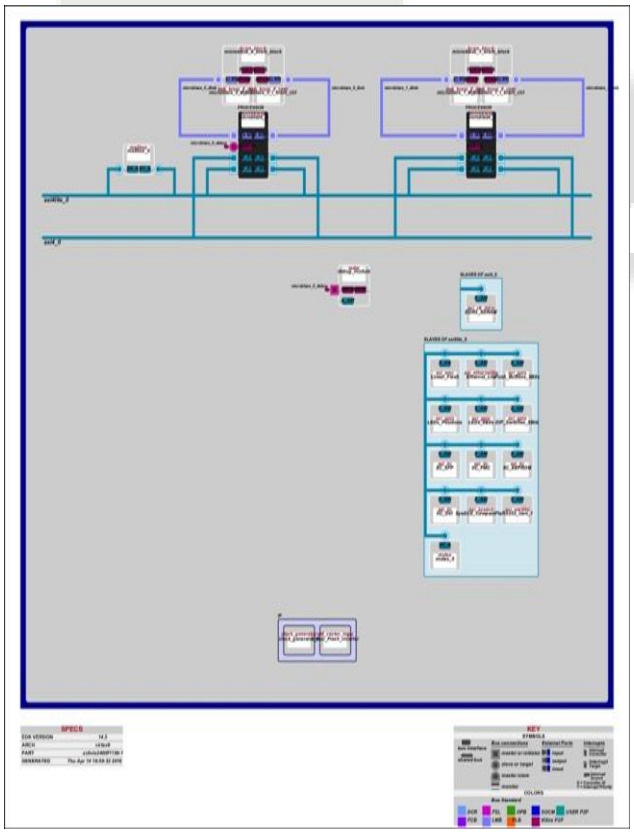

Fig. 5: Dual core microblaze processor design

A design step to create a multi soft core architecture using microblaze is as follows.

1) Create an XPS Project by using Base System Builder (BSB)
2) Create a simple hardware design by using Xilinx IPs available in the Embedded Design Kit.
3) Modified Xilinx generated software application as per need.
4) Implement the design.
5) Generate and Download the bit file to verify in hardware

This design was constructed with two microblaze processor on axi bus.XPS_Mutex and XPS_Mailbox cores are used to synchronize and pass messages between two processors .DDR3 SDRAM external memory accessed by both Processors via memory controller. Both processors have a debugger interface via the MDM core. Figure 5 shows a block diagram of the dual core MicroBlaze processor design.

B. Design and implementation of median filter on multi soft core architecture

Implement MATLAB algorithm in hardware by generating HDL code and deploying that code on Field Programmable Gate Array (FPGA). Write the MATLAB algorithm with syntax and functions that are compatible with HDL code generation. If the algorithm uses floating-point data, HDL Coder™ helps you to convert it to a fixed-point algorithm. After you generate HDL code and verify that it matches your original algorithm, deploy the HDL code on your target hardware design step for median filter implementation is follows.

1) Step 1: Adding Noise to the Image

Add the noise to the image by using the command in the MATLAB and then convert the data type into double data type. Generate the text file of the image.

2) Step 2: Processing of Image

In the second step removing of noise takes place.

3) Step 3: Read the Output Image

In the third step display of output image takes place. By using MATLAB, image can be displayed

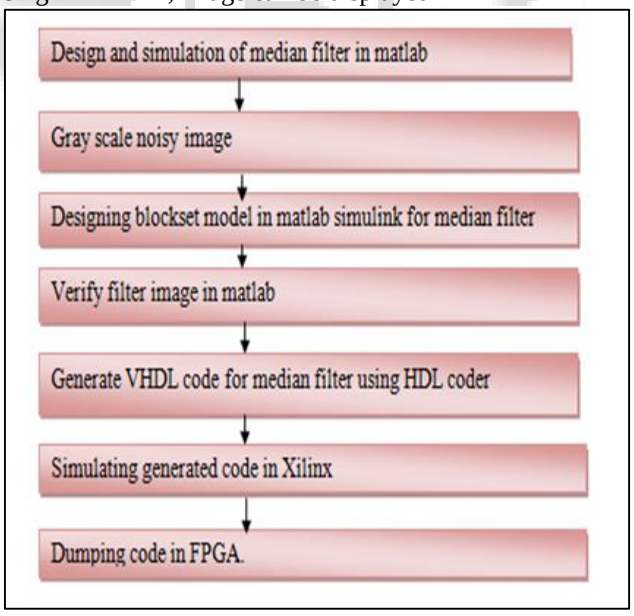

Fig. 6: Flow diagram for design and implementation of median filter in FPGA in HDL coder

VII. Matlab Simulation Results

Performance of median filter has been evaluated and tested using Matlab HDL Coder with different noise densities. Figure 7 shows original image, noisy and filtered images with noise densities 10% to 50%.

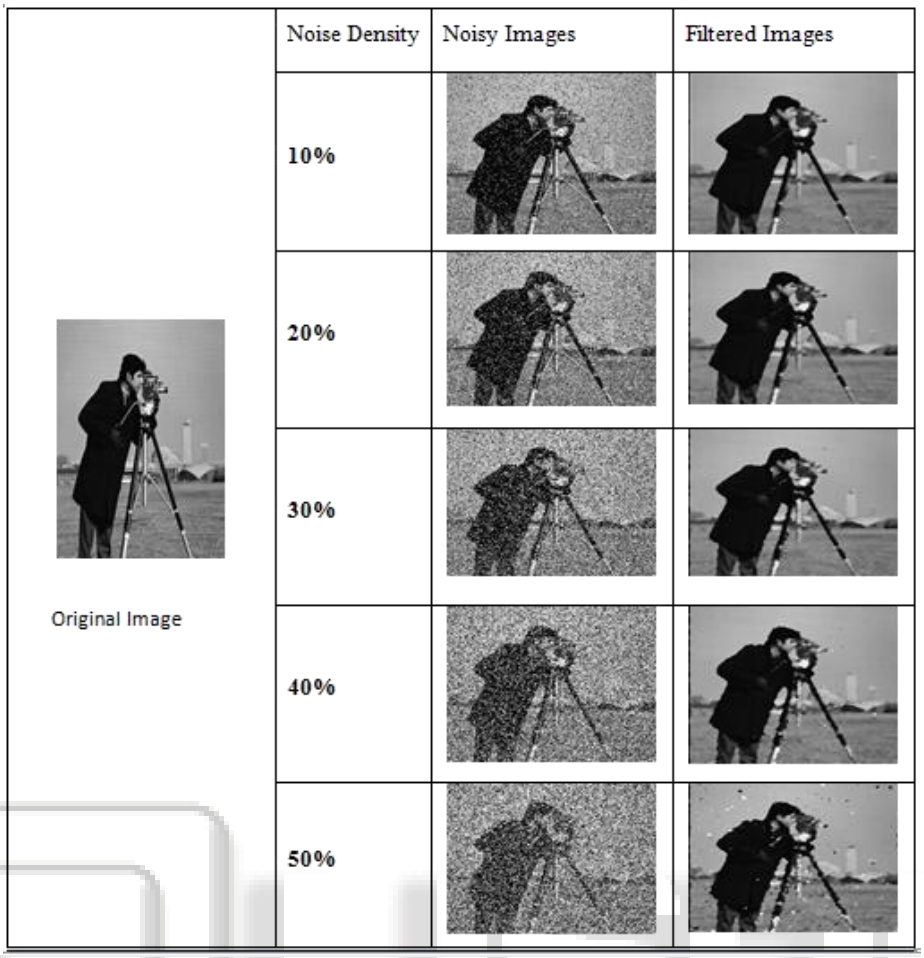

Fig. 7: Matlab simulation results

Device Utilization Summary (actual values)				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	9,369	301,440	3%	
Number used as Flip Flops	9,292			
Number used as Latches	1			
Number used as Latch-thrus	0			
Number used as AND/OR logics	76			
Number of Slice LUTs	11,236	150,720	7%	
Number used as logic	10,019	150,720	6%	
Number using O6 output only	7,729			
Number using O5 output only	227			
Number using O5 and O6	2,063			
Number used as ROM	0			
Number used as Memory	1,009	58,400	1%	
Number used as Dual Port RAM	288			
Number using O6 output only	12			
Number using O5 output only	10			
Number using O5 and O6	266			
Number used as Single Port RAM	11			

Fig. 8: shows device utilization summary for multi soft core architecture.

VIII. CONCLUSION

The design of Multi soft core architecture was done having one microblaze core as master and other microblaze cores as slave and implemented on virtex6 FPGA.whole system is connected using AXI bus. Median filter has been implemented on multi soft core architecture using matlab HDL Coder and performance has been tested for different noise densities. Design has been implemented on virtex 6 FPGA. Synthesis report generated for multi soft core shows that only 10 to 15% of virtex 6 slices use while implementing two microblaze processor therefore up to 8 microblaze processor can be used for designing and implementing multi soft core architecture on virtex 6 FPGA

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