Design and Implementation of Analog CMOS Phase Locked Loop using 180nm Technology

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Abstract— This paper deals with the design of Phase Locked Loop for achieving faster locking loop. The specific quality and property of fast locking of PLL is required in many clock and data recovery circuits. Many researches have been made to reduce this locking time but at the expense of power, phase noise and other parameters. Here, a PLL is implemented with redesigning of individual blocks like, phase and frequency detector(PFD) is designed using D flip flop to reduce area and static phase error, charge pump(CP) is designed to reduce the current mismatch using current mirrored structure and VCO has been designed using five stage current starved voltage controlled oscillator. The PLL is designed using 180 nm CMOS technology with 1.8 V power supply voltage.

Key words: Locking time, phase & frequency detector (PFD), charge pump(CP), voltage controlled oscillator(VCO), frequency divider(FDIV), phase locked loop(PLL), power consumption

I. INTRODUCTION

A Phase lock loop (PLL) is a closed loop control system that synchronizes an output signal with input signal in terms of frequency and phase. This synchronized state of PLL is referred as 'locked state'. PLLs are widely used in clock generation, frequency multiplication, data and clock recovery circuits and timing pulse distribution.

The phase and the frequency deviation between feedback and input signal should be ideally zero or constant at this locking time but in practical, small phase error occurs in the output signal. The time at which the output frequency of PLL matches the input frequency is known as locking time of PLL. This property is required in many clock and data recovery circuits.

Many researchers have tried to design PLL that offers either of the property of low power consumption, fast locking loop, high speed, less jitter, less phase noise and hence less area. This need gives rise to redesign of individual blocks in PLL. This paper presents a PLL with designing of each block to achieve fast locking time along with reduced power consumption.

This paper summarizes the detailed study of PLL with its individual blocks using Tanner Tool(S-edit, T-Spice, W-edit) in 180nm CMOS technology. The basics of PLL are described in Section-II. The implementation of PLL circuits and the calculative procedures are shown in Section-III. Section IV describes simulation results. Finally the conclusion and future scope is given in Section V.

II. BASICS OF PLL

A PLL is a closed loop feedback system as shown in figure 1 that compares the feedback signal with the input signal. This comparison is carried out by phase frequency detector(PFD). The basic building blocks of a PLL are Phase and frequency detector (PFD), Charge Pump (CP), Low Pass Filter (LPF) and Voltage Controlled Oscillator (VCO) in a feedback loop with a frequency divider.

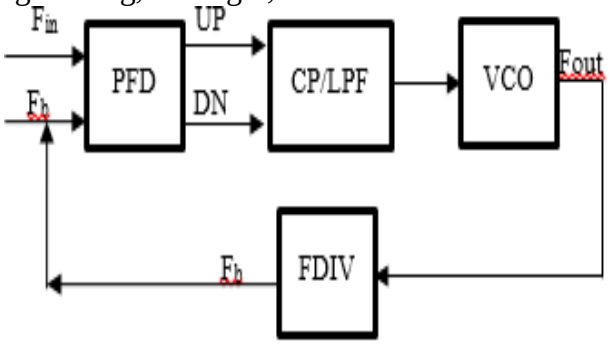

Fig. 1: Block Diagram of Phase Locked Loop [1]

The phase and frequency detector(PFD) generates a digital signal which drives the charge pump(CP) to either increase or decrease the control voltage of the VCO or to keep it unchanged. The charge pump then converts this digital signal to analog signal. This analog signal has high frequency signal which is undesired, also desired low frequency signal. Further, this high frequency signal is filtered out by a low pass filter and applied to the voltage controlled oscillator. This VCO output frequency (fout) is given to frequency divider where it is divided by the divider N. When the phase and frequency of input (Fin) and the divider output (fD) are aligned then the loop is said to be locked i.e. Fin=Fb
where Fb = Fout / N
and Fout = frequency of VCO output signal

III. WHOLE IMPLEMENTATION OF PLL BLOCKS

Parameters	Specifications
Technology	180nm
Locking Time	200ns(approx.)
Supply Voltage	1.8V
VCO Frequency	1 GHz

Table 1: Design Specifications of PLL

The whole PLL is designed here with the above specifications.

A. Phase Frequency Detector (PFD):

Here, PFD is implemented with Single Phase Clocked logic. Its circuit consists of two resettable, edge triggered D flip flops with their D inputs tied to logic 1. First, the UP and DN signals are set to low/zero and assuming both the REF frequency signal and the Vin signal are high/one. When a falling edge occurs on the REF input, the high or one on the D input is transmitted to the Q output or UP and similarly vice-versa for DN signal.

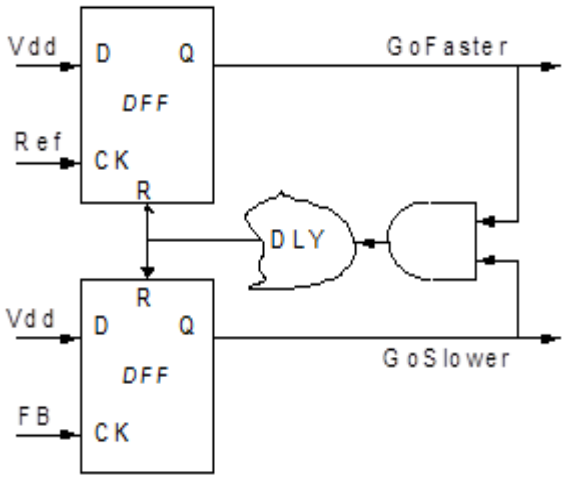

Fig. 2: Block Diagram of Edge Triggered PFD [1]

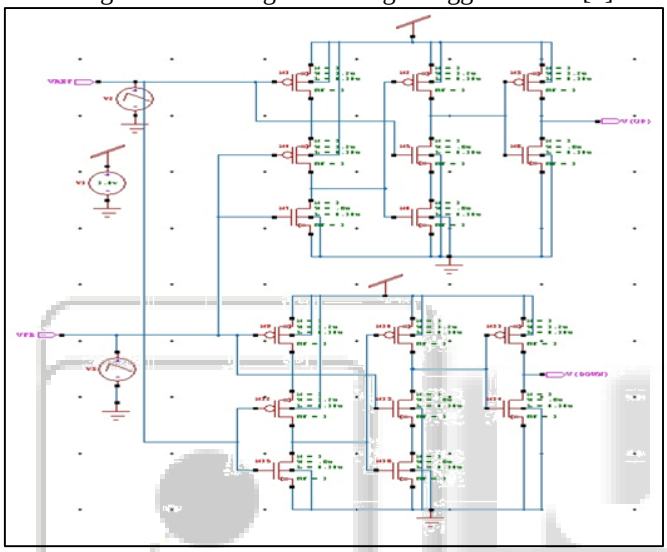

Fig. 3: Schematic of PFD (S-edit)

B. Modified Charge Pump (Cp):

The charge pump circuit is the heart of PLL. It transfers the digital signals of up and down from phase and frequency detector (PFD) to an analog signal in the form of control voltage for the VCO. The frequency of VCO is controlled by the output signal of charge pump circuit. [11]

The proposed charged is designed as shown in Fig.4. When the signal UP =1 (high logical level), P1 is 'OFF', the current source drives P3, when P3 is 'ON', P5 is 'ON', and so P3 and P5 compose a current mirror Capacitor Cp will be charged by the current source I1, raising the voltage DN =0 (Low logical level), pull-down network is OFF. When the signal UP =0 (low logical level), P1 and P2 are both 'ON'. P4 and N1 are used to pre-discharge to the gate of P5. On other hand DN =1 (High logical level), pull-down network is 'ON' and capacitor Cp will be discharged. When they are both ON, they operate in the saturation region. So, to carry the same currents, P4 and N1 have to be perfectly matched (IP4=IN1).

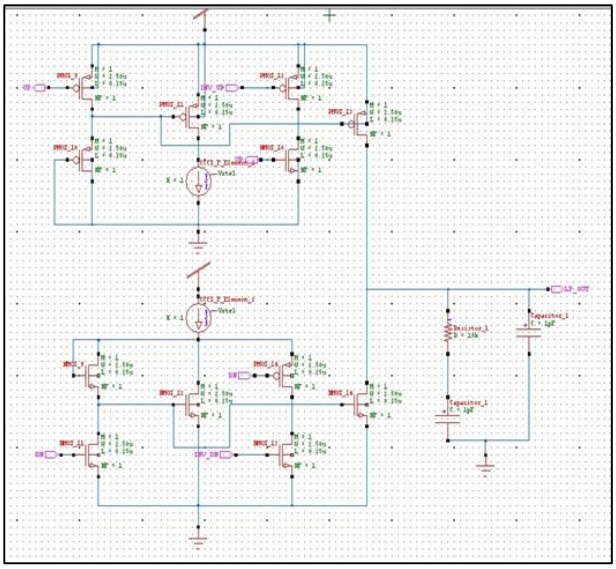

Fig. 4: Schematic of Charge Pump and Loop Filter (S-edit)

C. Low Pass Filter:

The loop filter designed in Fig. 4 consists of two capacitors and one resistor. Stability of the system is maintained even with the process variation of these on-chip components and second order low pass filter is used as Loop filter. The function of the loop filter is to convert the charge pump current to control voltage which is connected to VCO to control the frequency of VCO. The first-order loop filter does not have a second capacitor to smooth out current spikes which the second-order loop filter has.[11]

D. Voltage Controlled Oscillator:

The voltage controlled oscillator is the block where the input control voltage of charge pump controls its frequency output. VCO is initially tuned to the required frequency then the phase detector will compares the frequency of the input signal to that of the reference signal. VCO are used for achieving the frequency stability with respect to temperature, noise and power supply. A current starved voltage controlled oscillator(CS-VCO) is comprised of a number of stages, with the output of the last stage fed back to the input of the first. The ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. The schematic diagram of this VCO is shown in figure 5. [1]

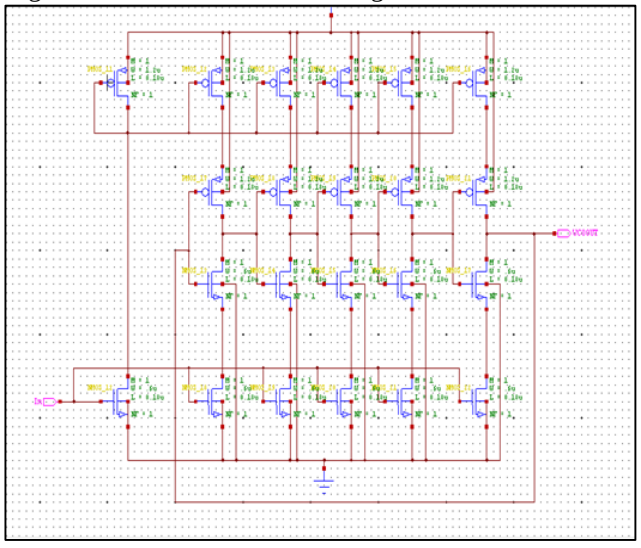

Fig. 5: Schematic of Current Starved VCO in S-edit

E. Frequency Divider:

The output of the VCO is to be divided before feeding back to the input of the PFD. A divider circuit as shown in figure 6.

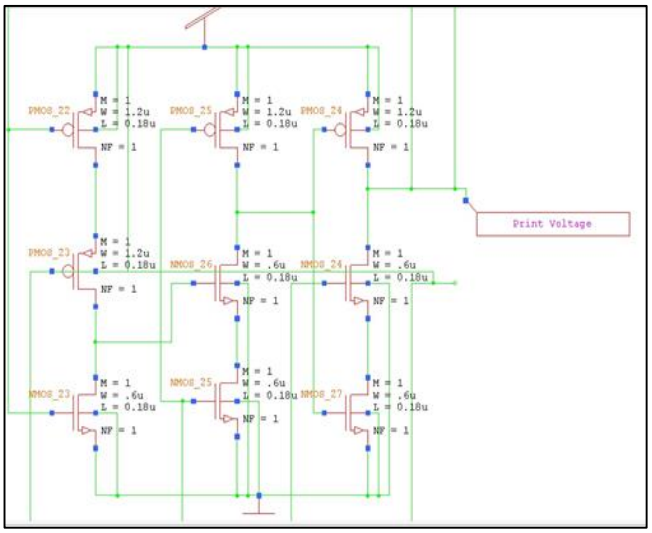

Fig. 6: Schematic of Frequency Divider in S-edit

It receives a reference clock signal of a frequency and is structured to divide the reference clock signal by N. It provides an output pulse signal for every N cycles of reference clock signal. [1]

IV. SIMULATED RESULTS

The output waveform and simulation results of various components of PLL is shown in figure 7,8,9 and Table 1 respectively.

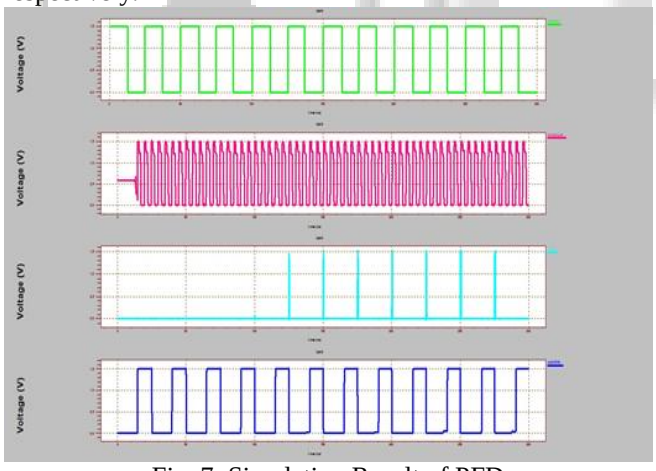

Fig. 7: Simulation Result of PFD

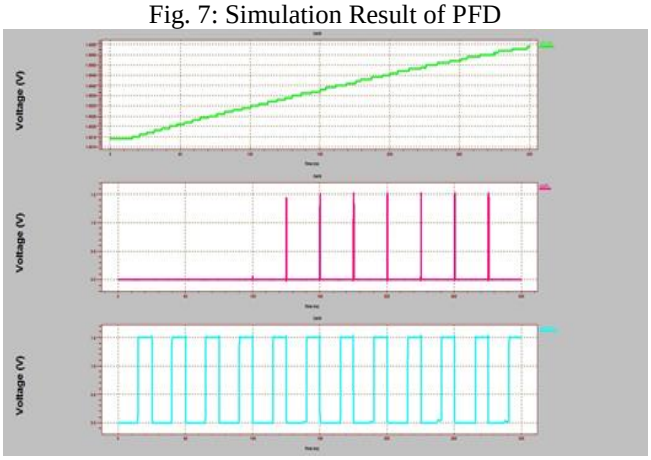

Fig. 8: Simulation Result of Charge Pump and Loop Filter

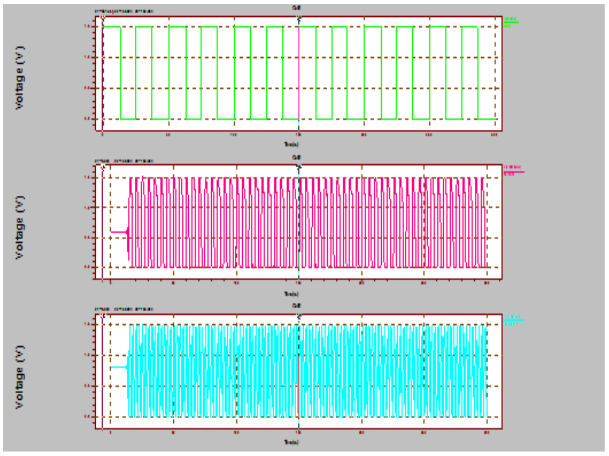

Fig. 9: Simulation Result of VCO & Frequency Divider

Parameter	Paper-1 [4]	Paper-2 [3]	Paper-3 [12]	Proposed Work
Technology	350nm	180nm	180nm	180nm
Locking Time	10 ms	75 us	554ns	150ns
Supply Voltage	3.3 V	5 V	2 V	1.8 V

Table 2: Comparison of Results with Specification

V. CONCLUSION

In this paper fast locking and low power PLL has been designed and simulated using 180 nm CMOS technology of tanner tool and for the analysis of locking time. Thus the PLL is designed with a very less locking time of 150ns at the VCO frequency of 1GHz. This can be further reduced to 100ns or less by increasing the number of stages of CS-VCO or by using another type of VCO. The additional step of this work is to measure power consumption.

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