Survey on Different Concepts about Carry Skip Adder

Blessy Mathai[1] Nizy Thomas[2]
[1]PG Scholar [2]Assistant Professor
[1,2]Department of Electronics and Telecommunication Engineering
[1,2]CKC, Kerala, India

Abstract— Digital computers perform a variety of processing tasks. Addition is one of the most important computation processes in digital system. To perform addition we need an efficient adder.one of the most efficient adder is the carry skip adder.(CSKA).In this paper we are conducting a survey on different improvements in carry skip adders.
Key words: Carry Skip Adder(CSKA), Carry Increment Adder(CIA),Carry Select Adder(CSLA),Carry Save Adder(CSA) And Parallel Prefix Adders(PPA)

I. INTRODUCTION

VLSI industries are meant for low power circuits. Adder circuits are the main building blocks of digital circuits. In the case of DSP and control system one of the most important computation processes is the addition. The accuracy and speed of computation depend on efficiency of adders.

Different types of adder families are there like Ripple Carry Adder (RCA), Carry Increment Adder (CIA), Carry Select Adder (CSLA), Carry Save Adder(CSA) And Parallel Prefix Adders(PPA).RCA has the simple structure and have greater power consumption. CSLA have more speed than RCA. One of the fastest structures is PPA. Among all these adders one of the most efficient adder is the Carry Skip Adder (CSKA).The most highlighted advantageous of CSKA are lower delay, power consumption and area usage.

The rest of this paper is organized as follows. Section II discuss related works on carry skip adders. Survey about different concepts related to carry skip adder is discussed. Section III is finally the conclusion.

Literature Review

Lehman and Burla [1] found firstly about the concepts of carry skip adder. The concept is based on detection and bypassing of stages when there exist a condition for carry propagation exists. Meaning is that carry signal can bypass those stages of carry circuits when input is different. They also found optimal number of equal size group for a CSKA and also suggest that variable block size is also acceptable.

Majerski [2] describes the formulas for variable block size optimization. He also gave formulas for two level adders. The major drawbacks of this paper are wire delays and non-restoring logics were not considered and also there is no derivation for the formulas.

Oklobdzija and Barnes [3] derive an optimum scheme for determine one level and two level CSKA group lengths. And also assume that time needed for skipping a block was constant. He publish another paper describe a well-designed carry skip adder.

Turrini [4] publish a search algorithm which can produce arbitrary number of skip levels. The basic concept behind the algorithm is that assign a pair of delays to a carry generation and carry ending that block. Each block contain delay and also contain maximum number of blocks. The algorithm can be divided into two steps. The first step is partitioning and delay assignment. The second step is building the tree. The first step describes that starting with total carry delay the highest level is computed and assign to corresponding blocks. The second step describes that the whole tree will be generated starting from top to down. Thereby producing optimum structure. The drawback of algorithm is that it requires larger execution time and the adders shown is not optimum.

Chan shlag [5] integrate second order CMOS technology to one level carry skip adder. The concept is that ripple delay is proportional to square of length of block and therefore skip delay is linearly related to length of block also assume that there is a constant delay between stages. They also describes carry life time equations based on carry generated in first block and skipping and then end in last block. The drawback of this paper it does not assist multiple level carry skips.

Alioto and Paiumbo [6] present a simple design for single level CSKA. The design is based on the concept that variable stage size technique in which minimum number of full adders are determine based on time delay of mux and time required by a carry to ripple through a FA.it consider a non-integer ratio.so by using this method critical path delay is reduced.

Markovic [7] design a low power adder operates in threshold region. He explains that energy consumption is same in sub threshold and threshold region. Weak, strong moderate region is also considered and it is a very useful paper in design means.

C.K Koh [8] describes that in variable latency adder there is no power and negative bias temperature instability. By using this concept he designs an adder which consumes low power and also saves energy.

Milad bhahadori [9] propose an energy efficient CSKA .He replaces the mux stages in conventional carry skip adder which contains more number of transistors by AOI/OAI gate which have fewer transistors and thereby reduces the area and delay. Also he introduce concatenation and incrementation technique to conventional design of carry skip adder to became energy efficient. The reason for using AOI/OAI gates as skip logics is the inverting functions. Concatenation approach uses a RCA block with carry input of zero. So that RCA block does not wait for the carry output of previous stage. Delay is small because delay of skip logic is considerably smaller.

II. CONCLUSION

In this paper we conducted a survey on different concepts that used in carry skip adder to improve speed energy efficient etc. The carry skip adder is an efficient adder in terms of power consumption and area usage. There are many attractive features are there in CSKA. Different improvements can be made in CSKA. A modified structure by combining the concatenation and the incrementation schemes to

conventional scheme thereby increasing the speed and also energy efficient. Investigations are going on the impact of voltage scaling on the efficiency of the modified CSKA. Also discuss about the concept of hybrid variable latency extension to the CSKA structure.

REFERENCES

[1] M.Lehman and Burla " skip techniques for high speed carry propagation in binary arithmetic units." IRE TRANS.E.Comput,vol.ec.EC-10NO.4 PP.691-698 DEC1961.

[2] S. Majerski, " On determination of optimal distributions of carry skips in adders," *IEEE Trans. Electron. Comput.*, vol. EC-16, no. 1, pp. 45– 58, Feb. 1967.

[3] V. G. Oklobdzija, B. R. Zeydel, H. Dao, S. Mathew, and R. Krishnamurthy, " Energy-delay estimation technique for highperformance microprocessor VLSI adders," in *Proc. 16th IEEE Symp. Comput. Arithmetic*, Jun. 2003, pp. 272– 279.

[4] S. Turrini, " Optimal group distribution in carry-skip adders," in *Proc.9th IEEE Symp. Comput. Arithmetic*, Sep. 1989, pp. 96– 103

[5] M. Alioto and G. Palumbo, " A simple strategy for optimized design of one-level carry-skip adders," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, no. 1, pp. 141– 148, Jan. 2003

[6] P. K. Chan, M. D. F. Schlag, C. D. Thomborson, and V. G. Oklobdzija, Delay optimization of carry-skip adders and block carry-lookaheadadders using multidimensional dynamic programming," *IEEE Trans. Comput.*, vol. 41, no. 8, pp. 920– 930, Aug. 1992.

[7] D. Markovic, C. C. Wang, L. P. Alarcon, T.-T. Liu, and J. M. Rabaey, " Ultralow-power design in near-threshold region," *Proc. IEEE*, vol. 98,no. 2, pp. 237– 252, Feb. 2010.

[8] Y. Chen, H. Li, J. Li, and C.-K. Koh, Variable-latency adder (VL-adder): New arithmetic circuit design practice to overcome NBTI," in *Proc. ACM/IEEE Int. Symp. Low Power Electron. Design (ISLPED)*, Aug. 2007, pp. 195– 200

[9] S. Ghosh and K. Roy, " Exploring high-speed low-power hybrid arithmetic units at scaled supply and adaptive clock-stretching," in *Proc. Asia*