Low Power High Speed Multiplexer using CMOS Technology for Industrial Applications

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Abstract— In today's digital era, CMOS technology is the cornerstone of semiconductor devices for years. With shrinking technology, reducing area and power consumption are the key challenges due to increased complexity. In digital design, Multiplexer is the core of any arithmetic circuits. Multiplexers are common building blocks for data path and data switching structures. It is used effectively in many applications which include processors, processor buses, network switching and DSP's with resource sharing. Also MUX plays a significant role in the working of CCTV cameras. We hereby designed and compared the multiplexers in several logic styles which provide high speed switching, reduction in transistors, minimal power usage and reduction in area.

Key words: Multiplexers, CMOS, Transmission Gate, Pass Transistor Logic, ALU

I. INTRODUCTION

The low power consumption is the major concern in the system SOC design, different techniques and technologies have been designed and developed for low-power applications [1]-[5]. The varieties of approach have been proposed to reduce power usage of MUX.

Multiplexers are key components in CMOS memory units and data manipulation structures. The need for low-power very large scale (VLSI) circuits can be designed at different levels. The basic chip design hierarchy is composed of five levels namely system, logic, circuit, physical and fabrication level. In circuit level design, the capacity for power stake prevailed by virtue of choice in logic style for implementation of combinational circuits. Low power logic style analysis is reported in the research; however it is predominantly concentrated on particular logic cell specifically multiplexers, used in arithmetic circuits.

Multiplexer plays a significant role in the digital system designs. They are used in various fields were multiple data need to be transmitted using a single line. Some of the applications of MUX are cameras, telephone network, building blocks of FPGA, computer memory and processor. Multiplexers are used to integrate multiple audio signals on a single line in the telephone network communication. In computer memory they are used to incorporate large amount of memory into the computer, simultaneously it reduces the count of copper lines. In CCTV the motion captured by different camera which is displayed on a single monitor screen.

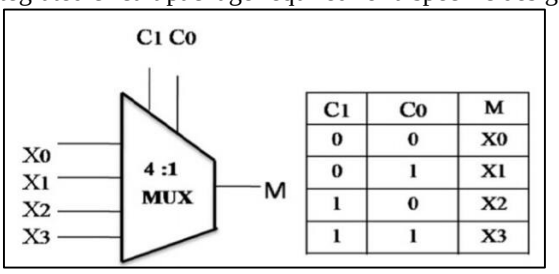
Moreover, it also reduces the layout area. MUX is expanded as multiplexer which is the core of any arithmetic circuit. In digital design multiplexer acts as a building block for the path of data and its switching structures, also used effectively in various applications including network switches, DSPs with resource sharing, processor and its buses.

The basic significant factor in today's trend that increases the presumption of the users for more and more backup time in miniature gadgets could be achieved by long battery back-up time. Hence the power consumed by MUX is a keystone to regulate. In reconfigurable architectures such as FPGAs, the area and power of MUX and interconnections have been far balanced the area and power of the functional units and registers. For example, in the FPGA Performance Benchmarking Methodology, it has been estimated that MUX normally occupies more than 25 % of the area in an FPGA design.

II. MULTIPLEXER

In large scale digital system design [1][8] a line is needed to carry multiple digital signals. We know that, only one signal can be passed at a time over a line. In this case a tool is required that will allow us to select, the signals we like to pass on this common line, at different instance. Such a device is named as Multiplexer. The function of multiplexer is to select any one of 'n' inputs and produce the single output. Therefore, multiplexer are referred as data selector. Fig 1a,b shows the symbol and truth table of 4:1 MUX.

In order to minimize the cost of the system, multiplexer are used by permitting the reduction of number of integrated circuit package required for a specific design.



C1	C0	M
0	0	X0
0	1	X1
1	0	X2
1	1	X3

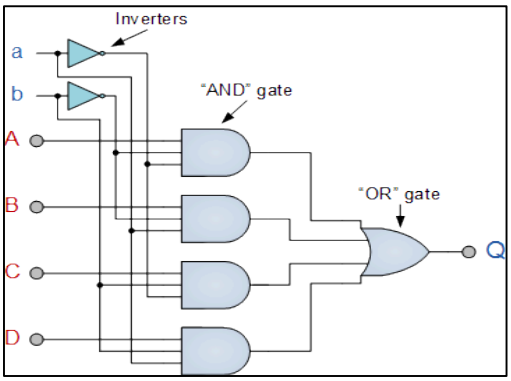
Fig. 1: (a) 4:1 MUX Graphical Symbol, (b) Truth Table

$$Output = X0.\overline{C0}.\overline{C1} + X1.C0.\overline{C1} + X2.\overline{C0}.C1 + X3.C0.C1$$

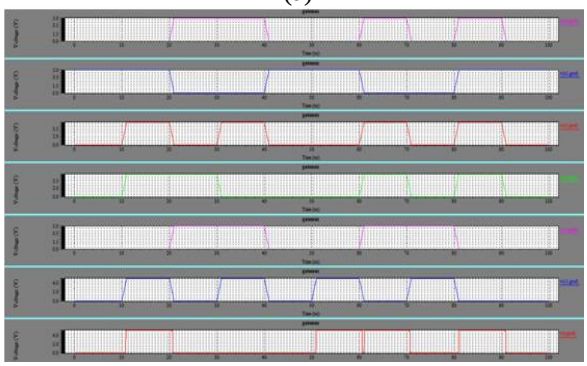
The above figure consists of four input lines x0, x1, x2 and x3 which is feed on one output line M. These inputs are called as data inputs and the additional two input signals c1, c0 are called as selection inputs. This selection input selects x inputs which has to be appeared on output (i.e.) M.

III. EXISTING METHOD

The existing method is the conventional CMOS logic method, where the design is represented in terms of logic method. Since we are dealing with transistor method, the logic level is converted into circuit level (i.e.) transistor method [1].



(a)



(b)

Fig. 2: (a) Gate implementation of a 4:1 MUX, (b) Output

The transistor level architecture requires large number of transistor. In 4:1 MUX design as shown in fig 2(a) each AND gate is replaced with 6 transistors, OR gate with 6 transistors and NOT gate with 2 transistors. So the complete design comprises of 54 transistors.

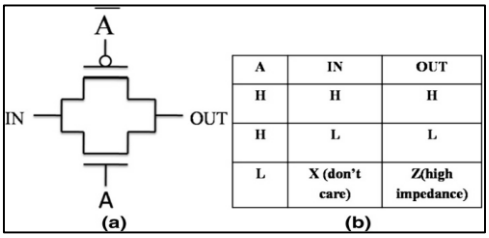
Due to increase in the count of transistors the required functionality will consume enormous power and abundant area, so the switching speed will be slow and the circuit looks complex. As a result, this method is not considered advantageous for shrinking technology.

IV. PROPOSED METHODS

The proposed methods are transmission gate and pass transistor logic. The main aim of the paper is to implement the MUX design with very minimum transistors compared to existing CMOS design.

A. Transmission Gate Logic

The transmission gate is an electronic element that is used to block or allow a signal level from the input terminal to the output terminal. It is constructed with CMOS technology and it functions as a non-mechanical relay. The parallel connection of NMOS and PMOS functions as switch is so called as transmission gate. The input to one of the transistor is the complementary input of the other transistor that both transistors are either ON or OFF [2].



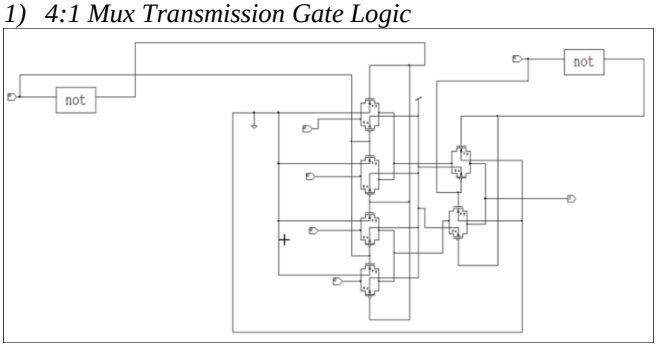
A	IN	OUT
H	H	H
H	L	L
L	X (don't care)	Z(high impedance)

(b)

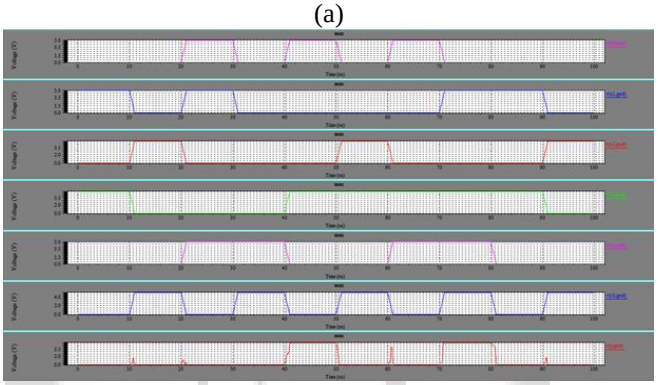
Fig. 3: (a) Transmission gate graphical symbol, (b) Truth table

When the input voltage at node A (NMOS) is Logic '1', the complementary '0' is given to active-low node A (PMOS), letting both the transistors to conduct and permits the signal from input to output. When the voltage at active-low node A is a logic '1', node A is applied with logic '0' which is complementary of active low node , switching off both transistors and driving a high-impedance condition.

1) 4:1 Mux Transmission Gate Logic



(a)



(b)

Fig. 4: (a) Transmission gate based 4:1 MUX, (b) Output

Fig 4(a) shows the connection of transmission gate that builds a structure of MUX. Every single transmission gate functions as an AND switch to replace the AND logic gate which is used in a conventional gate design of MUX which consists of 6 transistors. In this design each AND gate is built of only 2 transistors. Hence, the device count is reduced, so automatically the power consumption will be minimum and the switching speed will be high.

The performance of higher end design is verified and the analyses are made on 8:1and 16:1 MUX. Thus this design is said to be efficient.

B. Pass Transistor Logic

Pass transistor logic is a popularly and widely used alternative for complementary CMOS, that attempts to reduce the count of transistors required for implementation of logic by permitting the prime inputs for deriving the terminals of gate and source drain [3]. For connecting two nodes conditionally, the pass device acts as a switch. It is also often appropriate when the function of logic is conveniently analyzed as signals or tokens being temporarily steered through a network.

Compared to gate logic implementations, the utilization of NMOS transistor as a pass element in NMOS transistor logic leads to area savings, less power dissipation and speed improvements. NMOS pass- transistor networks will reduce complex designs to highly regular structures that functions faster than conventional logic gates. These networks of NMOS pass-transistor have poor low-to-high

transition characteristics. The disadvantage by using a parallel connection of PMOS and NMOS transistors is overcome by CMOS transmission gate. By considering, the pass transistor logic produces better area and improvement in speed when compared to CMOS gate logic.

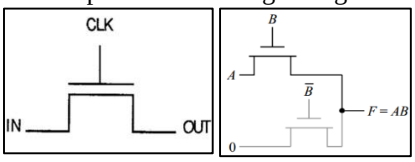
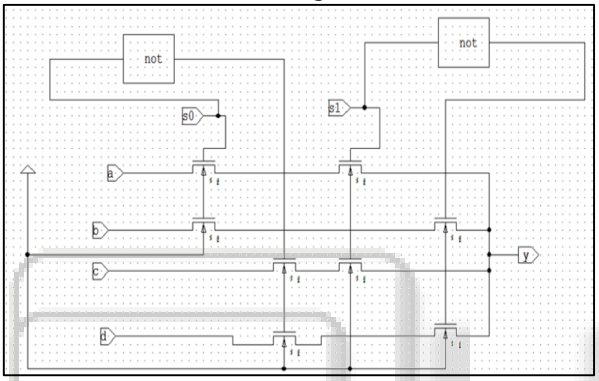


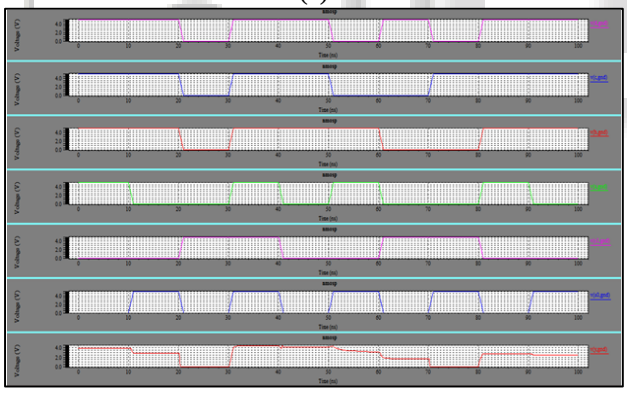
Fig. 5: (a) Pass- Transistor Logic Graphical symbol, (b) AND gate

Fig 5(b) shows the pass transistor logic for AND gate. When B is high, the output F=AB. In this logic design, each AND gate is replaced with a single transistor. So the PTL design is considered to be more advantageous than transmission gate and conventional logic method.

1) 4:1 Mux Pass Transistor Logic



(a)



(b)

Fig. 6: (a) Pass- Transistor Logic 4:1 MUX, (b) Output

Fig 6 (a) shows the connection of pass transistor logic that builds a structure of MUX. In order to analyze the performance of higher end design, examinations are made on 8:1and 16:1 MUX. As a result, the design is said to be efficient.

V. RESULTS

Logic Style	Parameters	4:1 MUX	8:1 MUX	16:1 MUX
Conventional Logic	No. of transistors	54	128	270
	Power consumption	2.10mwatt	2.41mwatt	2.52mwatt
Transmission Gate Logic	No. of transistors	16	34	80
	Power consumption	182µwatt	320µwatt	453µwatt
Pass Transistor Logic	No of transistors	12	20	60
	Power consumption	82µwatt	193µwatt	357µwatt

Table 1: Various multiplexers comparison table

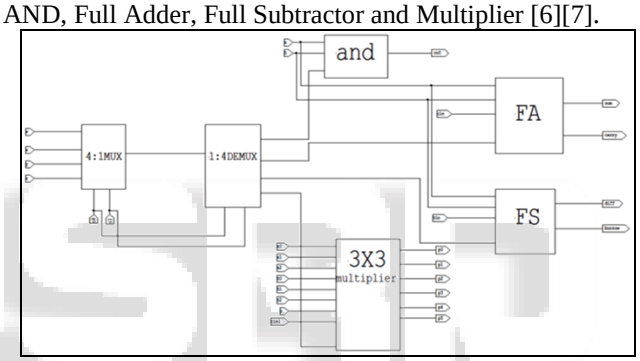
From the analysis of three designed multiplexer logics as shown in Table 1, the PTL (pass transistor logic) is the more efficient in terms of the power consumption, number of transistors, switching speed and ultimately reduction in area.

The TGL is efficient when collate to conventional logic style whereas PTL is significantly more efficient in terms of all the required parameters. Moreover various designs can be implemented by using comparatively few MOSFETs, thus the area and power consumption is reduced. Since the area is reduced the cost of implementation is also diminished.

Thus, Pass transistor logic proves to be an efficient way to design the multiplexers that is suitable to meet the requirements of digital circuits where they need to be considerably small in size, less power consumption and also perform operations in faster manner.

VI. DESIGN OF SIMPLE ALU

From the above analysis it is found that pass transistor is said to be efficient. By using this efficient PTL multiplexer design an Arithmetic Logic Unit (ALU) is designed as shown in fig 7(a) which performs the operations such as AND, Full Adder, Full Subtractor and Multiplier [6][7].



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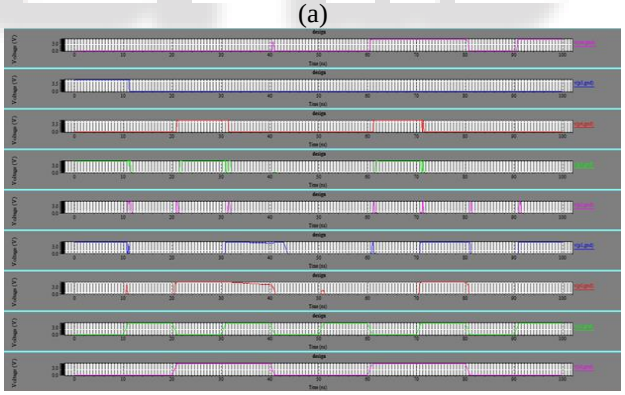

(b)

Fig. 7: (a) ALU Design, (b) ALU Output

VII. CONCLUSION

To design an energy efficient and a speedy multiplexer, the Pass Transistor Logic is proposed as an efficient design that involves reduction in count of transistors with minimal power consumption that includes the switching speed while compared to other multiplexers. This process of designing will not only increase the speed but also provide an efficient power consumption mechanism. The research work performed in this paper will achieve good results and also demonstrate the efficiency of high level optimization techniques.

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