Area Efficient Architecture for Network on Chip (NoC) based Router

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Abstract— This work consists of FPGA based design of reconfigurable router for NoC applications using VHDL. The router designed in this proposed session has four channels (namely, east, west, north and south) and a crossbar switch each consist FIFO buffers and multiplexers. FIFO buffers are used to store the data and multiplexers are used to control the input and output of the data. Firstly, south channel is designed which includes the design of FIFO and multiplexers. After that, the switch, arbiter and crossbar will design. All these designed channels, FIFO buffers, multiplexers and crossbar switches are integrated to form the complete router architecture. The proposed design is simulated using Modelsim and the RTL view is obtained using Xilinx ISE 13.4. Xilinx SPARTAN-6 FPGAs are used for synthesis of proposed design. Fixed priority arbiter is used to reduce the area of the proposed reconfigurable router.

Keywords: Network on Chip (NoC); Reconfigurable Router; First in First out (FIFO) Buffer; Crossbar Switch; Multiplexer; Register Transfer Level (RTL) Design, Low Power

I. INTRODUCTION

As per the work showing that due to technology has been enhanced the concept of network on chip is arises. In the same plane no of transistors can be implemented thus instead of designing tough processors, the technique is to replicate and include many easy way. By increasing the number of devices requires a proper interconnection structure inside the chip earlier designs are depends on buses or crossbar. There are three basic components in network on chip- routers, processing elements, and network interface. In all the router is perform the most important part as all performance improvement, low area, and low power are basic requirements of the router design. There are several routers are used in the design. A router contains various components like FIFOs, Arbiters. The IP cores are the main cause for the making blocks of much system on chip (soc) designs for implementing larger and complex applications of embedded system. This system of integration is called multiprocessor system on chip. The processing elements can be processors, Intellectual Property cores memory blocks and I/O communication modules [2]. A better interconnection is needed for transferring the data among various IP cores on a single chip. There are some types of interconnections namely optical fiber, Carbon Nanotubes, point to point, bus architecture and Network on chip. Among all of those a new concept called Network on Chip (NoCs) has been taken instead of previous type of chip interconnections [3]. as the number of IP cores increases, the previous type of approaches are not able to provide proper interconnection so NoCs are the best concepts of wide scale networks. A well designed structure is needed to perform the communication among IP cores. Because NoCs contain large number of IP cores on a single chip, the communication among these is a main problem. Communication among these IP cores should not be complex one. The main focus area of the present paper is to design a router which requires less area and also consume less power as compared to conventional routers and can be used in our Network on chip systems.

II. LITERATURE REVIEW

According to the concept of System on Chip, for point to point links communication between one IP to another buses are used, but these cannot gives proper interconnection from performance point of view so That network on chip architecture was introduced to provide communication in multiprocessor SoC(system on chip) and overcome the drawbacks[12] that why the concept is taken from large scale multiprocessors and wide area network domain and envisions on chip routers based network[18]. A design approach to on chip for reconfigurable systems is presented in [6]. It also shows about NOC topology & design of size of the buffers. Communication among processing elements, and integrated solutions to challenging design problems in the communications among different IPs are presented in [3]. Challenges and opportunities in software development based on the present hardware trends and the impact of massive parallelism on both the software and hardware industry are presented in [4]. Customize the routers in a network. Addressing Heterogeneous Bandwidth Requirements in Modified Fat-Tree Networks-on- Chips [7] an schematic for satisfying heterogeneous bandwidth requirements of clients connected using a modified Fat Tree network-on-chip [5] shows the design of a dynamically reconfigurable NOC router with bus dependent interface and shows integration of components in NoCs architecture with fixed IP, reconfigurable components, processor cores.

. [9] A complete synthesis flow, called Net Chip, for NOC architectures that divides the development work into main steps (topology mapping, selection, and generation) and provides proper tools for their automatic execution. A novel based technique including system-level physical design, and interconnection network generation that generates custom low power NOC architectures for application specific SOCs is presented in [10]. [11] Switching & round robin arbitration concept and dead lock free routing. The latest methodology that router having eight input ports and one output port for Network on Chip using IP core [12]. [14]Router architecture. In this architecture we can dynamically arranged different buffer depth for the channel. One problem in this architecture that it consuming more power. So including all such problems we require implementing a router architecture which uses less power and provide much better performance. Small optimizations in fig.21 NoC router architecture can show a important enhancement in overall performance of NoC based systems. On using simple algorithm and decoding logic [13] gives a design of 5-port 32-bit and 2D mesh network consist of 64 bit router architecture. According to this portion of architecture a large FIFO size is wasted even for short message because the router architecture described in [13] has a fixed and large FIFO size the router architecture given by Matos, this architecture uses less number of FIFOs for storing large data.

In this fig. Portion there are 4 channels south, east, west and north. They are connected with each other via crossbar switch. South channel is shown in Fig. From diagram each of 4channel consists of 5 Multiplexers, and two of such multiplexers are used to control the input and output data, while Other 3 multiplexers are used to control the read and write command of the FIFO.

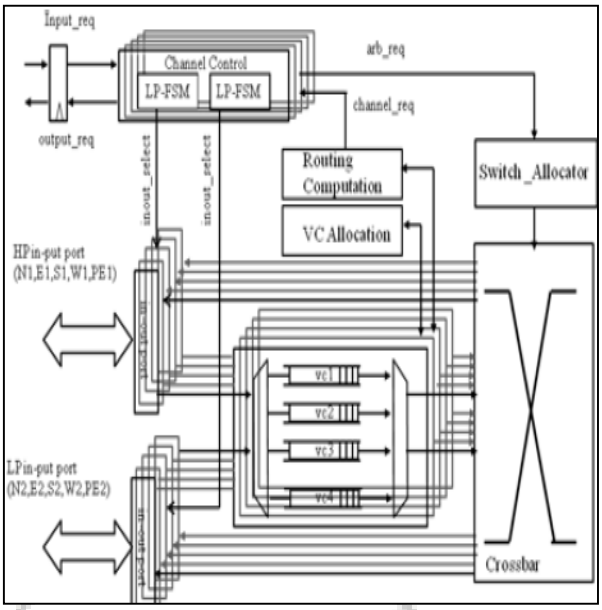

Fig. 1: Modified four-stage pipelined router architecture for our proposed BiNoC router with VC flow-control technique.[17]

Router is the main component which playing a important role in network on chip architecture, thus router should be properly designed because by proper interfaces Cores enters in the network and their packets linked to destination via routing path so routers are an important component for NOCs.

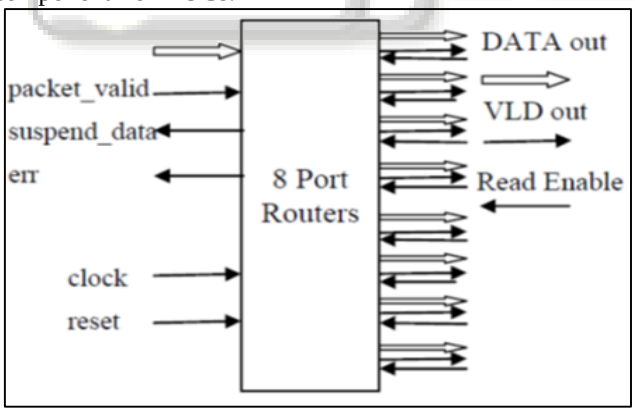

Fig. 2: BLOCK DIAGRAM OF 8 PORT ROUTER[18]

This project uses 4 port router design and I verified the function of this router by latest verification methodologies and by using cover points, cross and different test cases I improved the functional coverage of router. This paper helps us to understand the complete functional verification process of complex ASICs an SoC's and it provides an opportunity to try the latest verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages and sophisticated EDA tools, for the high quality verification .the functional coverage of Router is enhanced by me by using these tests and also by using 1 master and 8slaves to monitor the Router. So the functional coverage of Router was improved.[18]as the functional verification decides the quality of the silicon, we spend 60% of the design cycle time only for the simulation. Thus we can overcome the delay and meet the TTM.

For mesh network this network on chip router design has been tested. It is simulated with help of modelsim and an Xilinx 13.1 is on vertex xcv2-256 is used for implementation and in this architecture the results verified 2 dimensional deadlock free operations because of the store and forward behaviour There is a problem on latency in design because it follows store and forward behaviour[19]. [19] Network on chip is nothing but a proper way of building communication subsystems between intelligent property (IP) cores in System on chip with greater efficiency. The on chip router provides much better global on-chip communication, less complexity with great performance and also expected routing functionality. In this router architecture to overcome router latency drawback we introduced a new pipelined router design. In such design we limit the router frequency by identifying the router components that take most of the critical path. we also simplify the arbiter logic by using multiple smaller arbiters because the arbiter is the main cause that limits the router functionality. A new router design has been evolved by taking the initial set of requests in the initial arbiter is then distributing them over the smaller arbiters the operate in parallel.[20]this architecture provides simplicity because in the new technologies the no of cores in chip systems are keeps increasing by using 2D mesh topology and dimension order routing(DOR)(gives simplicity)algorithm.

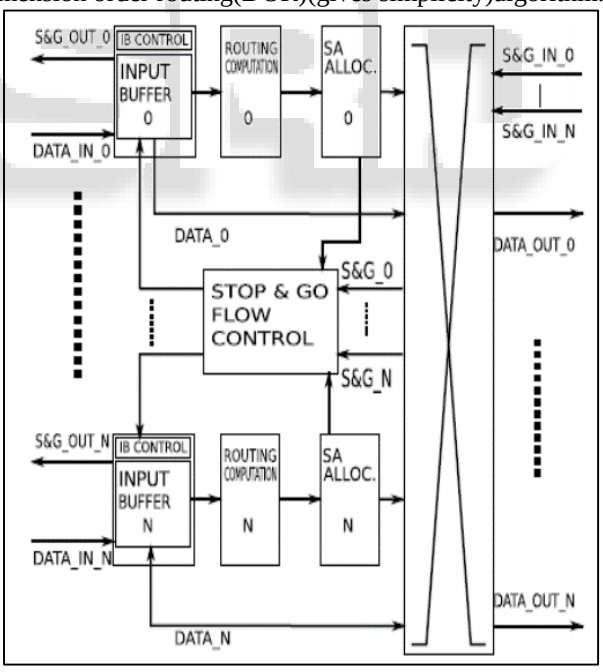

Fig. 3:

In this work they have proposed a new router design aimed to reduce the latency of the network. In particular, the arbiter complexity has been reduced. Multiple smaller arbiters are used in parallel and thus exhibiting a lower latency. In order to build a full operational router with such smaller arbiters new ports have been added to the router, and different internal connections in the router [20].

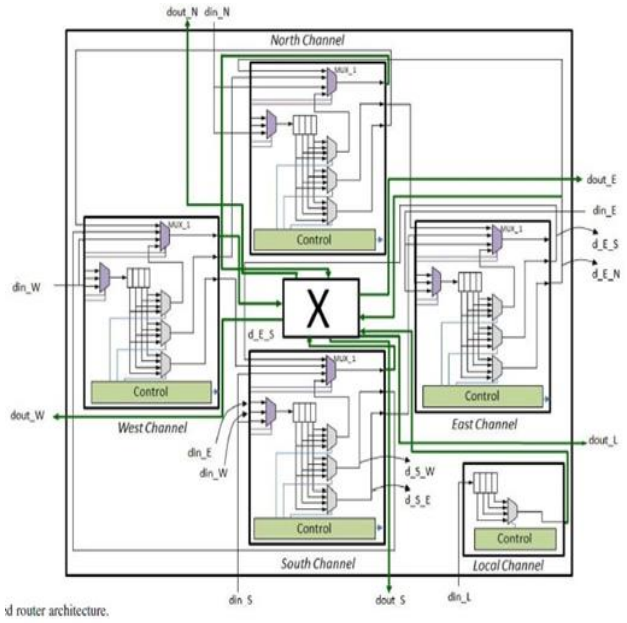

Fig. 4: Router architecture proposed by Matos [14].

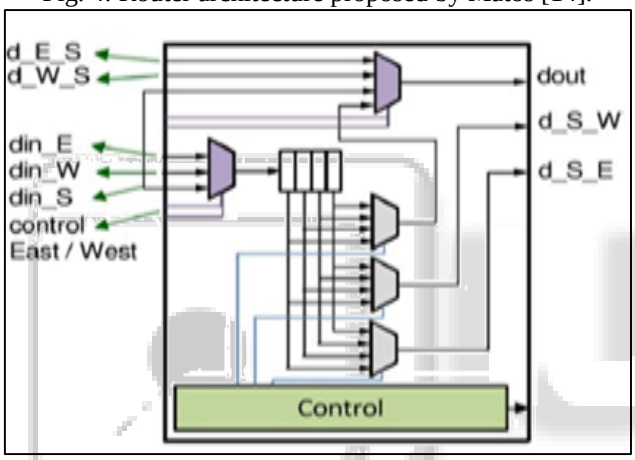

Fig. 5: Input FIFO in South Channel [14].

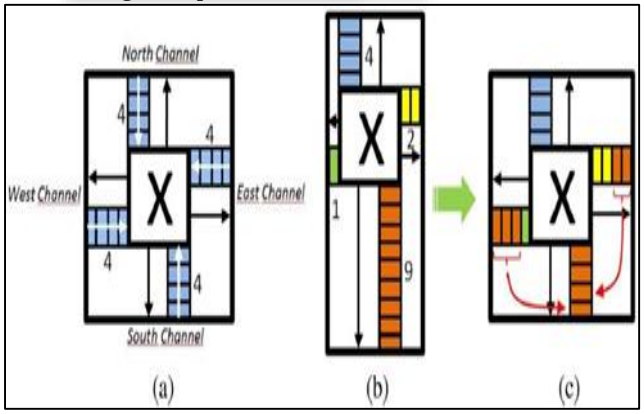

Fig. 6: Router designed with FIFO depth 4 (b) need of the router or according to need of data (c) Distribution of buffer words among the neighboring channel [14].

III. Conclusion

As per it has been already discussed that router is an important component of NoCs design. A modified work is showing in this paper on reconfigurable router for used in NoCs with objectives of low power consumption and high performance operation. The proposed router architecture consists of four channels (namely, east, west, north and south) and a crossbar switch. Each channel has First in First out (FIFO) buffers to store the data and multiplexers to control the input and output of data. Stack height of a FIFO buffer is considered to be four and stack width of FIFO is considered to be three. It means it has four locations and each location can three bit data. Each channel has five multiplexers. Two multiplexers are responsible to control the input and output of data and other three multiplexers are necessary to control read and write processes of FIFO. Verilog Hardware Description Language is used for the design entry of this router. For simulation and synthesis MODELSIM EDITION10.3 and XILINX ISE Design Suite 13.4 are used respectively. RTL view of architecture is shown by Xilinx ISE tool. The proposed reconfigurable router is synthesized using Xilinx SPARTAN-6 FPGAs. After Simulation and Synthesis of the proposed router architecture, total power is calculated with the help of XPower analyzer tool. The power gating technique is used to reduce the power dissipation of the proposed reconfigurable router. 5 mW power have been reduced after applying power gating technique in the proposed router architecture compared to the previous architecture.

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