A Review Paper on Booth Multiplier

Megha Jain[1] Pallavee Jaiswal[2]
[1,2]Dr. C.V. Raman University Bilaspur

Abstract— In this review paper different type of implementation of Booth Algorithm has been studied. In these algorithm, a multiplier is a fundamental arithmetic unit and used in a great extent in circuits. Multipliers are key components of many high performance systems such as FIR filters, Microprocessor, digital signal processors etc. Booth algorithm is used for design of multiplier but it suffers from some limitations like number of the partial products increases, so area and time delay also increases. In this review paper some techniques and algorithms are analyzed for design of multiplier in terms of delay, area and power consumption. All modules will be designed using VHDL and implemented on Xilinx FPGA development board.

Key words: FPGA, Multiplier, VLSI, Adders etc.

I. INTRODUCTION

As we know, based on theory of multiplication there are so many things that happens in backend which earlier was done by us manually in order to get the result. So, as there are so many processes causes so many phases and as it is automated in computing system, it ended up with so huge hardware resources as well. Considering the complexity of circuitry and huge hardware resources that caused the system execution/operating speed to be utterly slow which was then tried to be taken care of by presenting many ideas for over three decades. The major area of improvement which was under the consideration that time was the VLSI Operating Speed, Area and the Power Consumption in order to make it an efficient architecture. Though these three were under the attention, Speed was having high priority.

Basically as we know multiplication takes place in two steps, first one is producing and second one is adding. Now the speed of execution depends on how fast we are producing the products and how fast we are adding them together. Booth's Multiplier algorithm are meant to deal with the first one that is how fast it can produce the partial products to increase the operating speed. To achieve the second factor that is adding the products we need an architecture which can act as a fast adder. The performance of the system would have an impact of multiplier and in order to improve the performance many algorithms has come up with an architecture and some of them are used in Pipeline and Vector computers.

The multimedia and communication system are now using Digital Signal Processing(DSP) which is using the both high speed Booth multipliers and pipelined Booth multipliers to improve the speed. Now the challenge is the power and area as we have achieved the speed. Then after high speed DSP computation applications like Fast Fourier Transform came up with two requirements those were additions and multiplications. This absolute goal was achieved by using the conventional modified Booth encoding (MBE) which generates an irregular partial product array because of the extra partial product bit at the least significant bit position of each partial product row. This concept have low overhead with a simple approach to generate a regular partial product with fewer rows which ended up with lowering the complexity, reducing the area, delay and the power of MBE multipliers. The whole simulation is done using VHDL/Verilog HDL Modelism and XILINX ISE design tool is used to have it synthesized.

II. LITERATURE SURVEY

Akanksha Sharma, Akriti Srivastava, Anchal Agarwal, Divya Rana ,Sonali Bansal presented the best solution to the problem is determined by designing a high speed multiplier chiefly booth multiplier which reduces the number of flip flops and memory size in the design circuitry as compared to conventional serial multiplier. Then implementation of a calculator using booth multiplier and several other operational modules is done using codes written in VHDL language using ISE XILINX 6.1 and simulated in MODELSIM 5.4a.

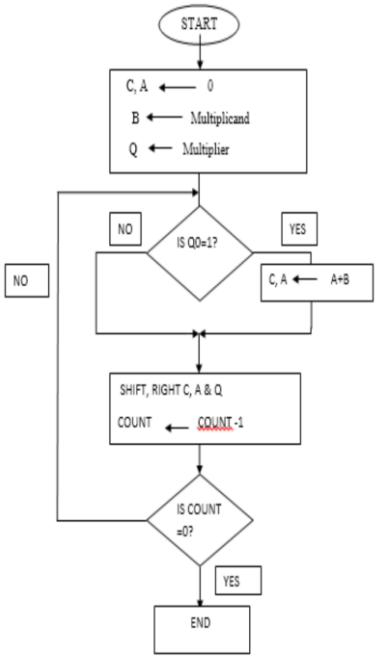

Fig. 1: Flowchart for booth's algorithm of unsigned number

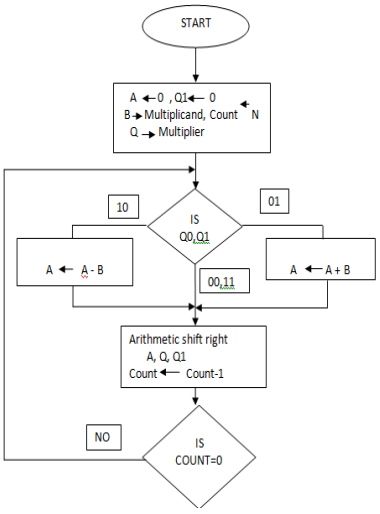

Fig. 2: Flowchart for booth's algorithm of signed number

It is seen from the Table 4 that no of multiplexers and adders Utilized in booth multiplier is less as compared to the serial Multiplier. So the objective of designing this multiplier is fulfilled as in large circuit design use of booth multiplier in place of serial multiplier considerably reduces the number of elements utilized in its design. Memory utilization of booth multiplier is less than that of serial multiplier i.e. for the case if booth reduces the memory usage by 2 % in a design of single gate so the reduction would be about of 10% in a large circuit design comprising of number of gates [1].

Sukhmeet Kaur, Suman and Manpreet Signh Manna describe implementation of radix-4 Modified Booth Multiplier and this implementation is compared with Radix-2 Booth Multiplier. Modified Booth's algorithm employs both addition and subtraction and also treats positive and negative operands uniformly. No special actions are required for negative numbers. In this Paper, we investigate the method of implementing the Parallel MAC with the smallest possible delay. Parallel MAC is frequently used in digital signal processing and video/graphics applications. A new architecture of multiplier - and accumulator (MAC) for high speed arithmetic by combining multiplication with accumulation and devising a carry-lookahead adder (CLA), the performance is improved. Modified Booth multiplication algorithm is designed using high speed adder. High speed adder is used to speed up the operation of Multiplication.

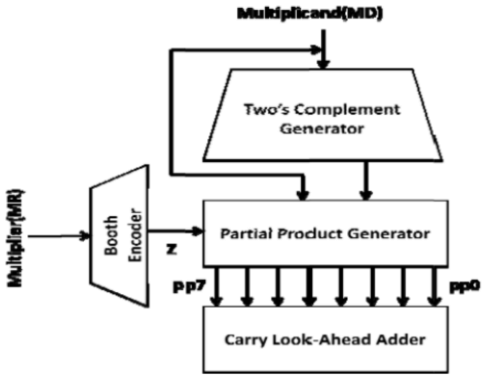

Fig. 3: Architecture of booth multiplier

Radix-2, 4 Booth Multipliers are implemented; the complete process of the implementation is giving higher speed of operation. The Speed and Circuit Complexity is compared, Radix-4 Booth Multiplier is giving higher speed as compared to Radix-2 Booth Multiplier and Circuit Complexity is also less as compared to it [2].

Neha Goyal, Khushboo Gupta, Renu Singla studied Low power consumption and smaller area are some of the most important criteria for the fabrication of DSP systems and high Performance systems. Optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas. In our project we try to determine the best solution to this problem by comparing a few multipliers.

The area and speed of the multiplier is an important issue, increment in speed results in large area consumption and vice versa. Multipliers play vital role in most of the high performance systems. Performance of a system depends to a great extent on the performance of multiplier thus multipliers should be fast and consume less area and hardware. This idea forced us to study and review about the Booth's Algorithm.

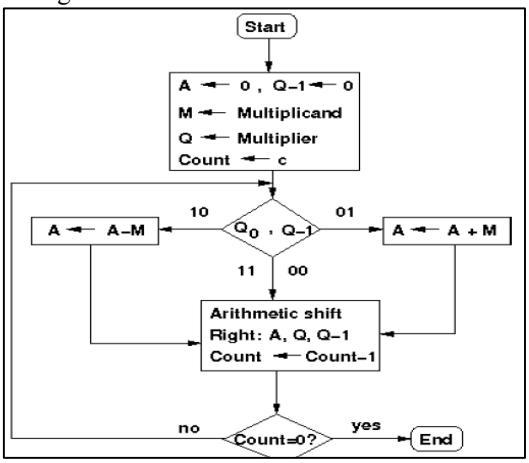

Fig. 4: Design flow of Booth algorithm

It can be concluded that Booth Multiplier is superior in respect like area, Complexity. In booth multiplier number of gates is reduced and hence area of booth multiplier is less than combinational multiplier. However Combinational Multiplier gives optimum number of components required. Hence for less delay requirement Booth's multiplier is suggested [3].

Udari Naresh, G.Ravi, K.Srinivasa Reddy, presents the design and implementation of Modified Booth encoding multiplier for both signed and unsigned 32 - bit numbers multiplication. The already existed Modified Booth Encoding multiplier and the Baugh-Wooley multiplier perform multiplication operation on signed numbers only. Whereas the array multiplier and Braun array multipliers perform multiplication operation on unsigned numbers only. Thus, the requirement of the modern computer system is a dedicated and very high speed unique Multiplier unit for signed and unsigned numbers. Therefore, this paper presents the design and implementation of SUMBE multiplier. The modified Booth Encoder circuit generates half the partial products in parallel. By extending sign bit of the operands and generating an additional partial product the SUMBE multiplier is obtained. The Carry Save Adder (CSA) tree and the final Carry Look ahead (CLA) adder used to speed up the multiplier operation. Since signed and unsigned multiplication operation is performed by the same multiplier unit the required hardware and the chip area reduces and this in turn reduces power dissipation and cost of a system.

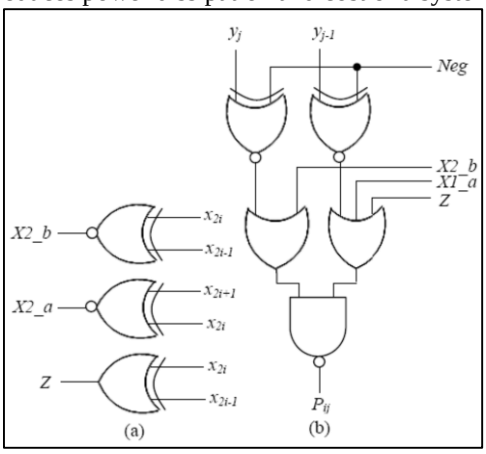

Fig. 5: The Encoder and Decoder for the new MBE scheme. (a) Simple encoder (b) Decoder.

In this work, they have presented a 32-bit multiplier capable of singed unsigned variable with carry out. In all multiplication operation product is obtained by adding partial products. The speed of the adder circuit is depending on the final speed of the multiplier although, then no. of partial product generated. If radix 8 Booth encoding technique is used then there are only 3 partial products and for that only one CSA and a CLA is required to produce the final product [4].

III. CONCLUSION

Here we have studied different multipliers and concluded that to perform better for a large binary number multiplication sequential multiplier better as compare to combinational multiplier with respect in speed and area. Booth multiplier is able to perform operation with low power consumption and area with higher speed at the different level of different technique. If the two booth multipliers and their characteristics in terms of multiplication speed, no of computations required, no of hardware is compared then it's results is shown that radix 4 booth multipliers is better than Radix-2 booth multipliers and also Radix -4 multiplier computation speed is higher than Radix-2 and Circuit Complexity is also less as compared to it. The simulation has been done by using VHDL/Verilog HDL Modelsim and synthesize has been done by using the XILINX ISE Design Tool.

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