An IIR Notch Filter Implementation on FPGA to Remove Power-Line Interference from ECG Signal

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Abstract— An Electrocardiogram (ECG) signal may be affected by different types of noises such as Power line interferences, Base line interferences and Electromyogram. For the accurate analysis of ECG signal these types of noises has to be removed. In this paper, we present a method to remove power line interference of 50Hz noise from an ECG signal. ECG signal is taken from MIT-BIH arrhythmia database. An IIR notch filter of cutoff frequency 50Hz is designed in Spartan6 FPGA for the removal of the power line interference noise

Key words: Electrocardiogram, Notch filter

I. INTRODUCTION

Electrocardiogram is a clinical tool for investigating various activities of heart. The activities are recorded in the form of waves which can be seen on monitor. Interpretation of these signals are of very importance since it diagnosis wide range of heart diseases. For a typical ECG acquisition system there will be an Analog Front End (AFE), Analog filters, a processor and a display unit. Generally, the ECG signals are processed by using any of the processors like Digital Signal Processors (DSP), Field Programmable Gate Array (FPGA) or ARM processors. While processing these ECG signals it may be corrupted by several noises such as Power line interference, Base line interferences and Electromyogram. Among all these noises power line interference noise of 50Hz is the worst kind of noise since it can destroy the ECG signal which has very low frequency of around 1Hz and these types of noise is due to the improper grounding of the ECG acquisition system as well as loose contacts on the patient cable or due to dirty electrode. So it must be removed from the ECG signal for the correct interpretation of the signal.

In order to remove this power line interference noise one can either use an analog filter or a digital filter. Digital filters are programmable and can be designed implemented and tested on a processor easily. Also digital filters are able to handle low frequency and since they do not have any analog components they are extremely stable. So we have designed an IIR Notch digital filter. IIR filters have lots of advantages over FIR filters and they require less number of calculations as well as less number of coefficients. Also IIR filters can be easily implemented on processors like FPGA.

II. PROPOSED FRAMEWORK

The proposed framework includes taking ECG signal from MIT-BIH Arrhythmia database, addition of 50Hz noise, designing of notch filter in matlab, converting matlab code in to Verilog code, simulating the model using Isim simulator and finally implementation of the notch filter in Spartan6 FPGA and verifying output on DSO.

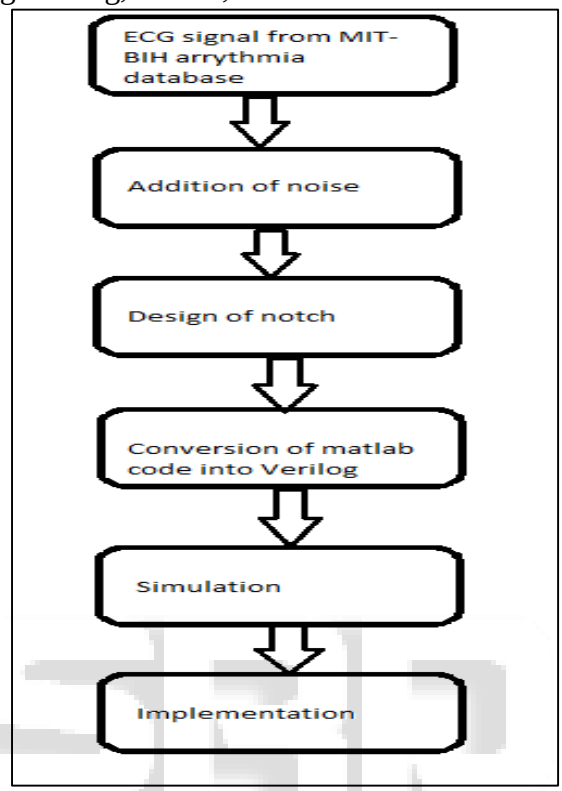

Fig. 1: Proposed Framework

Here a notch filter is used to filter the 50 Hz noise in ECG signal. ECG signal is taken from MIT-BIH arrhythmia database. The database which is in .dat format is converted to.mat format suitable for matlab implementation. From the complete ECG data only 9th row and complete 10000 columns are used as the input in matlab. Since the ECG signal taken from the MIT-BIH arrhythmia database is noise free a 50Hz noise is added to the input ECG signal. In real world case this 50 Hz noise is because of the power line interference which will make the recorded ECG signal impossible to analyze.

Then a notch filter is designed in matlab. We have taken IIR digital filter design for the notch filter. So in order to design the notch filter first we need the coefficients of the notch filter. The coefficients are designed using the matlab function [b,a] = iirnotch(Wo,BW). Here sampling frequency is taken as 1000 Hz and central frequency as 50 Hz. The magnitude response of the notch filter is seen by filter visualization tool. After that the notch filter is implemented by Direct form II Transposed Structure. This structure can be implemented directly in matlab using y=filter(b,a,x), where b and a are the filter coefficients and x is the input ECG signal. The ouput is checked and it doesn't contain any noise and is perfect ECG.

After the matlab implementation, the matlab code is converted in to a code accessible by Xilinx Spartan6. To implement in FPGA board first COE file of the noise added

ECG is taken from the matlab. Since FPGA board has memory limitations only 750 samples of ECG is taken. These values are stored in block memory as 8-bit data. Now the coefficients generated from matlab must be converted in to fixed point numbers that can be processed by FPGA board. So 10 bit representations of coefficients are used where 8 bits are the fractional part and 2 bits are the integer part. After simulation the design is synthesized using Xilinx Synthesis Tool (XST) and finally downloaded on chip. An R-2R Digital to Analog Converter (DAC) is used to convert the digital values in to analog representation and output is verified on DSO.

III. MATLAB IMPLEMENTATION

The filter coefficients are directly implemented using matlab second order IIR notch filter coefficient design. Transposed direct form II structure is used for the design. The notch filter is designed for a centre frequency of 50 Hz.
The filter coefficient values obtained are

b= [1 1.9022 1]

a= [1 1.8072 0.9025]

Then the ECG signal which is taken from MIT-BIH arrhythmia database in .dat format is converted to .mat format, suitable for matlab implementation. From the complete ECG data only 9th row and complete 10000 columns are used as the input in matlab. Since the ECG signal taken from the MIT-BIH arrhythmia database is noise free a 50Hz noise is added to the input ECG signal. In real world case this 50 Hz noise is because of the power line interference which will make the recorded ECG signal impossible to analyze.

Fig. 2 shows three different waveforms. First graph shows the ECG signal taken from MIT-BIH database which doesn't contain any noise. The second graph shows the 50Hz noise added ECG signal and the third graph shows the noise removed ECG signal output.

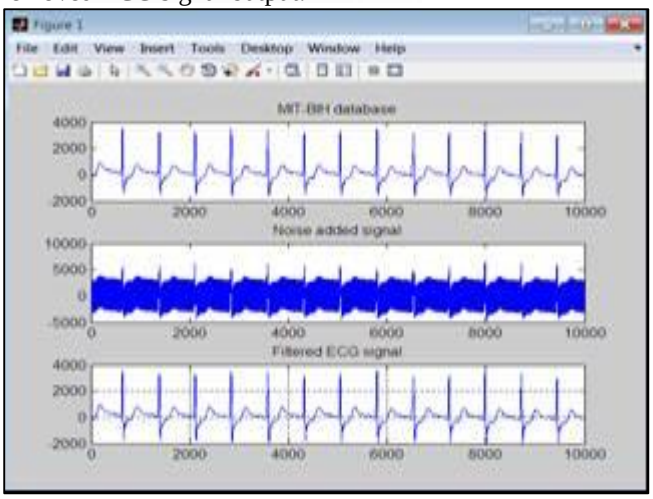

Fig. 2: Matlab Implementation

IV. FPGA IMPLEMENTATION

Since Spartan6 fpga has limited memory only 750 samples are selected from the 10000 samples. These 750 ECG samples are stored in the block memory of FPGA. A 10 bit address is used to select these values. The notch filter is implemented on FPGA by using mainly 3 modules. First module is the Clock generation module which creates 60 MHz clock for the working of Spartan 6 FPGA. Second module consists of wave generation which creates input ECG signal. Third block is the Filter module in which IIR Notch filter is implemented. All these modules are combined in Top Module.

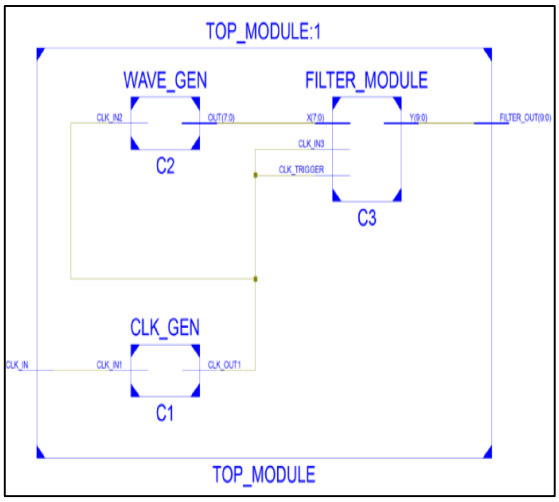

Fig. 3: RTL Schematic

The overall device utilisation summary is given below

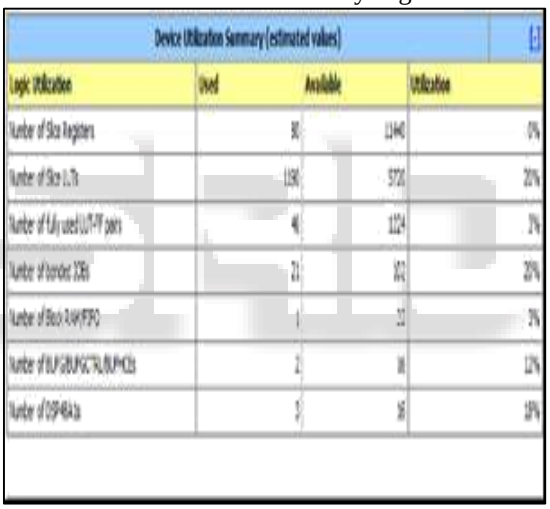

Fig. 4: Device utilisation summary

V. RESULTS

Fig. 5 shows the output of the noise added ECG signal as well as noise removed ECG signal displayed on DSO. An R-2R ladder is used to convert the digital output of the Spartan6 FPGA to analog output so that the output can be displayed on DSO.

Fig. 5: Input and Output displayed on DSO

VI. CONCLUSION

This work has proposed a novel method for removing 50Hz power line interference noise in ECG signal. An IIR Notch filter is designed in Matlab with a central frequency of 50Hz. Then the matlab code is converted in to Verilog code and the filter is implemented in Spartan6 FPGA board. A 10-bit R-2R DAC is used to convert the digital output in to analog output which can be seen on Digital Storage Oscilloscope (DSO).

REFERENCES

[1] Chun Mei WANG, ``Second Order IIR Notch FilterDesign and Implementation of digital signal processing system,'' Proceedings of the 2nd InternationalSymposium on Computer, Communication, Control and Automation (ISCCCA-13).
[2] Rajesh Kumar, Dr. Pankaj rai, Amit kumar, "Design & Analysis of IIR notch filter using bandwidth Parameter," International Journal of Innovative Research in Advanced Engineering (IJIRAE) ISSN: 2349-2163, Volume 1 Issue 8 (September 2014).
[3] Apurva Singh Chauhan, "Hardware Implementation of DSP Filters On FPGA," International Journal of Computer Applications (0975 – 8887) Volume 62– No.16, January 2013.
[4] Chi-Jui Chou, Satish Mohanakrishnan, Joseph B. Evans, "FPGA Implementation OF Digital Filters," Department of Electrical & Computer Engineering, University of Kansas, Lawrence, KS 66045-2228.
[5] P. R. Cappello, editor. VLSI Signal Processing. IEEE Press, 1984.
[6] Ray Goslin, Dr. San Jose, CA 95124 A Guide to Using Field Programmable Gate Arrays (FPGAs) for Application-Specific Digital Signal Processing Performance Gregory Digital Signal Processing Program Manager Xilinx, Inc. 2100 Logic
[7] Mark S. Manalo and Ashkan Ashrafi "Implementing Filters on FPGAs" Department of Electrical and Computer Engineering Real-Time DSP and FPGA Development Lab
[8] Spartan-6 FPGA Data Sheet, DS162 (v3.1.1) January 30, 2015

