Design of Low Power Area Efficient Pulsed Latches based Shift Register

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Abstract— The timing elements and clock interconnection Networks such as flip-flops and latches, is One of the most power consuming components in modern very large Scale integration (VLSI) system. The area, power and transistor count will compared and designed using several latches and flip flop stages. Flip Flop is a circuit which is used to store state information. Power consumption is one of the main objectives in designing a flip flop. The flip flops used in designing are Hybrid Latch Flip Flop (HLFF), explicit-pulsed data-close-to-output flip-flop (ep-DCO) and Adaptive-Coupling Redundant Flip-Flop (ACFF). Compare pulse triggered latches based on transistor count, power and layout area. Constructing shift registers by using conditional capture pulsed latches instead of normal flipflops, because a pulsed latch is much smaller than a flip-flop. All the latches and flip flop designs are made by using 90nm technology in DSCH2 schematic tool and MICROWIND design tool.

Key words: Pulse Triggered Latches, Flip Flop, Shift Register, Micro Wind

I. INTRODUCTION

In VLSI design power consumption has become a very important issue. Sequential logic circuits, such as registers, memory elements, counters etc., are heavily used in the implementation of Very Large Scale Integrated (VLSI) circuits. Power dissipation is critical for battery-operated systems, such as laptops, calculators, cell phones and MP3 players since it determines the battery life. Therefore, designs are needed that can consume less power while maintaining comparable performance. Flip-flop is a data storage element. The operation of the flip-flops is done by its clock frequency. When multistage Flip-Flop is operated with respect to clock frequency, it processes with high clock switching activity and then increases time latency. Therefore it affects the speed and energy performance of the circuit. Various classes of flip-flops have been proposed to achieve high-speed and low-energy operation. In the past decades, many works has been dedicated to improve the performance of the flip-flops.

II. D FLIP FLOP

The D Flip Flop is widely used. It is also known as a data or delay flip-flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change.

The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line. The "D flip flop" will store and output whatever logic level is applied to its data terminal so long as the clock input is HIGH. Once the clock input goes LOW the "set" and "reset" inputs of the flip-flop are both held at logic level "1" so it will not change state and store whatever data was present on its output before the clock transition occurred. In other words the output is "latched" at either logic "0" or logic "1".

III. FLIP FLOP

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design. The requirements of designing a flip flop are as follows.

A. Pulse-Triggered Flip-Flops

Pulse-triggered flip-flops can be classified into two types, implicit and explicit, and this classification is due to the pulse generators they use. In implicit-pulse triggered flip-flops (ip-FF), the pulse is generated inside the flip-flop, for example, hybrid latch flip-flip (HLFF), semi-dynamic flip-flop (SDFF), and implicit-pulsed data-close-to-output flip-flop (ip-DCO). Whereas, in explicit-pulse triggered flip-flops (ep-FF), the pulse is generated externally, for example, explicit- pulsed data-close-to-output flip-flop (ep-DCO) and the flip-flops.

At first glance, ep-FF consumes more energy due to the explicit pulse generator. However, ep-FF has several advantages. First, ep-FF can have the pulse generator shared by neighboring flip-flops, a technique that is not straightforward to use in ip-FF. This sharing can help in distributing the power overhead of the pulse generator across many ep-FF, and a system using ep-FF will be more energy efficient than a system using ip-FF.

Second, double-edge triggering is straightforward to implement in ep-FF, but it is difficult to deploy in ip-FF. Using double-edge triggering, where data latching or sampling is issued at both the rising and falling edges, usually allows the clock routing network to consume less power.

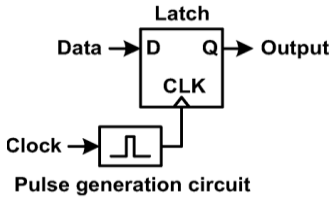

Fig. 1: Pulsed Latch

For example, for a system with a throughput of one operation per cycle and a clock frequency, double-edge triggering results in two operations being executed in one cycle; if we use half the frequency, we can maintain the same throughput of the original system. With half the frequency, the clock switching activity is reduced by half,

which leads to considerable power savings in the clock routing network. Third, ep-FF could have the advantage of better performance as the height of the NMOS stack in ep-FF is less than that in ip-FF. With this rationale, the authors believe that ep-FF topology is more suited for low-power and high-performance designs.

B. Explicit pulsed Data Close to out (Ep-DCO)

The schematic for the ep-dco flip-flop; its semi-dynamic structure consists of two stages: a dynamic (first stage) and a static stage (second). After the rising edge of the clock, transistors N2 and N3 turn on for a short period of time, which is equal to the delay incurred by the pulse generator. During this period, the flip-flop is transparent and the input data propagates to the output. After the transparent period, the pull-down paths in both stages are turned off via the same transistors N2 and N3. Hence any change at the input cannot pass to the output. Keepers are used to maintain the output and internal node states when the circuit is in the hold mode. Figure 2 shows the explicit pulsed data close to out. .

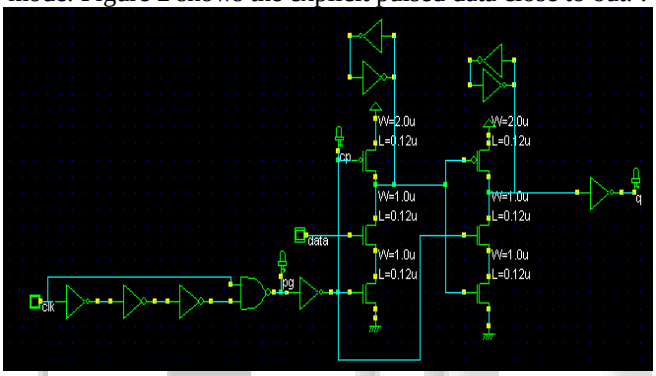

Fig. 2: Explicit pulse Data Close to out

C. Transmission Gate Flip Flop Design

The basis of the operation is that the two transmission gates operate alternatively. This is obvious if one looks at the way the enable input is connected to them: EN is connected to the n type transistor of the upper gate, while it is connected to the p type transistor in the lower one. Thus when EN falls to 0, the transmission gate at the input of the latch cuts off and separates the input from the output. At the same moment, the other gate in the feedback branch starts to conduct and will connect the output to the input of the first inverter. This is a stable circuit where the input capacitance of the inverters holds the information.

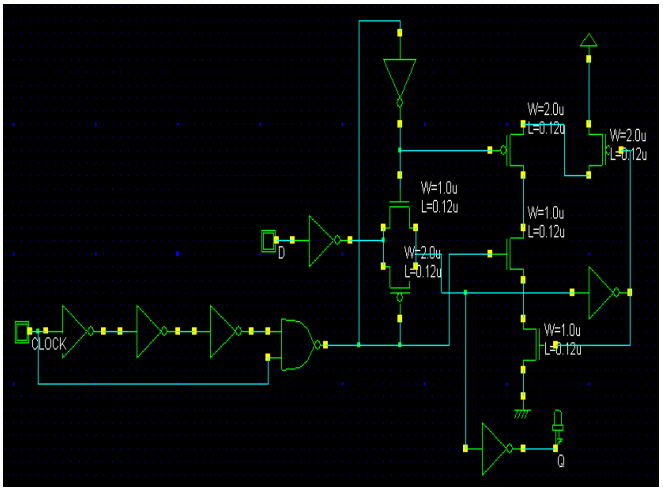

Fig. 3: Transmission Gate Flip Flop Design

D. Adaptive Coupling Redundant Flip Flop Design

It operates with the single-phase clocking scheme using pass-transistors. Without using local clock buffers, power dissipation can be reduced. As data activity becomes low, total power dissipation is drastically reduced. However, PMOS pass-transistors are too weak to pass through a substantially large drain current. It is difficult to overwrite the master latch because PMOS pass-transistors are located in front of the master latch. The Adaptive-Coupled (AC) two transistors make it easy to overwrite the master latch. When the next value is same as the current value, the cross-coupled loop keeps the current value. When it is different, the AC makes the holding value weak. The number of transistors of ACFF is fewer by two transistors than the transmission-gate (TG) FF.

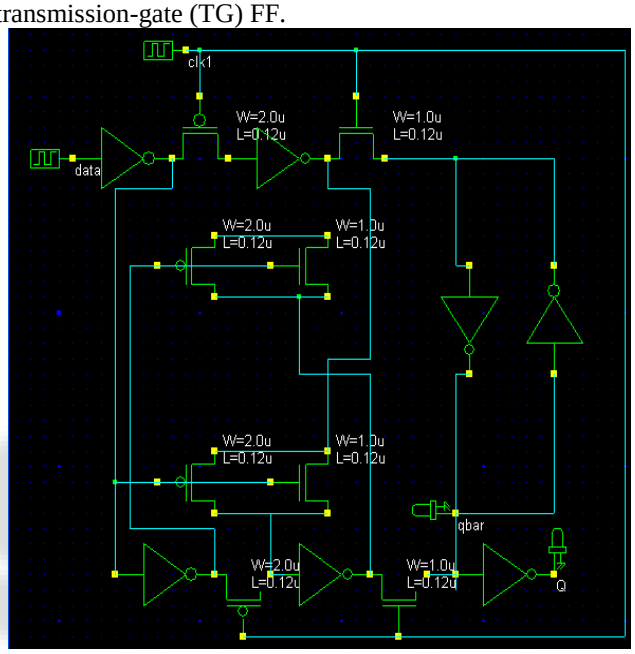

Fig. 3: Adaptive coupling Redundant Flip flop

All these hard-edged flip-flops are characterized by positive setup time, causing large -to- delays. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. The logic complexity and number of stages inside these pulse-triggered flip-flops are reduced, leading to small -to- delays. One of the main advantages of pulse-triggered flip-flops is that they allow time borrowing across cycle boundaries as a result of the zero or even negative setup time.

E. Adaptive Coupling Redundant Flip Flop Design

The SSASPL (static differential sense amp shared pulse latch) in Fig. 4, which is the smallest latch, is selected. The original SSASPL with 9 transistors is modified and selected to design .In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch.

The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal. The SSASPL updates the data with three NMOS transistors and it holds the data with four transistors in two cross-coupled inverters. It requires two differential data inputs (D and Db) and a pulsed clock signal. When the pulsed clock signal is high, its data is updated. The node Q or Qb is pulled down to ground according to the input data

(D and Db). The pull-down current of the NMOS transistors must be larger than the pull-up current of the PMOS transistors in the inverters.

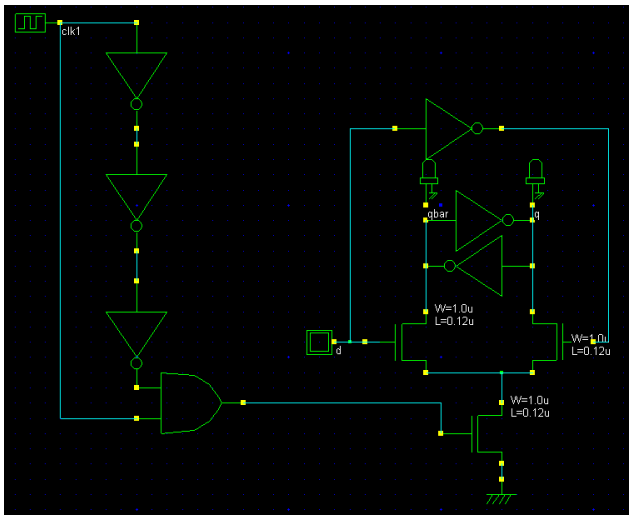

Fig. 4: Static differential sense amp shared pulse latch

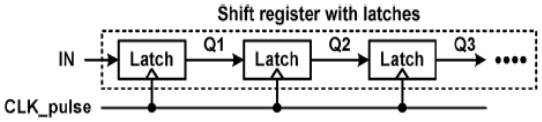

Fig. 5: Shift register using Latches

The shift register in Fig. 5 consists of several latches and a pulsed clock signal (CLK_pulse).

The operation shows the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signals of the first latch (IN) is constant during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

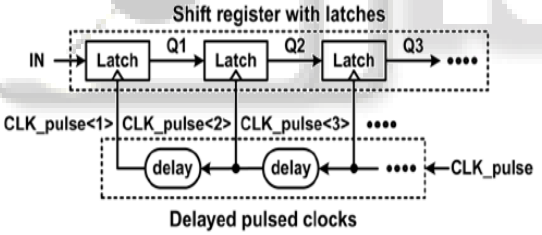

Fig. 6: Shift register with delayed clocked Latches

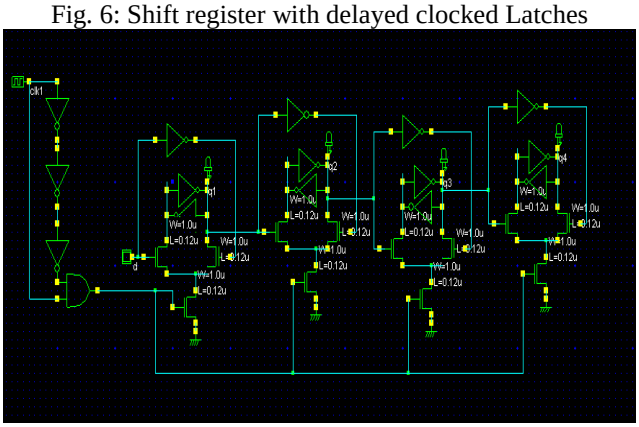

Fig. 7: Shift register design using SSASPL

However, the delay circuits cause large area and power overheads, Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 4(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits.

The several flip flop designs and latches are designed and 4 bit shift register is designed using Static differential sense amp shared pulse latch.

IV. Results and Discussion

The input Data (d), with respect to clock pulse is processed by D flip flop with various latches is designed and its results are shown here. The result shows the data to Q delay and power consumed.

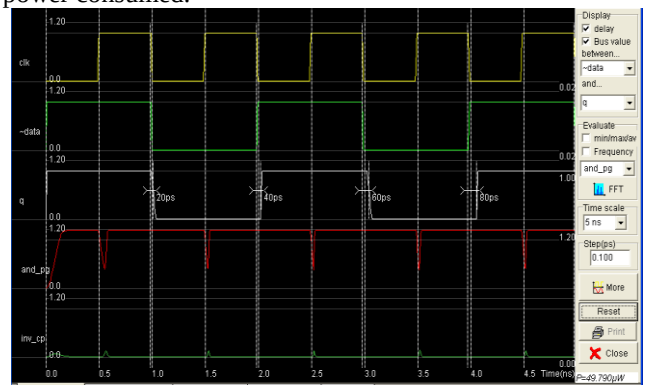

Fig. 8: Explicit pulse triggered data close to out

Explicit pulse triggered data close to out is designed with a data to Q delay and power which is consumed is given as 20ps and as 49.790 µw indicated in waveform.

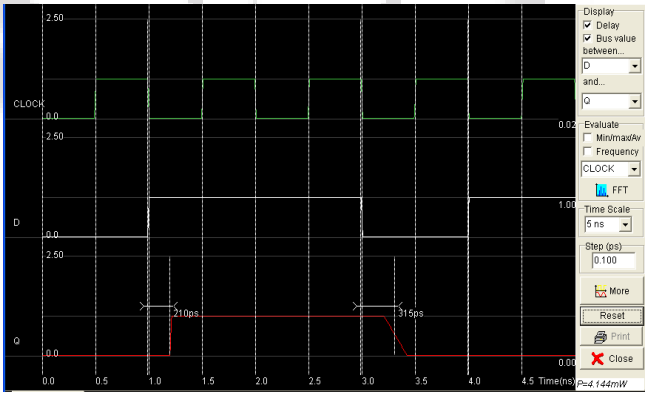

Fig. 9: Transmission gate flip flop design result

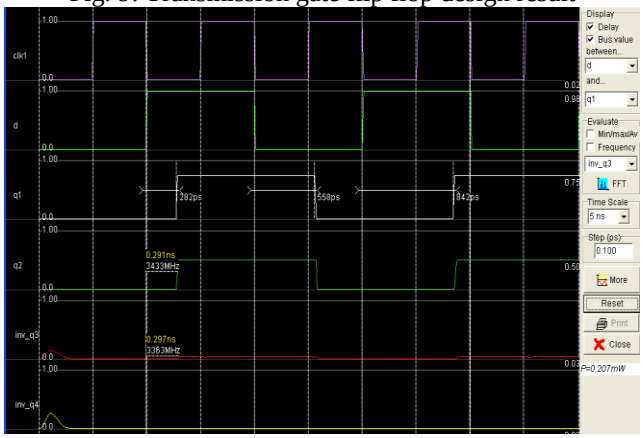

Fig. 10: Proposed4 bit shift register design result

Table I show the transistor comparison of pulsed latches and flip-flops. The transmission gate pulsed latch

(TGPL), hybrid latch flip-flop (HLFF) , conditional push-pull pulsed latch (CP3L), Power-PC-style flip-flop (PPCFF), Strong-ARM flip-flop (SAFF), data mapping flip-flop (DMFF), conditional pre-charge sense-amplifier flip-flop (CPSAFF), conditional capture flip-flop (CCFF), adaptive-coupling flip-flop (ACFF) are compared with the SSASPL used in the proposed shift-register.

Flip flop	Transistor count	Data to Q delay	Power	Power delay product
Ep-DCO	28	20ps	49.790µw	980
TGFF	24	210ps	04.14mw	860
ACFF	22	1041ps	18.781µw	18783
SSASPL	21	600ps	1.076mw	650

Table 1: Performance comparisons

V. CONCLUSION

The pulse Triggered concept is implemented in flip flops such as Transmission gate flip flop-TGFF, Hybrid latch flip flop, CCFF, Explicit pulse-Data Close to Out and Adaptive-Coupling Redundant Flip-Flop for power consumption. Using these flip flop design comparison CCFF is considered and it is used to design Shift Registers with delay element and without delay element were designed. Thus different flip flop structures can be used for different applications considering the parameters such as power, gate count and delay. The shift registers were designed by Conditional capture flip flop design; the logics were constructed and verified.

VI. FUTURE ENHANCEMENT

There are many other different techniques available to reduce the power consumption in the flip flops such as Low swing Voltage, Conditional operation, Clock gating etc. And power consumption can be reduced by using low swing voltage approach. If supply voltage is halved the switching activity of the transistor will be reduced leads power reduction. Then transistor scaling or layout optimization is another way to reduce power consumption.

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