A Novel Power Efficient Reversible Asynchronous Counter

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Abstract— Due to the high density of the chip, the power dissipation increases. So we are in the need of the best power optimization techniques. Reversible logic is the one which is used to optimize the power getting wasted. Reversible logic finds its applications in the field of low power CMOS designs, quantum computing, nanotechnology and optical computing. There are number of circuits designed by Reversible logic and possess their own importance in the digital world In this paper we have proposed a new reversible T-Flip flop using a newly proposed RHR(Raju Hazar Rahul) Gate. It is also shown that the proposed one is better than the existing one. Using the proposed design we also have implemented the counters which owns many advantages compared to the existing one.

Key words: Reversible Logic, Counter, RHG Gate,T-Flipflop.

I. INTRODUCTION

Reversible logic circuit synthesis is an introduction to design of quantum computing-based systems, low power CMOS circuits, and nanotechnology-based systems. Since quantum mechanics is essentially reversible, quantum mechanical processes appeared as good candidate to construct reversible gates and these gates are known as quantum gates [1]. After introduction of the idea of quantum computation it has already been seen that there exist some quantum algorithms [2] which work much faster than their classical counterparts, and these processes which establish quantum computing as a superior future technology involves quantum circuits and quantum gates. As quantum algorithms, quantum gates are more powerful than classical reversible gates [2]. There are some 3x3 classical reversible gates, provided constant inputs are permitted [3,4]. On the other hand, major of quantum 2*2 gates are universal, without needing the constant inputs [1].

A. Basic Definitions

1) Reversible Function:

A function is said reversible if, given its output, it is always possible to determine back its input, which is the case when there is a one-to-one relationship between input and output states[3].

2) Reversible Logic Gate:

The logic gate which satisfies the reversible function is termed as reversible logic gates. Here always the number of inputs goes equal to the number of outputs.[4] It not only determines input from the output but also vice versa.

3) Ancilla Input:

The unwanted or unused input in the gate or the circuit is known as Ancilla Input

4) Garbage Output:

The unwanted outputs in gate or circuit. Basically it is made used to attain the state of reversibility.

In reversible logic we have one more factor, which is more important than the number of gates used, namely the number of garbage outputs. The unutilized outputs from a reversible gate/circuit are called "garbage". Though every synthesis method engages them producing less number of garbage outputs, but sometimes garbage outputs are unavoidable. For example, a single output function of n variables will require at least n-1 garbage outputs, since the reversibility necessitates an equal number of outputs and inputs. Reversible logic imposes many design constraints that need to be either ensured or optimized for implementing any particular Boolean functions.

The following criteria must be maintained in designing a reversible gate.

1) In reversible logic circuit the number of inputs must be equal to the number of outputs.
2) For each input pattern there must be a unique output pattern.
3) Each output will be used only once, that is, no fan out is allowed.
4) The resulting circuit must be acyclic.

B. Problems Of Reversibility: [5]

1) However, in order to attain the supposed benefits of reversible computation, the reversible machine must actually be run backwards to attain its original state. If this step is not taken, then typically the machine becomes clogged up with digital heat i.e. entropy, and is thus rendered unable to perform further useful work.
2) Another problem is that you must make sure your computation was perfomed with no errors - otherwise chaos (and not the original starting condition) may result when the machine is run backwards.
3) Without running a reversible machine backwards, the main benefits of using reversible logic - namely dramatically reduced heat dissipation and power consumption - cannot be realized in a sustainable fashion.

C. Application

The potential application areas of reversible computing include the following

1) Nanocomputing
2) Bio Molecular Computations
3) Laptop/Handheld/Wearable Computers
4) Spacecraft
5) Implanted Medical Devices
6) Wallet “smart cards”
7) “ Smart tags” on inventory

II. LITERATURE SURVEY

A. Two Input Feynman Gate

Feynman gate can be implemented using two MZI based all optical switch, two beam combiner (BC) and two beam splitter (BS) in all optical reversible computing. As the beam combiner (BC) simply combines the optical beams while the beam splitter simply splits the beams into two optical beams, hence researchers do not consider them in the optical cost and the delay calculations [6]. The block diagram of the Feynman

gate is shown below. As the Feynman gate can be implemented using two MZI based optical switches thus the optical cost of Feynman gate is considered as 2

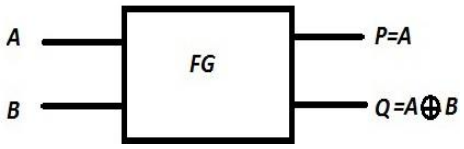

Fig. 1: Block diagram of 3 input Feynman gate

B. Three Input Feynman Gate

The Feynman gate (FG) is a 3 inputs and 3 outputs reversible gate. It has the mapping (A,B,C)to (P=A, Q=A B,Q= A C) where A, B and C are the inputs and P, Q and R are the outputs respectively.[12]

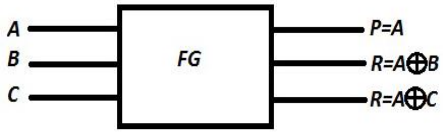

Fig. 2: Block diagram of 3 input Feynman gate

C. Universal ALL GATE

The 4*4 reversible ALL Gate performs all the Basic Logical Operations like AND, OR,NOT, NAND,EXOR, EXNOR. The inputs and the outputs are A,B,C,D and P,Q,R,S respectively. The reversible ALL Gate[13] is used to design all the logical operations as we have all the basic gates in the ALL Gate. The outputs of the ALL gate are as follows,

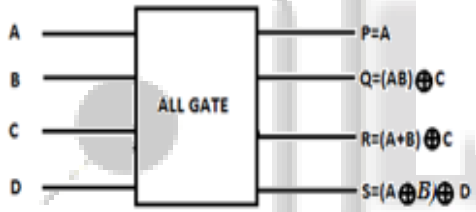

Fig. 3: Block diagram of ALL GATE

D. Garbage Less Gate (Glg)

The GLG Gate is a 4 x 4 reversible gate. The inputs and the outputs be A,B,C,D and P,Q,R,S respectively. It performs the Decoder.

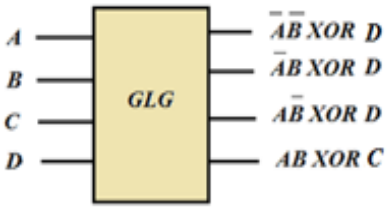

Fig. 4: Block Diagram of the GLG Gate

III. T FLIP-FLOP

If the T input is high, the T flip-flop changes state ("toggles") whenever the clock input is strobed. If the T input is low, the flip-flop holds the previous value. This behavior is described by the characteristic equation [6] (expanding the XOR operator)

$$Q_{next} = T \oplus Q = T\overline{Q} + \overline{T}Q$$

(expanding the XOR operator)

When T is held high, the toggle flip-flop divides the clock frequency by two; that is, if clock frequency is 4 MHz, the output frequency obtained from the flip-flop will be 2 MHz. This "divide by" feature has application in various types of digital counters. A T flip-flop can also be built using a JK flip-flop (J & K pins are connected together and act as T) or a D flip-flop (T input XOR Qprevious drives the D input).

A. Excitation Table

Q	Q_{next}	T	Comment
0	0	0	No change
1	1	0	No change
0	1	1	Complement
1	0	1	Complement

B. Characteristic Table

T	Q	Q_{next}	Comment
0	0	0	hold state (no clk)
0	1	1	hold state (no clk)
1	0	1	Toggle
1	1	0	Toggle

IV. PROPOSED WORK

A. Introduction To The RHR (Raju Hazar Rahul) Gate

The proposed RHR (Raju Hazar Rahul) Gate is a 4 x 4 reversible gate. The inputs and the outputs be A,B,C,D and P,Q,R,S respectively.

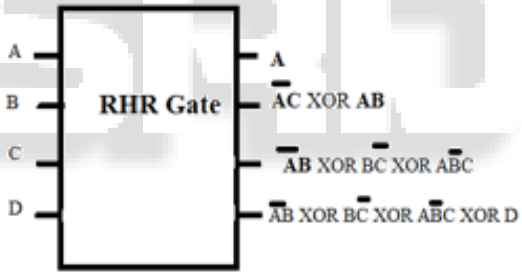

Fig. 5: Block Diagram of the RHR Gate

The truth table of the proposed RHR Gate is given below

INPUT				**OUTPUT**			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	1	0	0
0	0	1	1	0	1	0	1
0	1	0	0	0	0	1	1
0	1	0	1	0	0	1	0
0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1

1	0	1	1	1	0	1	0
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	0	0
1	1	1	1	1	1	0	1

From the truth table it is clearly inferred that the proposed RHR (Raju Hazar Rahul) is perfectly reversible as it is one to one mapping.

The proposed reversible RHR (Raju Hazar Rahul) Gate is used to design reversible T Flip flop. The main advantage of the proposed RHR (Raju Hazar Rahul) Gate is that with the only one single gate the T flip flop is performed. The existing uses many gates to implement theT flipflop. The comparison between this and the existing one is also proposed over here

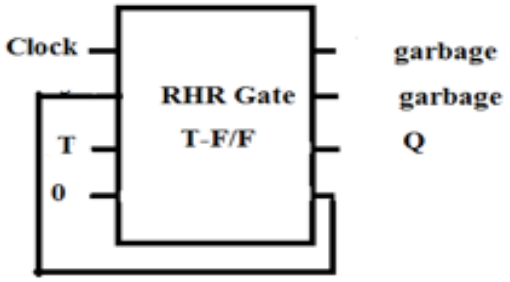

Fig. 6: Proposed T Flip flop using RHR Gate

B. Positive Edge Triggered T Flipflop

Clock	T	Q_{n+1}	Q
0	0	0	0
1	0	0	0
0	0	1	1
1	0	1	1
0	1	0	0
1	1	0	1
0	1	1	1
1	1	1	0

The comparison between the existing T-flipflops and the proposed one is given over here.

S.No	Particulars	Gate Count	Garbage OP	Constant IP
1	Existing [7]	10	12	10
2	Existing [8]	10	10	10
3	Existing [9]	5	3	2
4	Existing [10]	5	3	2
5	Existing [11]	3	3	2
6	Proposed	1	2	1

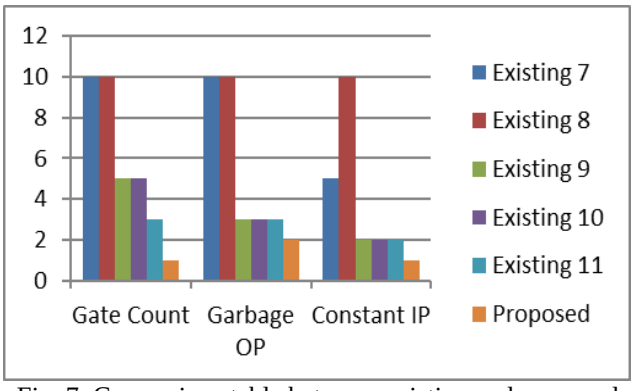

Fig. 7: Comparison table between existing and proposed

V. COUNTER IMPLEMENTATION

A. Asynchronous Down Counter

The proposed reversible asynchronous counter consists of 7 gates which is the advantage compared to the existing one. The architecture consists of 4 RHR GATE (Raju Hazar Rahul) which acts as the T Flip flop also two 2 Input Feynman Gate. The Enable pin is given commonly to all the Flip flops which is implemented using the proposed RHR GATE(Raju Hazar Rahul) Gate. The Q port is connected to the first input port of the Feynman gate. '0' is supplied to the second input terminal of the Feynman Gate.

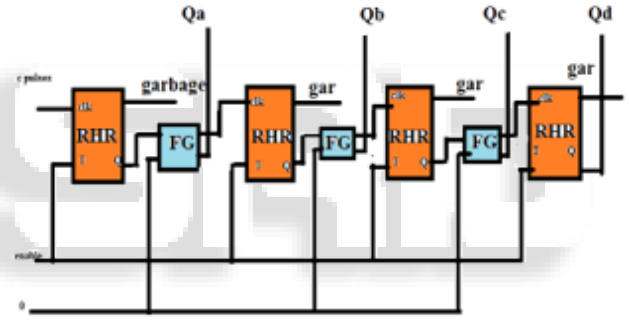

Fig. 8: Block Diagram of the asynchronous down counter

The first output port is connected is given as the Clock pulses of the proposed RHR(Raju Hazar Rahul) Gate. Similarly the outputs are taken correspondingly as shown in the figure.

S.No	Particulars	Gate Count	Garbage OP	Constant IP
1	Existing [11]	15	12	11
2	Proposed	7	4	3

Comparison table between existing and proposed

B. Asynchronous Up Counter

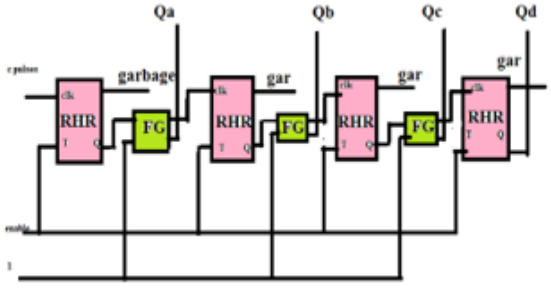

Fig. 9: Block Diagram of the asynchronous up counter

The proposed reversible asynchronous counter consists of 7 gates which is the advantage compared to the existing one. The architecture consists of 4 RHR (Raju Hazar Rahul) GATE which acts as the T Flip flop also two 2 Input Feynman Gate. The Enable pin is given commonly to all the Flip flops which is implemented using the proposed RHR (Raju Hazar Rahul) GATE. The Q port is connected to the first input port of the Feynman gate. '1' is supplied to the second input terminal of the Feynman Gate. The first output port is connected is given as the Clock pulses of the proposed RHR(Raju Hazar Rahul) Gate. Similarly the outputs are taken correspondingly as shown in the figure

VI. CONCLUSION

In this article, a method of asynchronous counter design from the proposed reversible RHR gates is presented. This paves an important role construct complex reversible sequential circuits using the reversible logic gates. Hence we can reduce the power consumption and improve application in various fields.

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