Power Reduction for Pulse Triggered Flip Flop using Sleep Transistor

S.Jagadeesh kumar[1] G.Balakrishna[2]
[1]P.G. Scholar [2]Assistant Professor & HOD
[1,2]Department of Electronics & Communication Engineering
[1,2]Sreenivasa Institute of Technology and Management Studies, Chittor, India

Abstract— The flip flop technologies is an essential importance design of VLSI design circuits for low power ,high speed and high performance .In this thesis used low power flip flop is designed by pulse generator and latch ,low power flip flop design featuring explicit type pulse triggered flip flop structure and a modified true single phase clock depends on a signal feed through logic is presented .It is need to reduce power dissipation in both clock distribution and flip flop .Here some kinds of pulse triggered was designed, the proposed design improves discharging problem and dynamic and leakage power using sleep transistor technology and achieve better speed and power than convectional flip flop.

Key words: Pulse Triggered Flip Flop, Low Power, Flip Flop

I. INTRODUCTION

Flip flop(FF) are the critical components in sequential digital logic circuits**,** it consist of a FF rich module such as register file, stack, queue, and first in first out **.**flip flops having main three timing parameters associated with flip flop that is setuptime, holdtime, propagation delay setup time (TD-C), hold time (Thold) and propagation delay (TC-Q). The input (D) must valid before the clock triggering edge and TD-C is the time difference between input (D) and clock. Thold is the time that the input (D) must remain valid after the clock edge. TC-Q is the time difference between the output (Q) and the clock edge. Assuming Thold is met, the delay of a flip-flop can be express the time difference between input (D) and output (Q).It is also estimated that power consumption of clock system, which consist of a clock distribution networks and storage elements is as high as 50%of the total system power .the clock system composed having a interconnection and also timing elements, is one of the most power consuming components in sequential digital circuits. So reduce the clock interconnection power as a result reduces power consumed by the clock will deep impact on the total system power.

A flip flop can be designed as a latch pair, where one is transparent high, and other is transparent low. The transmission gate flip flop with input gate isolation (TGFF).Pulse triggered flip flop where the first stage is a pulse generator and the second stage is a latch. Low power pulse triggered flip flop consumes low power compare to remaining flip flops and also performance also high now a days power consumption is one of the top issues of vlsi design for which cmos latest technology. a days present digital vlsi world concentrate on only low power design only, low power devices are like mobile phones, batteries etc.In previous days power consumption is secondary concern at that time concentrate on area and performance. Now a days

Technology scaling due to this leakage power increases, to solve power dissipation many researches have implemented different thoughts from device level to the architecture level, however there is no universal way to avoid trade-off between power, delay and area and thus designers takes a appreciate technique that satisfy application and product needs. In order to get a high density and high performance of cmos.

II. EXISTING FLIP FLOP DESIGNS

### A. Conventional Explicit Type P-FF Designs

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate [7]. Without generating pulse signals explicitly, implicit type P-FFs are in general more power-economical.
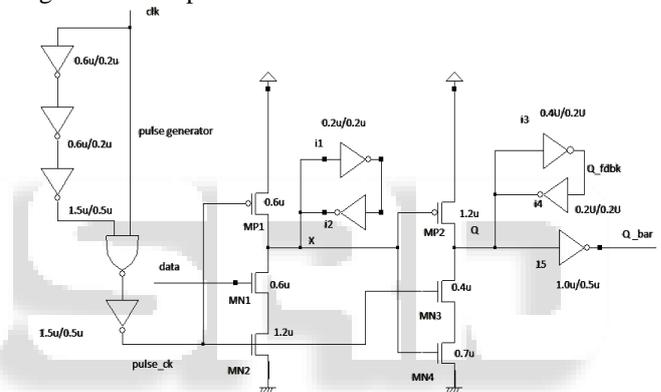

However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an *n*-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.

To provide a comparison, some existing P-FF designs are reviewed first. Fig. 1(a) shows a classic explicit P-FF design, named data-close to-output (ep-DCO) [7]. It contains a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node *X*. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node *X* is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation..To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed [10]–[9].

Conditional discharged (CD) technique: An extra nMOS transistor MN3 controlled by the output signal Q_ fdbk is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node X is simplified
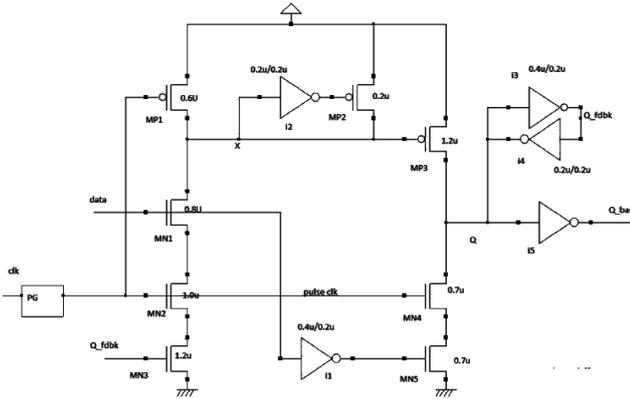
and consists of an inverter plus a pull-up pMOS transistor only Static condition discharge flip flop: Fig. 1(c) shows a similar P-FF design (SCDFF) using a static conditional discharge technique [17].
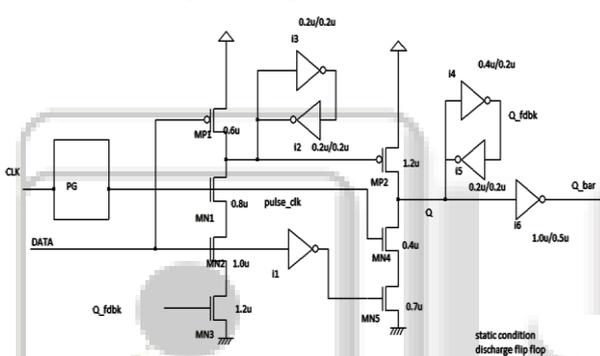
It differs from the CDFF design in using a static latch structure. Node X is thus exempted from periodical pre charges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The modified hybrid latch flip flop shown in figure
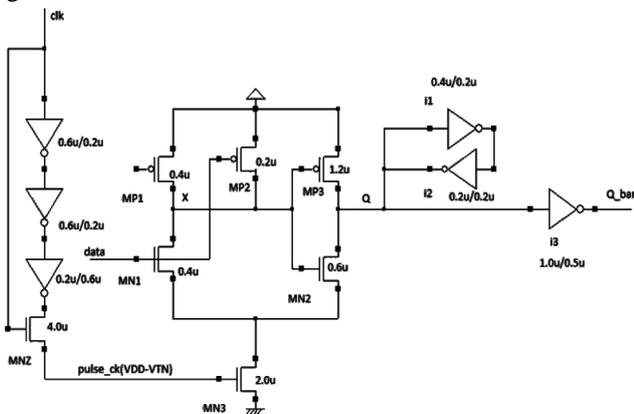

Fig. 1(d) also uses a static latch. The keeper logic at node X is removed. A weak pull-up transistor MP1controlled by the output signal Q maintains the level of node X. when Q equals 0. Despite its circuit simplicity, the MHLFF design

en counters two drawbacks. First, since node X is not pre discharged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT) is applied to the discharging transistor MN3. Second, node X becomes floating in certain cases and its value may drift causing extra dc power [18].

B. Pulse Triggered Flip Flop

1) Pulse triggered –Flip Flop Design

Recalling the four circuits reviewed in Section II-A, they all encounter the same worst case timing occurring at 0 to 1 data path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging transitions. Referring to Fig. 2(a), the proposed design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure
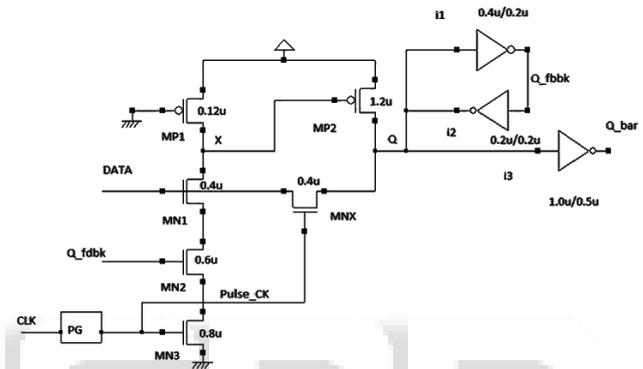

And a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved.In addition to the circuit simplicity, this approach also reduces the load capacitance of node X [20], [21]. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly Pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging node Q during "1" to "0" data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feed through. This scheme actually improves the "0" to "1" delay and thus reduces the disparity between the rise time and the fall time delays. In comparison with other P-FF designs such as ep-DCO, CDFF, and SCDFF, the proposed design shows the most balanced delay behaviors.

III. PROPOSED PULSE TRIGGERED FLIP FLOP USING SLEEP TRANSISTOR

A. *Transmission Gate*
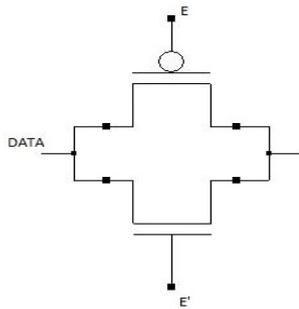
The CMOS transmission gate consists of two MOSFETs, one n-channel responsible for correct transmission of logic zeros, and one p-channel, responsible for correct transmission of logic ones. Here transmission gate used to find out circuit will be active mode or sleep mode. Where lines connect only to logic 1 the nMOS devices may be omitted. Where lines connect only to logic 0 the pMOS devices may be omitted.
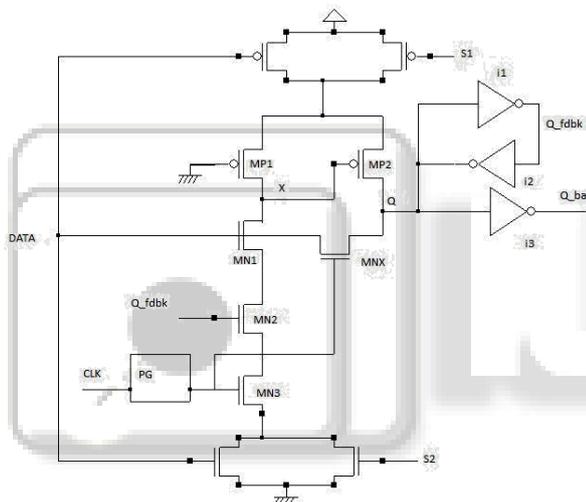
The sleepy stack technique divides existing transistor into two transistor each typically with same width w1half of the original single transistor 's' width w0(w1=w0/2).then sleep transistor are added in parallel to one of the transistor in each set of two stacked transistor ,changing sleep transistor width may provide additional trade off" s between delay, power and area .The sleepy stack works during active mode and sleepy mode. Generally any flip flop in normal mode it need to enter a active mode we can use drive this circuit to use another driving circuit that is transmission device by using transmission device circuit we can know the circuit will be active mode or sleep mode. The sleep mode transistor control input's' is controlled by input driving transmission device control inputs

Whenever E=0 circuit will be active mode
Whenever E=1 circuit will be sleep mode

In this sleep transistor PMOS is connected between vdd and virtual vdd and also sleep nmos connected between vss and virtual vss .when ever circuit active mode at the time sleep transistor on state through power supplies and also whatever data present in the input that will be copied in the output. When ever sleep transistor off mode by cutting

off power rails then disconnect vdd and vss ,there is no leakage power in circuit ,it is called as standby mode.

IV. SIMULATION RESULTS

The performance of the proposed P-FF design is evaluated against existing designs through post-layout simulations

A. *Simulation Waveforms*

1) *Wave form for explicit Flip Flop*

These are performs a normal mode of flip flop .whenever data entering into the at the 1 or 0 state at that time whatever data present that will be passed through the output. The output responds in the input only at the positive or negative edge of the clock input.
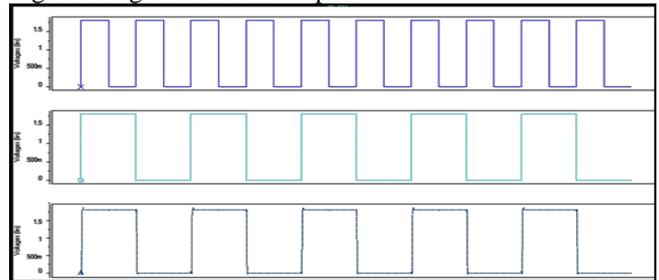

Fig. 6.1: explicit Flip Flop
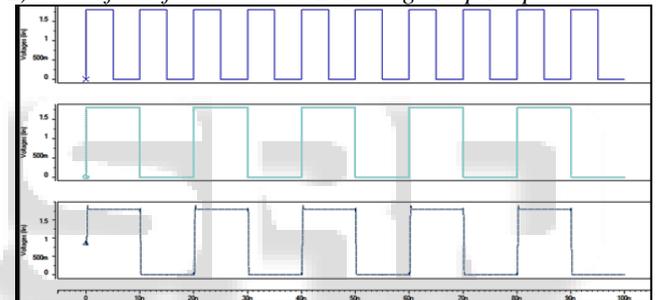
2) *Waveform for Condition Discharge Flip Flop*

Fig. 6.2: condition discharge Flip-flop

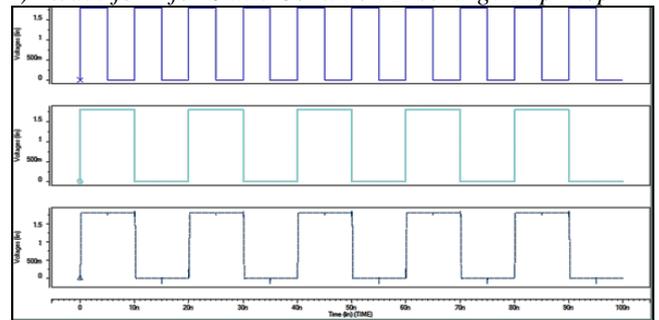#### 3) *Wave form for Static Condition Discharge Flip Flop*

Fig. 6.3: Static condition discharge Flip Flop
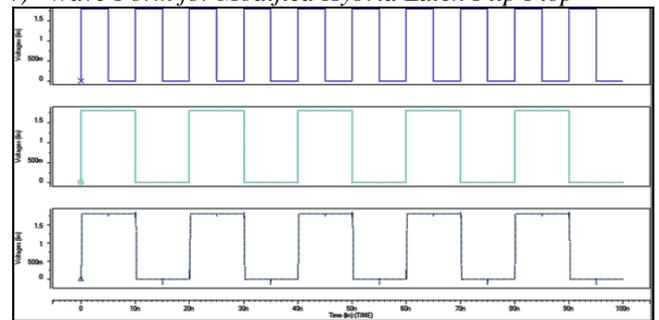
4) *Wave Form for Modified Hybrid Latch Flip Flop*

Fig. 6.4: Modified hybrid latch Flip Flop

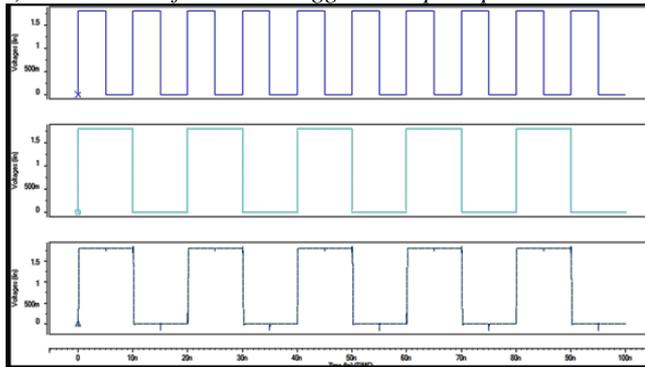### 5) Wave Form for Pulse Triggered Flip Flop

Fig. 6.5: pulse triggered Flip Flop
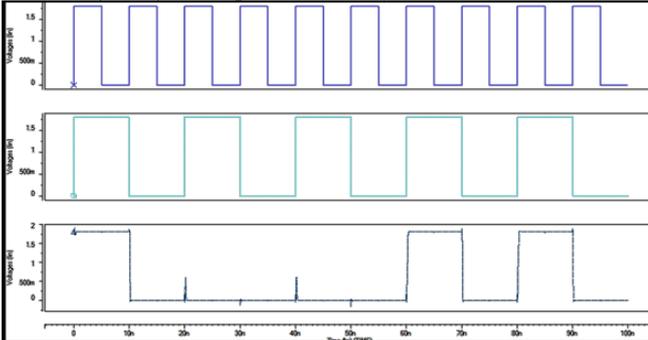
6) Waveform for Proposed P FF System

Fig .6.6: Proposed method

B. Power Performance Analysis of Flip Flop

Paramet ers	EPF F	CDF F	SCD FF	MHL FF	PFF	PROPOS ED PFF
Avg Power (uw)	18.49	18.04	19.20	17.92	17.91	14.25
Delay (ps)	173.7	128.7	155.16	86.74	9.144	9.8
Power delay Product	3.211	2.322	2.97	1.55	0.16	0.13

Table 1: Power Performance Analysis Of Flip Flop

V. CONCLUSION

In this thesis the various flip flop design like EP DCO, MHLFF, SCDFF, CDFF based on a pulse flip flop and new proposed flip flop are discussed.

That is sleep transistor technology is used to reduce unnecessary power dissipation in the circuit. These employee new design measures, the successfully reduces power dissipation in the flip flop and also solves discharging problem. These were has been designed Hspice tool those result wave forms are discussed with these result performed pulse flip flop better power than remaining flip flops.

REFERENCES

[1] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," IEEE J. Solid-State Circuits, vol. 33, no. 5,pp. 807–811, May 1998.

[2] Fabian Klass, Chaim Amir, Ashutosh Das, Kathirgamar Aingaran, Cindy Truong, Richard Wang, Anup Mehta, Ray Heald, and Gin Yee " A New Family of Semi dynamic and Dynamic Flip-Flops with Embedded Logic for High-Performance Processors".

[3] James Tschanz, Siva Narendra, Zhanping Chen, Shekhar Borkar, Manoj Sachdev, and Vivek De "Comparative Delay and Energy of Single Edge-Triggered & Dual Edge-Triggered Pulsed Flip-Flops for High- Performance Microprocessors".

[4] Bai-Sun Kong, Sam-Soo Kim, and Young-Hyun Jun "Conditional- Capture Flip-Flop for Statistical Power Reduction".

[5] Peiyi Zhao, Student Member, IEEE, Tarek K. Darwish, Student Member, IEEE, and Magdy A. Bayoumi, Fellow, IEEE "High-Performance and Low- Power Conditional Discharge Flip-Flop".

[6] Ying-Haw Shu, Member, IEEE, Shing Tenqchen, Senior Member, IEEE, Ming- Chang Sun, and Wu-Shiung Feng, Senior Member, "XNOR-Based Double-Edge-Triggered Flip-Flop for Two-Phase Pipelines".

[7] Hamid Mahmoodi, Member, IEEE, Vishy Tirumalashetty, Matthew Cooke, and Kaushik Roy, Fellow, IEEE "Ultra Low-Power Clocking Scheme Using Energy Recovery and Clock Gating".

[8] Peiyi Zhao, Jason McNeely, Weidong Kuang, Nan Wang, and Zhongfeng Wang "Design of Sequential Elements for Low Power Clocking System".

[9] Seyed E. Esmaeili, Asim J. Al-Kahlili, and Glenn E. R. Cowan "Low- Swing Differential Conditional Capturing Flip-Flop for LC Resonant 1Clock Distribution Networks".

[10] Y.-T. Hwang, J.-F. Lin, and M.-H. Sheu, "Low power pulse triggered flip-flop design with conditional pulse enhancement scheme,".