A CMOS Phase Locked Loop based PWM Generator using 90nm Technology

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Abstract— A CMOS class D phase locked loop based PWM generator is presented in this paper. The implementation is done in a 90nm CMOS process using CADENCE tool. The architecture in this project eliminates the requirements for a high-quality carrier generator and a high-speed voltage comparator that are often required in PWM implementations. Voltage comparison is replaced by Phase comparison and precise ramp signal is replaced by Reference clock. Phase comparison is fast and accurate when compared to voltage comparison. Reference clock does not have a stringent linearity requirement like precise ramp signal. With this we can achieve a PWM signal with 70% duty cycle.

Key words: PWM, Duty Cycle, Phase Detector, Class D, Phase Locked Loops, Pulse Width Modulation

I. INTRODUCTION

PWM architectures often rely on the use of a precise ramp signal. In such systems, the input is compared to the ramp, in order to provide a PWM output. If a similar architecture is employed for signals at higher frequencies, the switching frequency can also be expected to increase by a similar order. In this case, the use of conventional ramp-based PWM schemes can be impractical. One reason is that the required ramp signal frequency can be in the range of several MHz, where achieving such low distortion can be extremely challenging. Further, generation of an accurate ramp signal at this frequency ramp signal. For natural sampling PWM (NSPWM) to be employed, the linearity of the ramp over time is critical. A bandwidth limitation at the input of the comparator, or within the comparator itself, can cause the ramp to deviate from its linear dependence on time, thereby leading to distortion. Another challenge is that the voltage comparator has to make decisions with inputs in the range of sub-mV, where the comparator is vulnerable to noise and spurs. Additionally these decisions need to be made over a wide range of the input. These design issues become progressively more challenging as the switching frequency is increased.

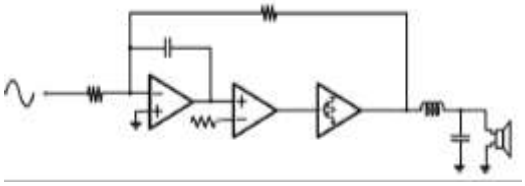

Fig. 1: Convetional PWM generator using ramp signal

The power dissipation and efficiency performance in linear mode amplifiers may not be competitive compared to switching amplifiers. The efficiency of an ideal class B amplifier decreases in a near-linear manner as signal amplitude drops. The peak ideal efficiency of a class B amplifier is 78%, however, if the output power has to be backed off by 10 dB to accommodate the peak-to-average ratio of the modulation, as in the case above, then the best operating efficiency of the class B amplifier is nearly 25%. The efficiency performance of a class AB amplifier is further degraded due to quiescent current consumption. Furthermore, if the transistor channel length is scaled due to migration to a finer technology, a higher quiescent current is required to maintain the same gain because of increased transistor loss owing to relatively lower device output resistance. Thus we explore the use of Class-D amplifiers employing PWM for such wider bandwidth applications as well.

II. PROPOSED PWM GENERATOR

Fig. 2 depicts the PLL-based PWM Class-D driver described in this work. In this architecture, the phase detector compares the phase of a voltage controlled oscillator (VCO) to that of a reference clock. The phase detector has a two-level output, which is used to drive a power stage. The output of the power stage is fed back to an analog low-pass loop filter and subtracted from the analog input. Compared to a PLL used for frequency synthesis, the charge pump is replaced by a power stage and a modulated analog input signal is injected into the loop filter. The signal of interest here is the output of the power stage which is driven by the PD (phase detector), unlike a PLL employed for frequency synthesis, where the output of the VCO is the signal of interest. If we assume that the VCO free running frequency is identical to then the frequency of the Class-D stage must be at the output of the phase detector. The phase detector performs a continuous-time comparison of the phases of the VCO and the reference, and generates an output that is proportional to the phase difference. The loop enforces the requirement that the VCO control line must ideally have a zero average in locked state. Thus the differential input of the low-pass filter, within the bandwidth of the filter, must have a zero average. This can be achieved only if the low-frequency content of the power stage output is a negative replica of the input base-band signal which ensures that the output of the power stage has to be PWM.

Compared to a ramp-based PWM generator, the PLL-PWM approach offers two key advantages. First, the voltage comparison is replaced by phase comparison, which can be fast and accurate in deep submicron technologies, and benefit from process scaling. Second, the ramp signal is substituted by a reference clock, e.g., a sinusoid, which does not have a stringent linearity requirement.

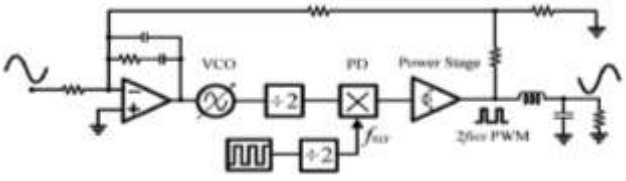

Fig 2: Proposed PWM Generator

Moreover, since the phase detector drives the output stage, the requirement on phase noise or jitter of the reference clock is relaxed, due to a high-pass noise transfer function. In the proposed design the reference clock frequency and the loop VCO signal are divided by two in order to achieve 50% duty cycleclocks. A non-50% duty cycle clock can lead to instability, which is analyzed in below. Stability in this context is defined as the ability of the loop to achieve and sustain locked operation.

III. CIRCUIT IMPLEMENTATION

A. Two Stage Differential Amplifier

The op amp used in this architecture is a two stage differential amplifier. The first stage in Fig. 3 consists of a p-channel differential pair M1-M2 with an n-channel current mirror load M3-M4 and a p-channel tail current source M5. The second stage consists of an n-channel common-source amplifier M6 with a p-channel current-source load M7. Because the OP-AMP inputs are connected to the gates of MOS transistor, the input resistance is essentially infinite when the OP-AMP is used in internal applications. For the same reason, the input resistance of the second stage of the OP-AMP is also essentially infinite

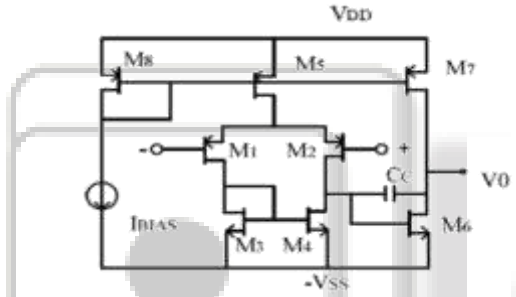

Fig. 3: Block diagram of two stage differential amplifier

The two stage shematic design is implemented in cadence tool as shown in fig 4. The fully differential two stage operational amplifier is fed with 5mV, 1KHz sinusoidal input signal. A bias current of 30uA is applied. The circuit is powered with positive and negative power supplies of 2.5V.

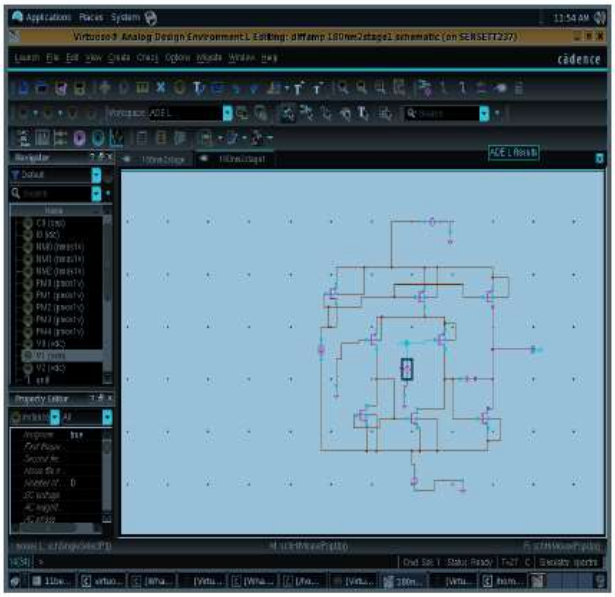

Fig 4: Implementation of two stage differential amplifier

B. Power Stage Design and Implementation

The power stage is also implemented in the 90nm CMOS process. The power stage uses cascade devices to improve reliability since it is supplied by a high voltage, such as 4.8 V. The H-bridge is driven by gate drivers that provide non overlapping signals to the output stage, in order to prevent current shoot-through in either leg of the H-bridge. The non-overlapping circuit improves efficiency by avoiding the loss that would occur if large shoot-through currents were allowed to flow, especially when the switching frequency is very high, in the range of 10–20MHz.A level shifter is designed as an interface between the high-voltage PA and low-voltage digital blocks. The H-bridge supply is separated from that of the gate driver for reducing supply ringing. Using a common power supply in these two stages can lead to the formation of a feedback loop through the supply connection, which can cause significant supply bounce due to package bond-wires. The gate driver supply is connected in series with a 10 resistor to lower the quality factor of the network formed by the parasitic inductance of bond-wire and on-chip decoupling capacitor, which is approximately 10 Pf. The size of the inductor is 500 nH for the switching frequencies employed here that are in the range of 10–20 MHz. The PD is implemented with an exclusive NOR gate

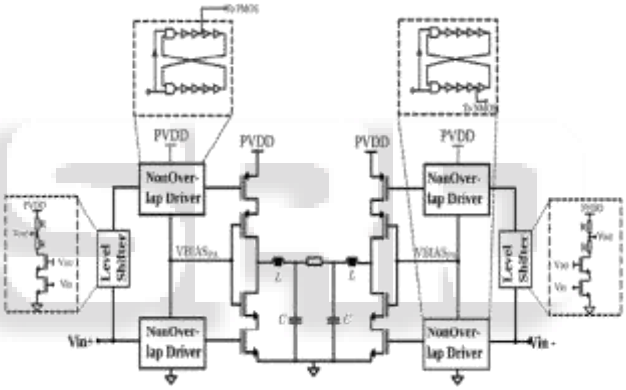

Fig. 5: Power stage design

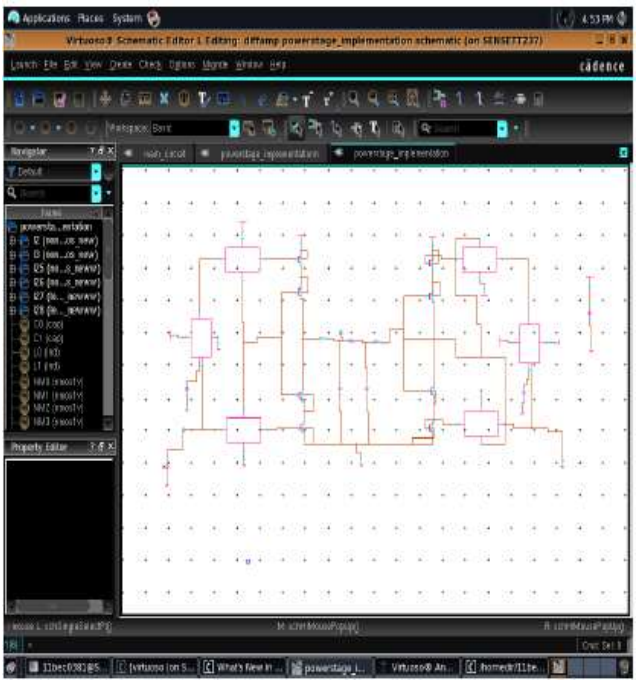

Fig. 6: Power stage implementation

The output of the phase detector is fed as an input to the power stage. The output power stage is powered with 3.2V and 4.8V power supplies.

C. Level Shifter

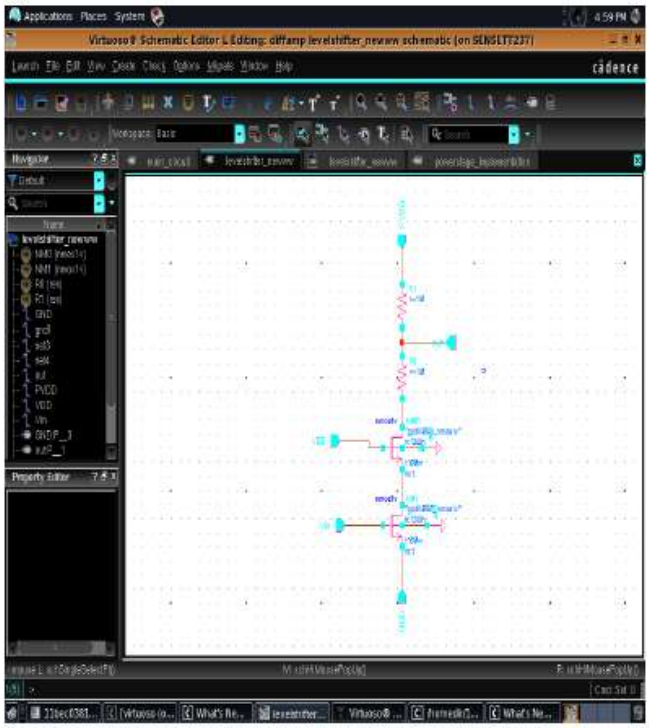

Fig 7: Schematic of level shifter

The level shifter is acts as an interface between the high-voltage PA and low-voltage digital blocks. It is powered with 3.2V power supply.

D. Non Overlap Driver

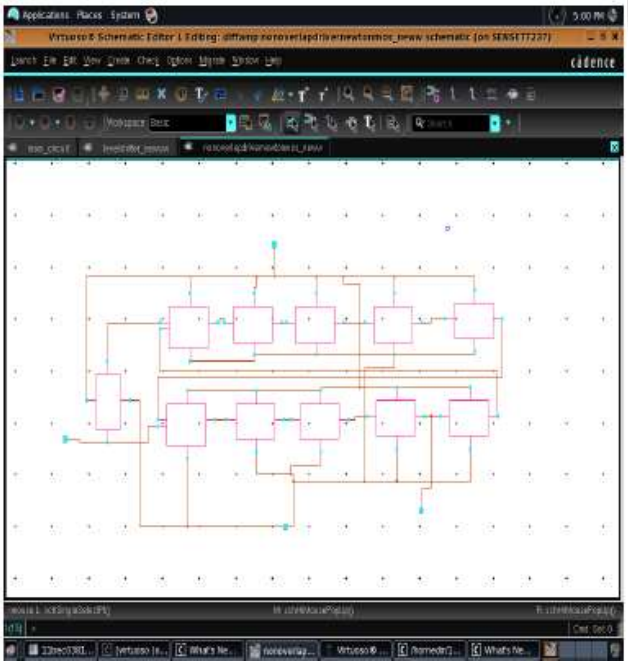

Fig. 8: Non Overlap driver

Non Overlap Driver is RS flip-flop. It sets the true and complement of the waveform. The inverter provide delays so that when p-channel output transistor is ON the n-channel is OFF and vice-versa.

E. Voltage Controlled Oscillator

The VCO cell is a current-starved inverter as shown in fig 9. A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. This current starved VCO is designed using ring oscillator and its operation is also similar to that. From the schematic circuit shown in the Fig. 2.2, it is observed that MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for the current. The MOSFETs M5 and M6 drain currents are the same and are set by input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage. The upper PMOS transistors are connected to the gate of M6 and source voltage is applied to the gates of all lower NMOS transistors. This digital-intensive design has a low area requirement since it does not require inductors, in addition to low complexity. Both the VCO and the op amp are powered by a 1.2 V supply from an on-chip voltage regulator, which helps to reduce the noise coupling from the integrated PA through the supply bond-wires or substrate. The design is laid out such that the analog power grounds and supplies are orthogonal to those of the power stage, which reduces mutual coupling arising from bond-wires in the package.

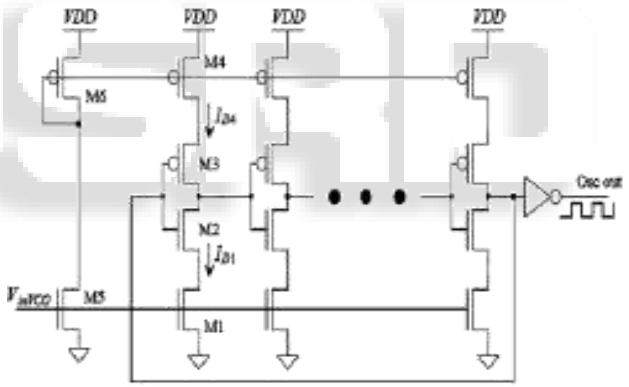

Fig. 9: Current starved VCO

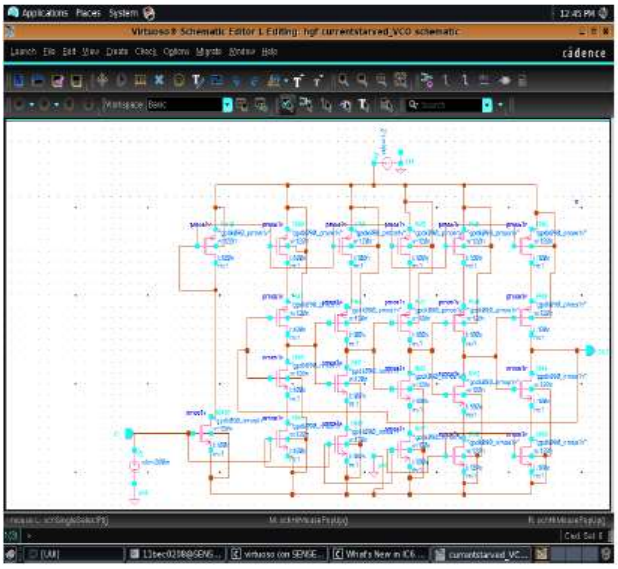

Fig 10: Schematic of current starved VCO

A current starved VCO is implemented whose operation is similar to that of the ring oscillator. It is powered with a power supply of 1.2V. The variations of output frequency of the VCO with respect to the control voltage and power supplies are analyzed.

F. Frequency Divider

Frequency divider is implemented using D flip-flop. The complemented output of the D flip-flop is fed back. D flip-flop is implemented using two input and three input NAND gates.

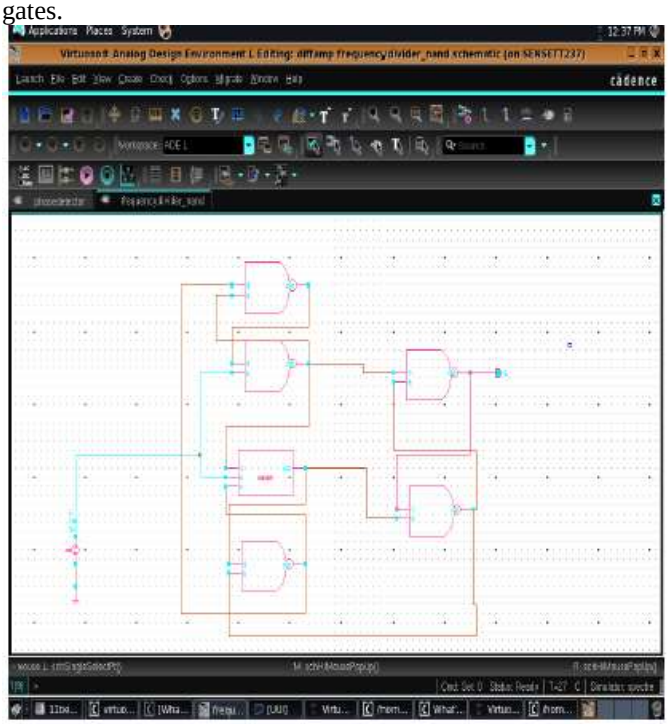

Fig 11: Schematic of Frequency Divider

G. Phase Detector

Phase detector is implemented using XOR gate. XOR gate is implemented using NAND gate.

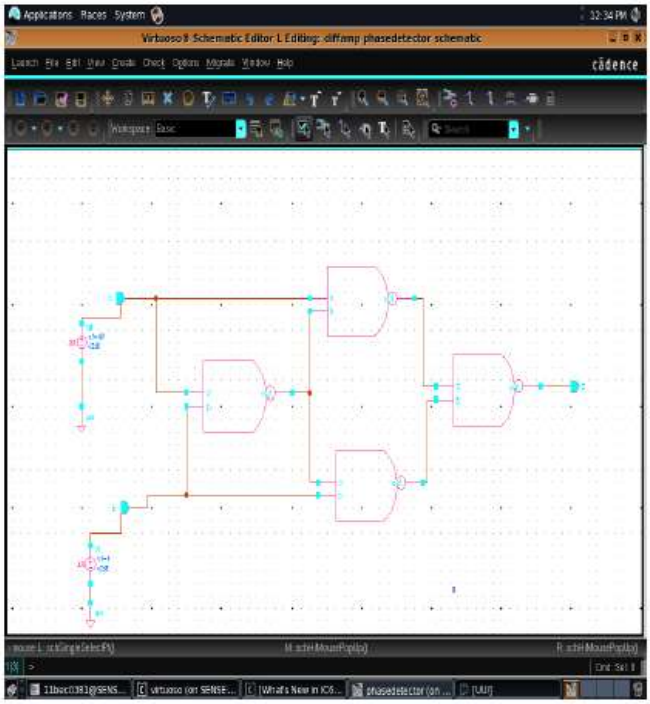

Fig 12: Phase Detector

H. Final Implementation of PWM Generator

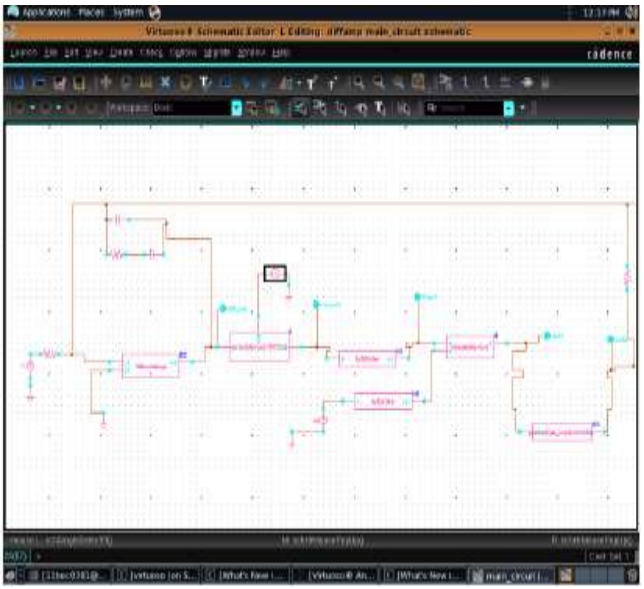

Fig. 13: Schematic1 of PWM Generator

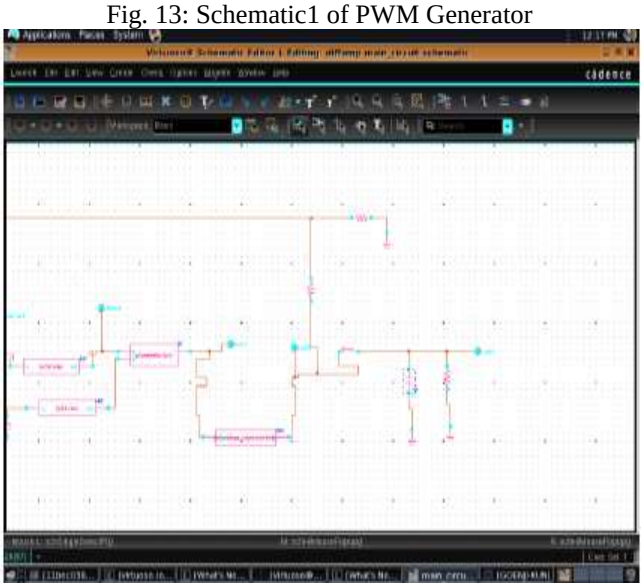

Fig 14: Schematic2 of PWM Generator

IV. RESULTS

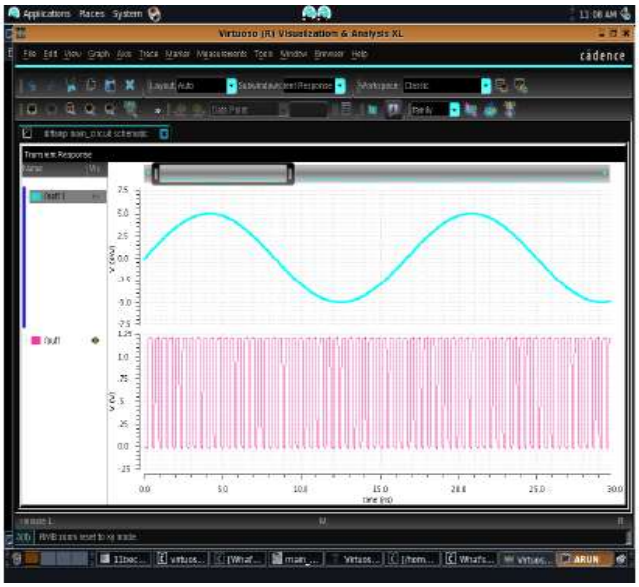

Fig. 15: Waveform at the output of Phase Detector

Finally here we achieve PWM signal with 70% duty cycle.

V. CONCLUSION

The analysis and design of a high performance PLL-based Class-D line driver is presented in this thesis. The presented approach eliminates the requirements for a high-quality ramp generator and fast voltage comparator that are the primary sources of distortion in conventional ramp-based PWM systems. This makes the approach useful for applications such as powerline communications. This work processes the input signal in the phase domain, and as such is expected to be a promising approach for high speed PWM generation..

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