Design of Quaternary Signed Digit Adder

Bhavya Sree Kotte[1] S Saleem Malik[2]
[1,2]Department of Electronics & Communication Engineering
[1,2]SITS, Kadapa, Andhra Pradesh, India

Abstract— Now-a-days adders are mostly used in various electronic applications such as Digital signal processors and computing devices. Adders are used to perform various algorithms like FIR, IIR etc. In Modern electronics, Digital systems play a prominent role in day to day life. Arithmetic operations such as addition, subtraction and multiplication still suffer from known problems including limited number of bits, propagation time delay, and circuit complexity. The speed of digital processor depends heavily on the speed of adders they have constraints like area, power and speed requirements. The delay in an adder is dominated by the carry chain. In adders Binary Signed Digit Numbers are known to allow limited carry propagation with more complex addition process. Some of the limitations of this system are computational speed which limits formation and propagation of carry especially as the number of bits increases. Therefore it provides large complexity and low storage density. Carry free arithmetic operations can be achieved using a higher radix number system such as Quaternary Signed Digit (QSD). In present study, QSD number system eliminates carry propagation chain which reduces the computation time substantially, thus enhancing the speed of the machine. QSD Adder or QSD Multiplier circuits are logic circuits designed to perform high-speed arithmetic operations. A higher radix based signed digit number system, such as quaternary signed digit (QSD) number system, allows higher information storage density, less complexity. A high speed area effective adders and multipliers can be implemented using this technique. Carry free addition and other operations on a large number of digits such as 64, 128, or more can be implemented with constant delay and less complexity. The Design is simulated & synthesized using Xilinx 10.1.

Key words:

I. INTRODUCTION

A binary signed digit representation of an integer k ∈ [0, 2n− 1] is a base-2 representation denoted by (Kn, Kn−1, . . . , K0) BSD where κi ∈ {−1, 0, 1}. A binary signed digit representation of an integer k ∈ [0, 2n− 1] is a base-2 representation denoted by (Kn, Kn−1. . . K0) BSD where κi ∈ {−1, 0, 1}. We will call the K is signed bits, or s bits for short, and -1 will be written as 1. An integer can have several BSD representations. For example, k = (9)10 can be written as (01001) BSD.

Among the possible BSD representations of an integer there are two unique representations. Modern computers are based on binary number system (radix =2). It has two logical states ‘0’ and ‘1’. In such system, ‘1’ plus ‘1’ is ’0’ with carry ‘1’ (i.e. 1+1=10). This carry should have to add with another ‘1’, as a result further carry ‘1’ generates. This creates the delay problem in computer circuits.

The simplest arithmetic operation in binary is addition. Adding two single-digit binary numbers is relatively simple, using a form of carrying:
0 + 0 → 0
0 + 1 → 1
1 + 0 → 1
1 + 1 → 0, carry 1
(since 1 + 1 = 2 = 0 + (1 × 21))

Adding two "1" digits produces a digit "0", while 1 will have to be added to the next column. This is similar to what happens in decimal when certain single-digit numbers are added together; if the result equals or exceeds the value of the radix (10), the digit to the left is incremented:
5 + 5 → 0, carry 1
(since 5 + 5 = 10 = 0 + (1 × 101))
7 + 9 → 6, carry 1 Quaternary Signed Digit (QSD), *FIR*, Simulation of Full Adder module
(since 7 + 9 = 16 = 6 + (1 × 101)

A. *Quaternary Signed Digit Number*

A carry-free arithmetic operation can be achieved using a higher radix number system such as Quaternary Signed Digit (QSD). In QSD, each digit can be represented by a number from-3 to 3. The redundancy associated with signed-digit numbers offers the possibility of carry free addition. The redundancy provided in signed-digit representation allows for fast addition and subtraction because the sum or difference digit is a function of only the digits in two adjacent digit positions of the operands for a radix greater than 2, and 3 adjacent digit positions for a radix of 2. Thus, the add time for two redundant signed-digit numbers is a constant independent of the word length of the operands, which is the key to high speed computation.

B. *Aim of the project:*

Design and implementation of fast Addition by Using Quaternary Signed Digit (QSD) Number System. In this project we are design a new adder system based on high radix Number System to achieve carry free addition. We are using Quaternary Signed Digit Number System to design a 32-bit adder, So it is named as QSD adder. Advantage of Signed Number System is we can represent a digit in more than one form, this will help us to eliminate carry in addition process.

II. PROPOSED SYSTEM

A carry-free arithmetic operation can be achieved using a higher radix number system such as Quaternary Signed Digit(QSD). In QSD, each digit can be represented by a number from-3 to 3.QSD is a signed digit number system so we can represent a single number in more than one unique form, for example 3 can be represented by 11 QSD numbers have redundancy. This is the biggest advantage for QSD number system adders over the binary number system adders to achieve the carry free addition. The redundancy associated with signed-digit numbers offers the possibility

of carry free addition. The redundancy provided in signed-digit representation allows for fast addition and subtraction because the sum or difference digit is a function of only the digits in two adjacent digit positions of the operands for a radix greater than 2, and 3 adjacent digit positions for a radix of 2. Thus, the add time for two redundant signed-digit numbers is a constant independent of the word length of the operands, which is the key to high speed computation.

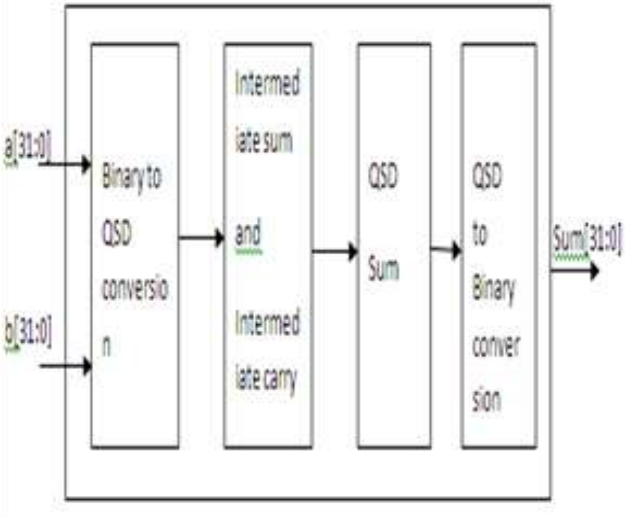


Fig. 1: Quaternary Signed Digit (QSD)

A. QSD Sum Generator

The final sum which is carry free is generated from Intermediate carry (IC2, IC1, and IC0) and Intermediate sum (IS2, IS1, and IS0). Therefore QSD Sum Generator has six input and three output bits as shown in figure.

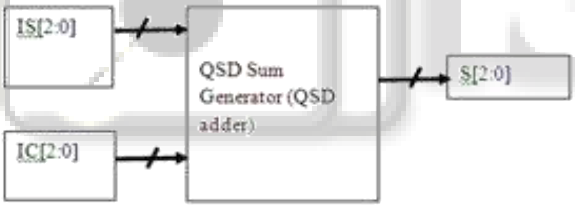


Fig. 2: QSD Sum Generator

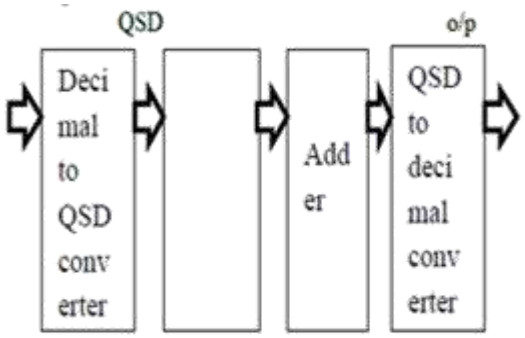
B. Design of QSD Adder

It offers the advantage of reduced circuit complexity both in terms of transistor count and interconnections. QSD number uses 25% less space than BSD to store number. QSD numbers save 25% storage compared to BSD:

So the proposed QSD adder is better than RBSD adder in terms of number of gates, input connections and delay though both perform addition within constant time. Proposed design has the advantages of both parallelisms as well as reduced gate complexity. The computation speed and circuit complexity increases as the number of computation steps decreases. A two-step scheme appears to be a prudent choice in terms of computation speed and storage complexity. Quaternary is the base 4 redundant number system. The degree of redundancy usually increases with the increase of the radix. The signed digit number system allows us to implement parallel arithmetic by using redundancy. QSD numbers are the SD numbers with the digit set as:

$$D = \sum_{i=0}^{n} x_i \, 4^i$$

Where *xi* can be any value from the set $\{\bar{3}, \bar{2}, \bar{1}, 0, 1, 2, 3\}$ for producing an appropriate decimal representation. For digital implementation, QSD numbers are represented using 3-bit 2's complement notation. A QSD negative number is the QSD complement of the QSD positive number. In QSD number system carry propagation chain are eliminated which reduce the computation time substantially, thus enhancing the speed of the machine. As range of QSD number is from -3 to 3, the addition result of two QSD numbers varies from -6 to +6. The decimal numbers in the range of -3 to +3 are represented by one digit QSD number.



Block diagram of QSD conversion

Step 1: First step generates an intermediate carry andintermediate sum from the input QSD digits i.e., addend and augend.

Step 2: Second step combines intermediate sum of current digit with the intermediate carry of the lower significant digit.

Fig. 3: Design of QSD Adder

III. SIMULATION RESULTS

A. Simulation of Full Adder Module

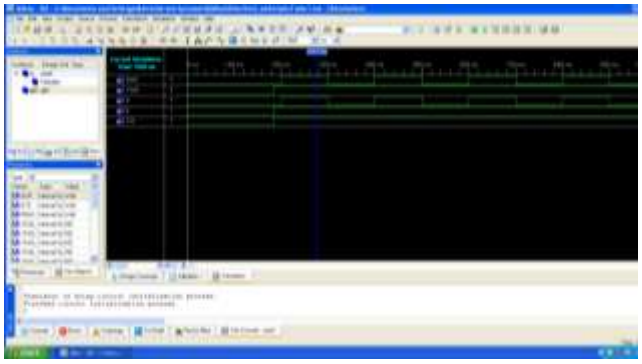


Fig. 4: Simulation of Full Adder module

B. RTL Diagram

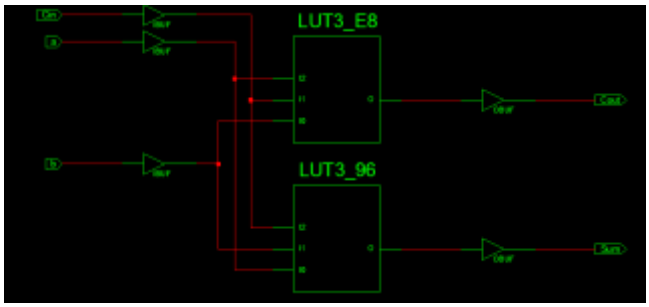


Fig. 5: RTL Diagram

C. Simulation of IS and IC Generator

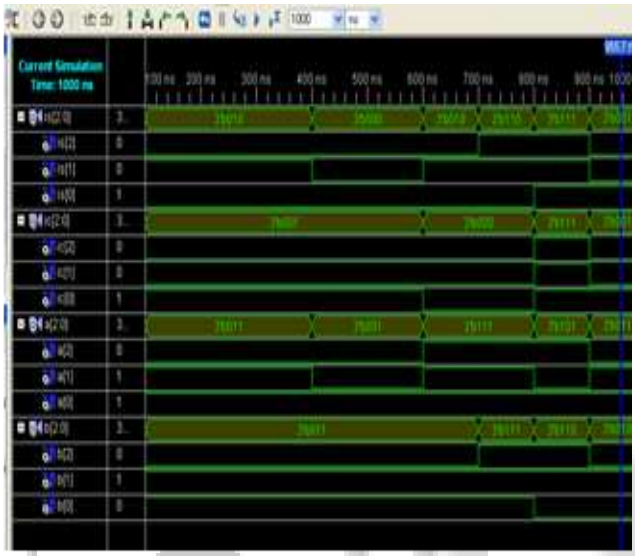


Fig. 6: Simulation of IS and IC Generator

D. Simulation of QSD Generator

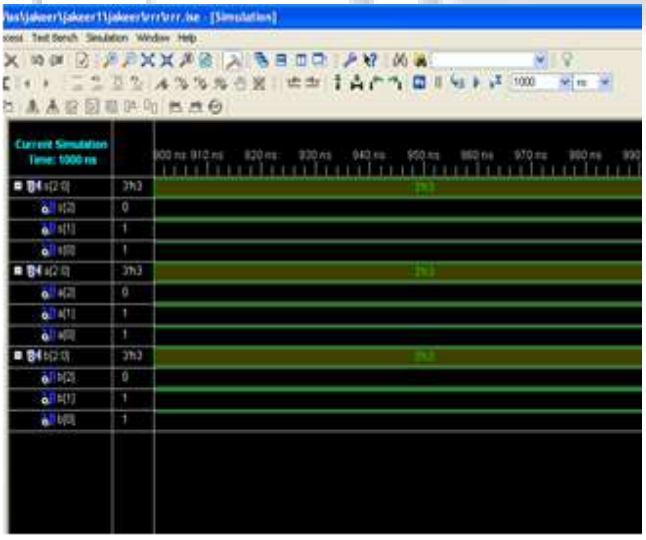


Fig. 7: Simulation of QSD Generator

E. RTL Schematic Diagram

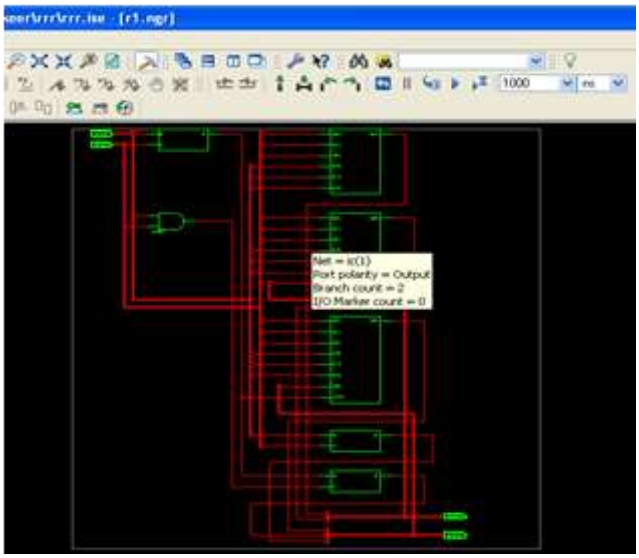


Fig. 8: RTL Schematic Diagram

F. Result Analysis

S.No	Number Representation	Binary signed digit number	QSD one bit representation
1	No. of Luts	25	15
2	Delay	20.265ns	11.620ns
3	Timing	8.00sec	4.00sec
4	Total Real time Xst completion	202572 kilobytes	156924 kilobytes
5	Utilization	18%	13%

Table 1: Differences between BSD QSD One bit and QSD one bit

IV. CONCLUSION

In the proposed work Quaternary Signed Digit adder using NAND-NAND implementation for single digit addition, has been designed. The performance of these adders is evaluated by reducing the circuit complexity and their computations. The designed adder using QSD number representation allows fast addition or subtraction is capable of carry free addition and borrows free subtraction. The carry propagation chain is eliminated hence it reduces the propagation time in comparison with radix 2 system, thus enhancing the speed of the machine These designed circuits consume less energy and power which shows better performance in the design analysis. The QSD adder proposed is better than other binary adders in terms of number of gates and higher number of bits addition within constant time.

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