Design of the Physical Layer of PCI Express using VHDL

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Abstract— PCI Express (PCIe) is the newest name for the technology formerly known as 3GIO. . It is used as a High speed communication protocol for connecting among different devices. According to PCI Express 1.0a, this paper presents the physical layer architecture. It uses packet data for reliable communication to transport the data from transmitter to receiver side. The paper presents the reliable conveying of data, with the addition of start and end bit to each TLPs and DLLPs in the transmit side, and how the packets are processed on the receiver side. The simulation is performed using Xilinx ISE 9.1 Software and coding is done using Very High Speed Integrated Circuit Hardware Description Language (VHDL).

Key words: PCI Express, Physical Layer, VHDL Code

I. INTRODUCTION

In today's modern era of communication, use of high speed data transfer system is must. Data transfer rate is mainly dependent on the data transfer protocol and the method of communication. These days, all high speed data communication are digital. Due to the requirements of the digital transmission rate in communications is becoming higher and also the need of high speed data transfer which lead to the development of PCI Express. Digital data communication method is more secure and less interfered by noise. The important thing is to select the protocol used for communication. There are many protocols like SPI, I2C, PCI, PCIE, and USB. PCI Express (Peripheral Component Interconnect Express), is a computer expansion card standard designed to replace the older PCI, PCI –X, and AGP standards[1][2].PCI-E is the latest standard used in personal computers which was introduced by INTEL. PCI Express is based on serial point-to–point interconnect which reduces the cost and design complexity. PCI Express serve as a general purpose I/O interconnect for wide variety of future computing and communication platform. The intent of this serial interconnect is to establish very high bandwidth communication [3].

A. Packet Flow:

PCI Express uses packet to communicate information between two devices. Packets are formed in the transaction and data link layers to carry the information from transmitter to receiver device. As the transmitted packets flow through the layers, they are extended with additional information necessary to handle packets at those layers. At the receiver side the reverse process occurs and the additional bits are terminated.

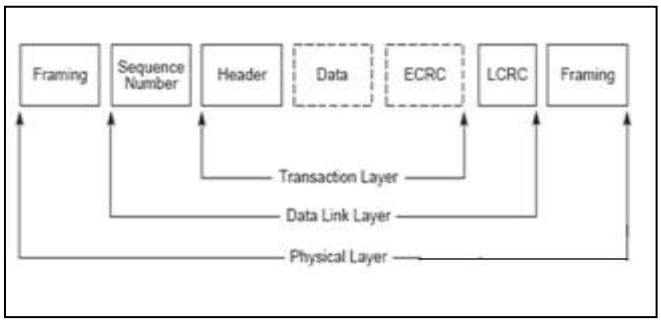

Fig. 1: Packet Flow through Layers

B. PCI Express Link:

A Link represents the dual simplex communication channel between two components. The fundamental PCI Express link consists of two Low voltage differential signal pairs: a Transmit pair and a Receive Pair. The connection between two PCI-E device is called as link. Each link is composed of one or more lanes. Each lane compose of one pair of signals: send and receive. This full-duplex communication is possible because each lane consist of one pair of signals: send and receive. PCI-E supports x1, x4, x8, x12, x16, and x32 link widths. A single lane is capable of transmitting 2.5Gbps in each direction simultaneously.

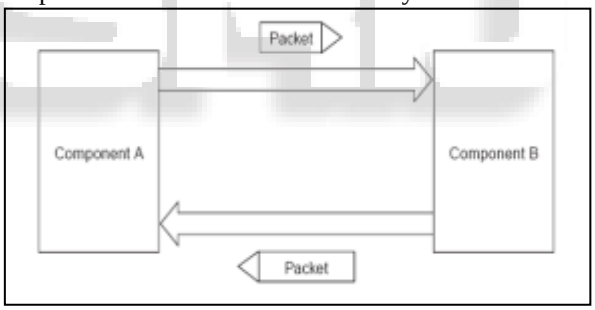

Fig. 2: PCI Express Link

C. PCI Express Layering Overview:

The PCI Express specification defines three discrete layers: The Transaction layer, the Data link Layer and the Physical layer. Each of these layer is further divided into two sections: one is the transmitter that processes outbound information and other is the receiver that processes inbound information[8].

The Transaction Layer is the topmost PCI Express architecture layer. Its primary function is the assembly and disassembly of transaction layer packets (TLPs), and is responsible for managing credit based flow control of TLPs.

The Data link Layer is the intermediate stage between transaction and data link layer. It provides reliable mechanism for the exchange of TLPs between two components on a link. It also provides service for error detection and recovery.

The Physical layer isolates the Transaction and Datalink Layer from the signaling technology used for link data interchange. It consist of Logical and electrical sub-

blocks. The Physical Layer is responsible for exchanging information with the data link layer in an implementation specific format. The Logical block consists of drivers and buffers, parallel-to-serial and serial-to-parallel conversion, scrambler circuitry.

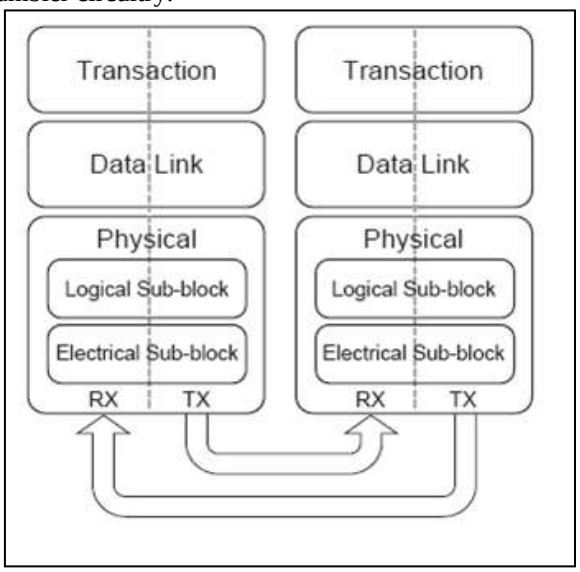

Fig. 2: PCI Express Layering

II. Literature Review

S. Monika. et.al.[12] in January 2014'. This paper implements the DC balanced 8B/10B coding in Super speed USB which employ a very fast FPGA from Xilinx family is proposed. Using the look-up table and memory with fast technique made this design efficient to be implemented. The Scrambling and descrambling modules are added in the above modules. This work can be extended by connecting this total module in between Link layer and Physical analog layer of USB 3.0architecture. Also the work can be extended to do the FPGA implementation by using SPARTAN 3E or Virtex V XILINX FPGA's. The Design of Physical layer coding can be rigorously tested if soft cores of link layer, physical analog layer are available. This can be an extended work for the present paper.

SatishK.Dhawan worked on PCI Express-A New High Speed Serial Data Bus. It is a very high speed dual-simplex, point to point serial differential low voltage interconnect. The signaling rate is 2.5 Gbit per second, with 8/10 bit encoding to embed the clock in the data stream. On the transmit side parallel data is shifted out serially and on the receive side serial data is shifted into registers for parallel data output. The data is shifted serially at 2.5GHZ to the printed circuit board traces or to the cable segment [5].

Hemant Kumar Soni,[11]et.al. The aim of this paper is to design and verify the physical layer implementation by using ISE 8.1 from Xilinx and Spartan 3 FPGA to reduce the cost and hardware.PCS is the sub layer of the physical layer of PCI Express 1.0. The major constituents of this layer are transmitter and receiver. Transmitter comprises of 8b/10b encoder. The Primary purpose of this scheme is to embed a clock into the serial bit stream of transmitter lanes with advancement in the design by reducing the utilized hardware resources within FPGA . No clock is transmitted along with the serial data bit stream. This eliminates EMI noise and provides DC balance. Receiver comprises of special symbol detector, elastic buffer and 8b/10b decoder. Disparity error and Decode error can be known though this module. This work uses VHDL to model different blocks of the PCS of physical layer of PCI Express. Then RTL code is simulated, synthesized and implemented using the ISE 8.1 from Xilinx and the Spartan 3 FPGA was targeted for implementation. In this paper we have reduced the hardware as well as cost of total system without affecting the speed of the PCI Express.

Ravi Budruck, et.al.[12] in September 2003. The book gave a brief description about why different blocks are required to process data to ensure the transmission is successful without any sort of error. The book contain information about design, verification and test , as well as background information essential for writing low level BIOS and device drivers.It also provided the different layers a data undergoes in PCI bus architecture. On further consultation it was decided to design the physical to physical layer transmission between the transmitter and receiver section.

III. Design Methodology

Understanding of PCI Express 1.0a Physical Layer architecture. According to the specification mentioned, designing each sub-blocks of Physical layer using VHDL. To develop effective communication between each sub-block of Physical Layer. The test bench verification is done to verify the correctness of the design module and its function simulation.

A. Physical Layer Design:

The proposed physical layer architecture consist of both transmitter and receiver.

1) Transmitter:

Transmit buffer receives TLPs and DLLPs from data link layer. The physical layer frames the packet with start and end character using control signal. The framing characters (start and end of packet) allows the receiver to easily detect the framing symbols.

With the aid of multiplexer, the packet data is framed with start and end character. The mux gates the data or control characters with the help of D/K signal. If the D/K signal is driven high then Transmitter buffer contents are gated otherwise start and end characters are gated out at the start and end of a packet respectively.

The scrambler uses an algorithm to pseudo randomly scramble each byte of packet. The start and end framing bytes are not scrambled. It eliminates repetitive patterns in the bit streams, which leads to EMI noise generation. Scrambling spreads energy over a frequency range and minimise noise.

The 8b/10b Encoder encodes the scrambled 8 bit character into 10 bit symbols. These are then converted into serial bit stream by the parallel-to-serial converter.

8b/10b Encoder performs DC balancing on transmission lines ,providing that there are enough state transitions for clock recovery. This coding scheme is used for high speed serial data Transmission.

2) Receiver:

The high speed deserializer on the receiver side converts the received serial data stream from serial-to-parallel.

The 10b symbol are converted back to 8b character by the 8b/10b decoder. It eliminates the start and end characters, that frames the packet and also look for errors.

The De-scrambler reproduces the de-scrambled packet stream from the incoming scrambled packet stream. It implements the inverse of the algorithm implemented in the transmitter scrambler.

Scrambling/descrambling are an algorithm that converts an input string into a seemingly random string of the same length to avoid simultaneous bits in the long format of data.

The receiver buffer stores the data received from the de-scrambler. The stored data is then feed back to the datalink layer.

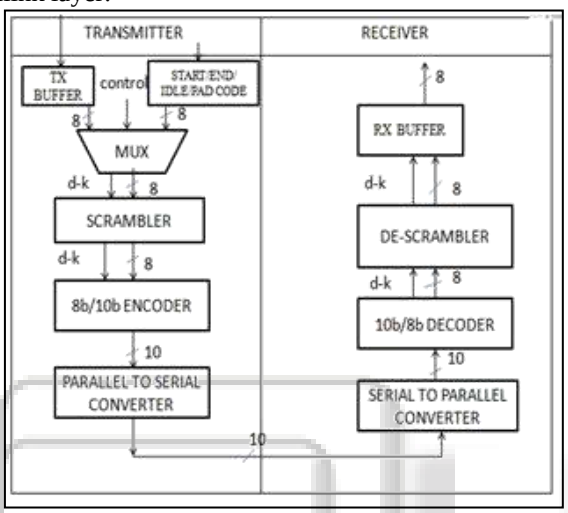

Fig. 3: Shows the Physical Layer Diagram

IV. SOFTWARE IMPLEMENTATION

The above figure shows the Physical layer architecture of PCI Express 1.0a x1 link i.e for 8 bit serial data transmission. In our work the 65h data from higher layer is assumed and stored in buffer.

This data is framed with start and end bit by using mux. The framed data is scrambled by the scrambler. Scrambling eliminates long strings of 1s and 0s with random strings of same length in order to avoid EMI noise. The 65h data is scrambled into 72h.

The framed data is passed onto 8b/10b encoder where it performs sufficient data transition for faster clock recovery. The 72h data is converted to 0D3h by encoder.

This encoded data is passed to Parallel to serial , serial to parallel block. The exact data 0D3h is obtained at the 10th clock cycle at the receiver side. This data is decoded by 8b/10b decoder to get 72h at the output.

The descrambled output obtained is 65h and is stored inside the buffer. The receiver buffer gives the final output 65h with framed byte.

A. Device Utilization Summary:

Number of Slices: 261 out of 960 27%
Number of Slice Flip Flops: 313 out of 1920 16%
Number of 4 input LUTs: 388 out of 1920 20%
Number of IOs: 21
Number of bonded IOBs: 21 out of 66 31%
Number of GCLKs: 1 out of 24 4%

Thus I had implemented the PCI Express Bus Physical layer XILINX ISE 9.1. The RTL VIEW and Simulation waveforms are shown below

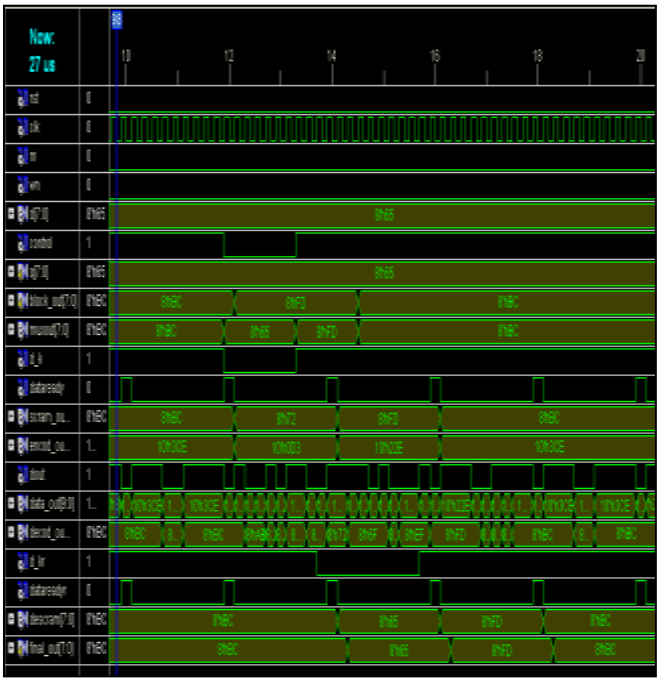

Fig. 4: Simulation Result

B. RTL View:

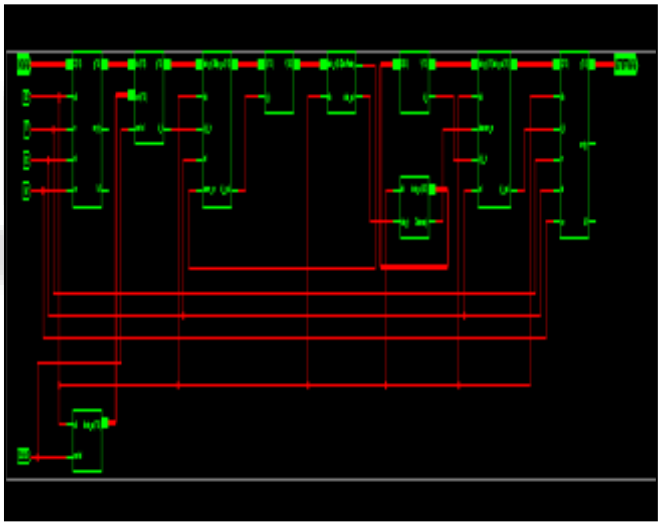

Fig. 5: RTL View of Complete System

V. CONCLUSION AND FUTURE WORK

This paper presents the design of PCI Express Physical layer architecture. The paper determines various sub-block functions of physical layer. It also depicts about peer-to-peer communication for transmitting data in serial manner between transmitter and receiver device. This paper can further be extended by designing data link layer and transaction layer of PCI Express. An improvement in PCI Express transfer rate can greatly improve system performance.

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